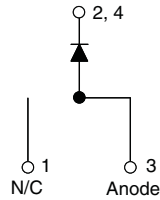


HEXFRED[®] Ultrafast Soft Recovery Diode, 8 A


D-PAK (TO-252AA)

FEATURES

- Ultrafast recovery time
- Ultrasoft recovery
- Very low I_{RRM}
- Very low Q_{rr}
- Guaranteed avalanche
- Specified at operating conditions
- Compliant to RoHS Directive 2002/95/EC
- Meets MSL level 1, per J-STD-020, LF maximum peak of 260 °C


RoHS
COMPLIANT

BENEFITS

- Reduced RFI and EMI
- Reduced power loss in diode and switching transistor
- Higher frequency operation
- Reduced snubbing
- Reduced parts count

DESCRIPTION

These diodes are optimized to reduce losses and EMI/RFI in high frequency power conditioning systems. The softness of the recovery eliminates the need for a snubber in most applications. These devices are ideally suited for freewheeling, flyback, power converters, motor drives, and other applications where high speed and reduced switching losses are design requirements.

PRODUCT SUMMARY	
Package	D-PAK (TO-252AA)
$I_{F(AV)}$	8 A
V_R	600 V
V_F at I_F	1.7 V
t_{rr} typ.	18 ns
T_J max.	150 °C
Diode variation	Single die

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Cathode to anode voltage	V_{RRM}		600	V
Maximum continuous forward current	I_F	$T_C = 100\text{ °C}$	8	A
Single pulse forward current	I_{FSM}		60	
Peak repetitive forward current	I_{FRM}		24	
Maximum power dissipation	P_D	$T_C = 100\text{ °C}$	14	W
Operating junction and storage temperature range	T_J, T_{Stg}		- 55 to + 150	°C

ELECTRICAL SPECIFICATIONS ($T_J = 25\text{ °C}$ unless otherwise specified)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNITS
Breakdown voltage, blocking voltage	V_{BR}, V_R	$I_R = 100\text{ }\mu\text{A}$		600	-	-	V
Forward voltage	V_F	$I_F = 8\text{ A}$	See fig. 1	-	1.4	1.7	
		$I_F = 16\text{ A}$		-	1.7	2.1	
		$I_F = 8\text{ A}, T_J = 125\text{ °C}$		-	1.4	1.7	
Maximum reverse leakage current	I_R	$V_R = V_R$ rated		-	0.3	5.0	μA
		$T_J = 125\text{ °C}, V_R = 0.8 \times V_R$ rated		-	100	500	
Junction capacitance	C_T	$V_R = 200\text{ V}$	See fig. 3	-	10	25	pF
Series inductance	L_S	Measured lead to lead 5 mm from package body		-	8.0	-	nH



DYNAMIC RECOVERY CHARACTERISTICS (T _J = 25 °C unless otherwise specified)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Reverse recovery time	t _{rr}	I _F = 1.0 A, di _F /dt = 200 A/μs, V _R = 30 V	-	18	-	ns
		T _J = 25 °C	-	37	55	
		T _J = 125 °C	-	55	90	
Peak recovery current	I _{RRM}	T _J = 25 °C	-	3.5	5.0	A
		T _J = 125 °C	-	4.5	8.0	
Reverse recovery charge	Q _{rr}	T _J = 25 °C	-	65	138	nC
		T _J = 125 °C	-	124	360	
Rate of fall of recovery current	di _(rec) /dt	T _J = 25 °C	-	240	-	A/μs
		T _J = 125 °C	-	210	-	

THERMAL - MECHANICAL SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Maximum junction and storage temperature range	T _J , T _{Stg}		- 55	-	150	°C
Thermal resistance, junction to case	R _{thJC}		-	-	3.5	°C/W
Thermal resistance, junction to ambient	R _{thJA}	Typical socket mount	-	-	80	
Weight			-	2.0	-	g
			-	0.07	-	oz.
Marking device		Case style D-PAK	HFA08SD60S			

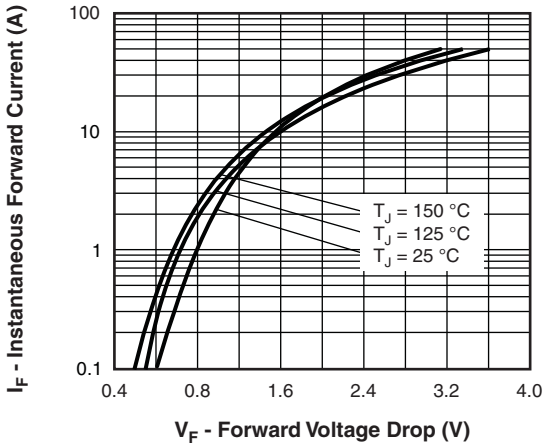


Fig. 1 - Typical Forward Voltage Drop Characteristics

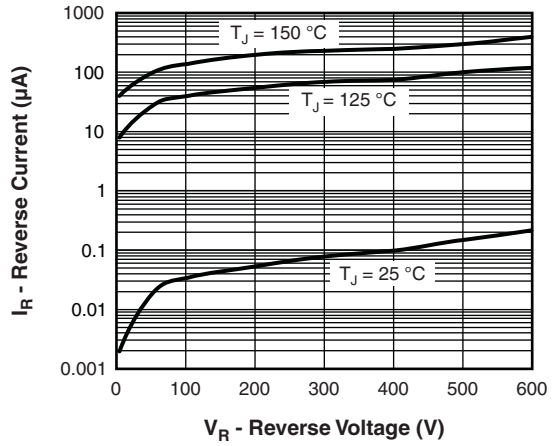


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

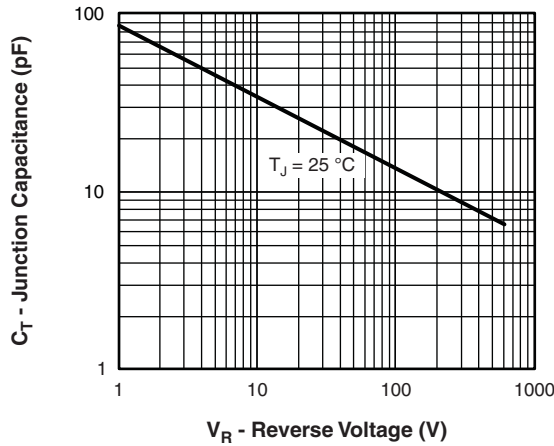


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

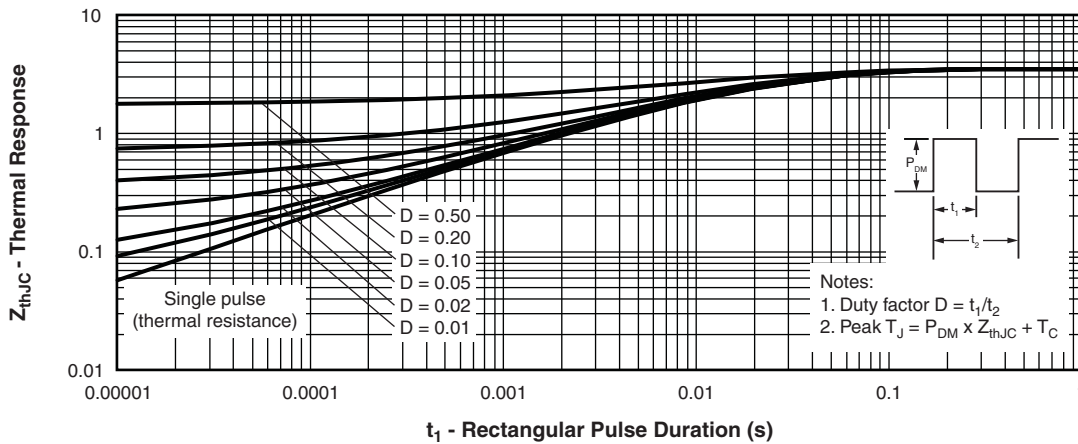


Fig. 4 - Maximum Thermal Impedance Z_{thJC} Characteristics

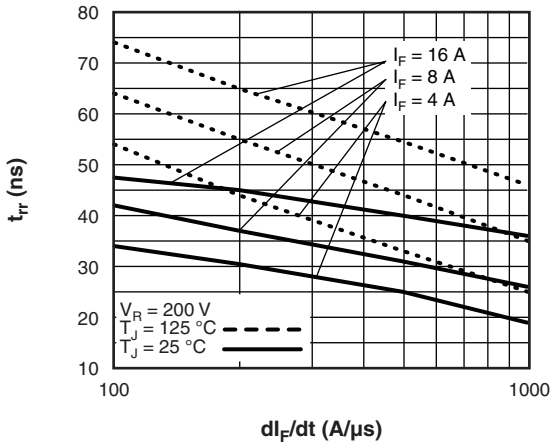


Fig. 5 - Typical Reverse Recovery Time vs. di_F/dt

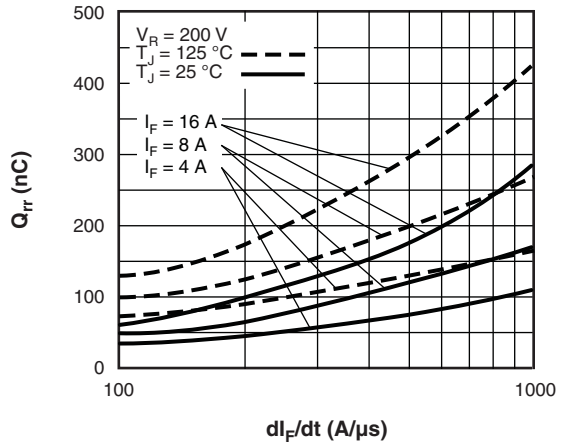


Fig. 7 - Typical Stored Charge vs. di_F/dt

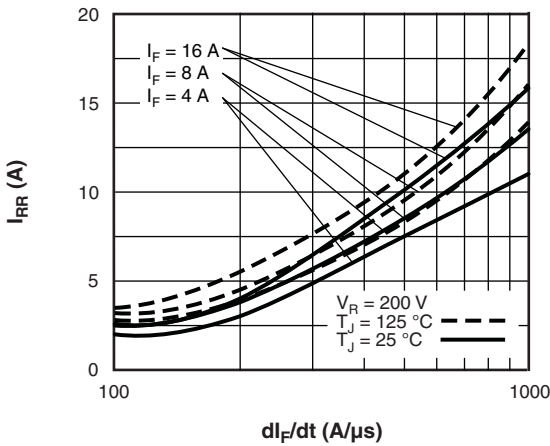


Fig. 6 - Typical Recovery Current vs. di_F/dt

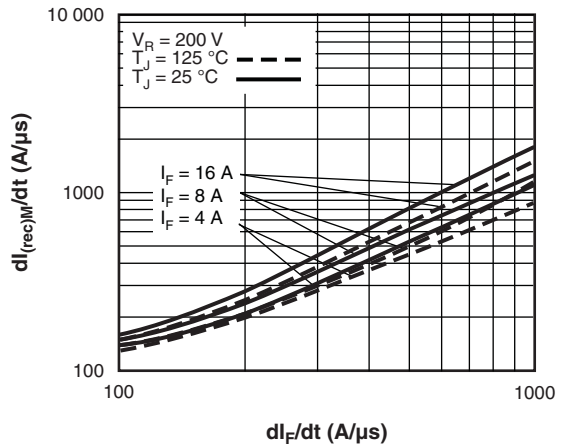


Fig. 8 - Typical $di_{(rec)M}/dt$ vs. di_F/dt

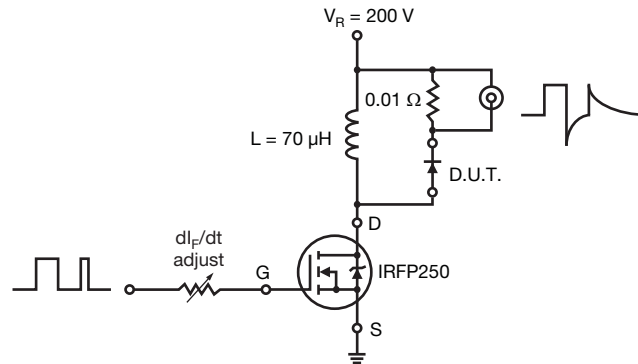
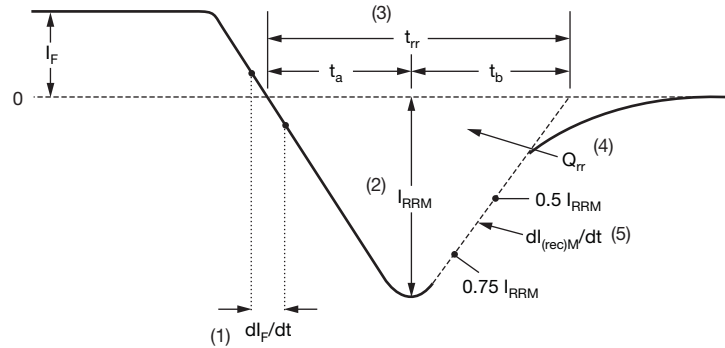


Fig. 9 - Reverse Recovery Parameter Test Circuit

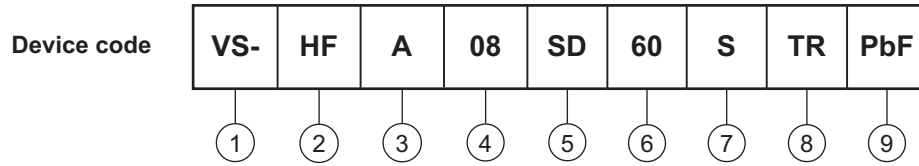


- | | |
|--|--|
| (1) dI_F/dt - rate of change of current through zero crossing | (4) Q_{rr} - area under curve defined by t_{rr} and I_{RRM} |
| (2) I_{RRM} - peak reverse recovery current | $Q_{rr} = \frac{t_{rr} \times I_{RRM}}{2}$ |
| (3) t_{rr} - reverse recovery time measured from zero crossing point of negative going I_F to point where a line passing through $0.75 I_{RRM}$ and $0.50 I_{RRM}$ extrapolated to zero current. | (5) $dI_{(rec)M}/dt$ - peak rate of change of current during t_b portion of t_{rr} |

Fig. 10 - Reverse Recovery Waveform and Definitions



ORDERING INFORMATION TABLE

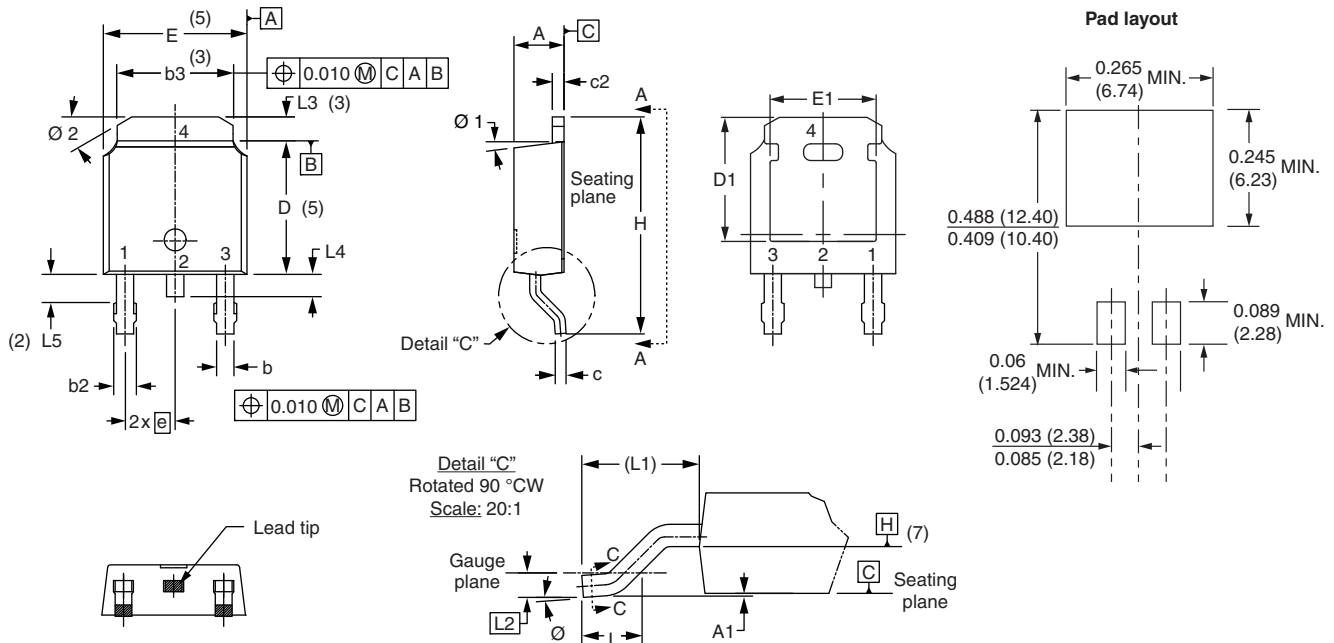


- 1** - Vishay Semiconductors product
- 2** - HEXFRED® family
- 3** - Electron irradiated
- 4** - Current rating (08 = 8 A)
- 5** - D-PAK
- 6** - Voltage rating (60 = 600 V)
- 7** - S = D-PAK
- 8** -
 - TR = Tape and reel
 - TRR = Tape and reel (right oriented)
 - TRL = Tape and reel (left oriented)
- 9** -
 - PbF = Lead (Pb)-free
 - P = Lead (Pb)-free (for TRR and TRL)

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95016
Part marking information	www.vishay.com/doc?95059
Packaging information	www.vishay.com/doc?95033

D-PAK (TO-252AA)

DIMENSIONS in millimeters and inches



SYMBOL	MILLIMETERS		INCHES		NOTES	SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.			MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	0.094		e	2.29 BSC		0.090 BSC		
A1	-	0.13	-	0.005		H	9.40	10.41	0.370	0.410	
b	0.64	0.89	0.025	0.035		L	1.40	1.78	0.055	0.070	
b2	0.76	1.14	0.030	0.045		L1	2.74 BSC		0.108 REF.		
b3	4.95	5.46	0.195	0.215	3	L2	0.51 BSC		0.020 BSC		
c	0.46	0.61	0.018	0.024		L3	0.89	1.27	0.035	0.050	3
c2	0.46	0.89	0.018	0.035		L4	-	1.02	-	0.040	
D	5.97	6.22	0.235	0.245	5	L5	1.14	1.52	0.045	0.060	2
D1	5.21	-	0.205	-	3	Ø	0°	10°	0°	10°	
E	6.35	6.73	0.250	0.265	5	Ø1	0°	15°	0°	15°	
E1	4.32	-	0.170	-	3	Ø2	25°	35°	25°	35°	

Notes

- (1) Dimensioning and tolerancing as per ASME Y14.5M-1994
- (2) Lead dimension uncontrolled in L5
- (3) Dimension D1, E1, L3 and b3 establish a minimum mounting surface for thermal pad
- (4) Section C - C dimension apply to the flat section of the lead between 0.13 and 0.25 mm (0.005 and 0.10") from the lead tip
- (5) Dimension D, and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (6) Dimension b1 and c1 applied to base metal only
- (7) Datum A and B to be determined at datum plane H
- (8) Outline conforms to JEDEC outline TO-252AA



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