

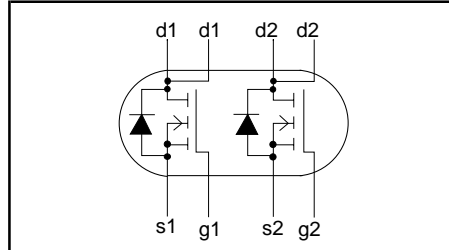
# Dual N-channel enhancement mode TrenchMOS™ transistor

PHN210T

## FEATURES

- Dual device
- Low threshold voltage
- Fast switching
- Logic level compatible
- Surface mount package

## SYMBOL



## QUICK REFERENCE DATA

$V_{DS} = 30\text{ V}$
$I_D = 3.4\text{ A}$
$R_{DS(ON)} \leq 100\text{ m}\Omega$ ( $V_{GS} = 10\text{ V}$ )
$R_{DS(ON)} \leq 200\text{ m}\Omega$ ( $V_{GS} = 4.5\text{ V}$ )

## GENERAL DESCRIPTION

Dual N-channel enhancement mode field-effect transistor in a plastic envelope using 'trench' technology.

### Applications:-

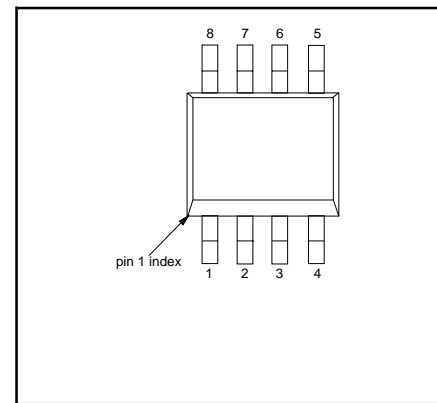
- Motor and relay drivers
- d.c. to d.c. converters
- Logic level translator

The PHN210T is supplied in the SOT96-1 (SO8) surface mounting package.

## PINNING

PIN	DESCRIPTION
1	source 1
2	gate 1
3	source 2
4	gate 2
5,6	drain 2
7,8	drain 1

## SOT96-1



## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	Repetitive peak drain-source voltage	$T_j = 25\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$	-	30	V
$V_{DS}$	Continuous drain-source voltage		-	30	V
$V_{DGR}$	Drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	30	V
$V_{GS}$	Gate-source voltage		-	$\pm 20$	V
$I_D$	Drain current per MOSFET <sup>1</sup>	$T_a = 25\text{ }^\circ\text{C}$	-	3.4	A
		$T_a = 70\text{ }^\circ\text{C}$	-	2.8	A
$I_D$	Drain current per MOSFET (both MOSFETs conducting) <sup>1</sup>	$T_a = 25\text{ }^\circ\text{C}$	-	2.4	A
		$T_a = 70\text{ }^\circ\text{C}$	-	1.9	A
$I_{DM}$	Drain current per MOSFET (pulse peak value)	$T_a = 25\text{ }^\circ\text{C}$	-	14	A
$P_{tot}$	Total power dissipation (either or both MOSFETs conducting) <sup>1</sup>	$T_a = 25\text{ }^\circ\text{C}$	-	2	W
		$T_a = 70\text{ }^\circ\text{C}$	-	1.3	W
$T_{stg}, T_j$	Storage & operating temperature		-65	150	$^\circ\text{C}$

<sup>1</sup> Surface mounted on FR4 board,  $t \leq 10\text{ sec}$

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### THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th(j-a)}$	Thermal resistance junction to ambient	Surface mounted, FR4 board, $t \leq 10$ sec	-	62.5	K/W
$R_{th(j-a)}$	Thermal resistance junction to ambient	Surface mounted, FR4 board	150	-	K/W

### AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$E_{AS}$	Non-repetitive avalanche energy (per MOSFET)	Unclamped inductive load, $I_{AS} = 3.4$ A; $t_p = 0.2$ ms; $T_j$ prior to avalanche = $25^\circ\text{C}$ ; $V_{DD} \leq 15$ V; $R_{GS} = 50 \Omega$ ; $V_{GS} = 10$ V	-	13	mJ
$I_{AS}$	Non-repetitive avalanche current (per MOSFET)		-	3.4	A

### ELECTRICAL CHARACTERISTICS

 $T_j = 25^\circ\text{C}$ , per MOSFET unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0$ V; $I_D = 10 \mu\text{A}$ ; $T_j = -55^\circ\text{C}$	30 27	- -	- -	V V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ ; $I_D = 1$ mA $T_j = 150^\circ\text{C}$ $T_j = -55^\circ\text{C}$	1 0.4 -	2 - 80	2.8 - 100	V V m $\Omega$
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 2.2$ A $V_{GS} = 4.5$ V; $I_D = 1$ A $V_{GS} = 10$ V; $I_D = 2.2$ A; $T_j = 150^\circ\text{C}$	- - -	80 120 -	100 200 170	m $\Omega$ m $\Omega$ m $\Omega$
$g_{fs}$	Forward transconductance	$V_{DS} = 20$ V; $I_D = 2.2$ A	2	4.5	-	S
$I_{D(ON)}$	On-state drain current	$V_{GS} = 10$ V; $V_{DS} = 1$ V; $V_{GS} = 4.5$ V; $V_{DS} = 5$ V	3.5 2	- -	- -	A A
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = 24$ V; $V_{GS} = 0$ V; $V_{DS} = 24$ V; $V_{GS} = 0$ V; $T_j = 150^\circ\text{C}$	- -	10 0.6	100 10	nA $\mu\text{A}$
$I_{GSS}$	Gate source leakage current	$V_{GS} = \pm 20$ V; $V_{DS} = 0$ V	-	10	100	nA
$Q_{g(tot)}$	Total gate charge	$I_D = 2.3$ A; $V_{DD} = 15$ V; $V_{GS} = 10$ V	-	6	-	nC
$Q_{gs}$	Gate-source charge		-	0.7	-	nC
$Q_{gd}$	Gate-drain (Miller) charge		-	0.7	-	nC
$t_{d on}$	Turn-on delay time	$V_{DD} = 20$ V; $R_D = 18 \Omega$ ;	-	6	-	ns
$t_r$	Turn-on rise time	$V_{GS} = 10$ V; $R_G = 6 \Omega$	-	8	-	ns
$t_{d off}$	Turn-off delay time	Resistive load	-	21	-	ns
$t_f$	Turn-off fall time		-	15	-	ns
$L_d$	Internal drain inductance	Measured from drain lead to centre of die	-	2.5	-	nH
$L_s$	Internal source inductance	Measured from source lead to source bond pad	-	5	-	nH
$C_{iss}$	Input capacitance	$V_{GS} = 0$ V; $V_{DS} = 20$ V; $f = 1$ MHz	-	250	-	pF
$C_{oss}$	Output capacitance		-	88	-	pF
$C_{rss}$	Feedback capacitance		-	54	-	pF

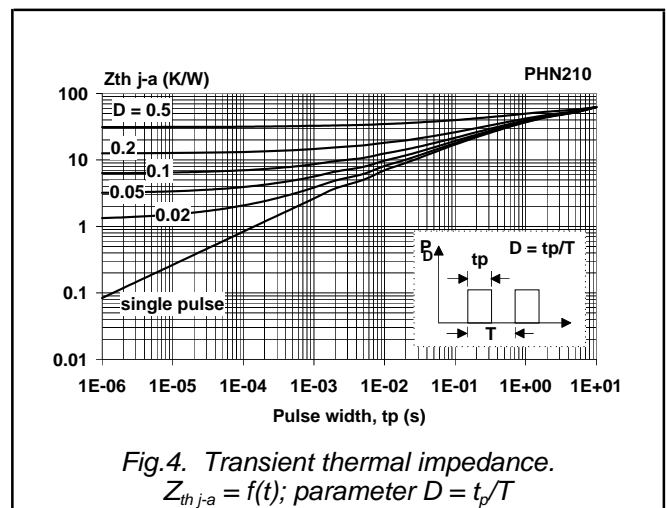
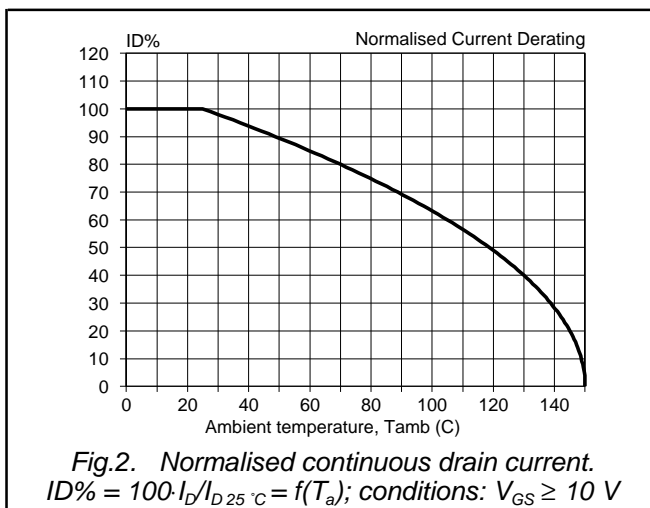
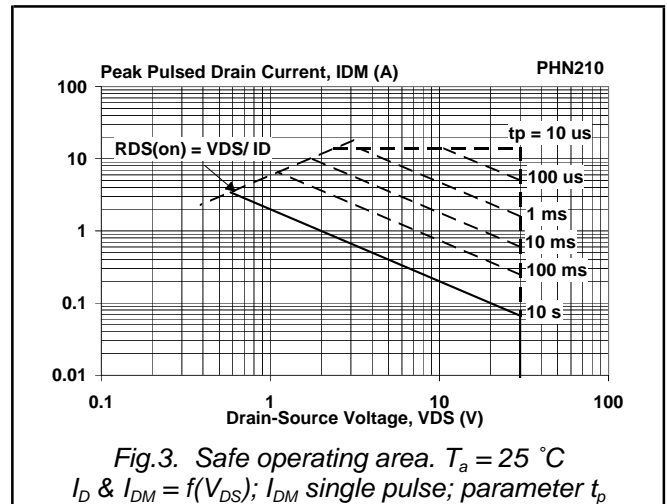
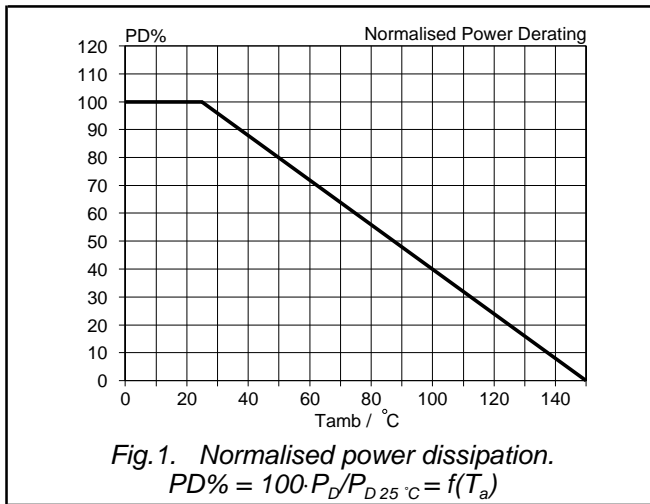
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REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

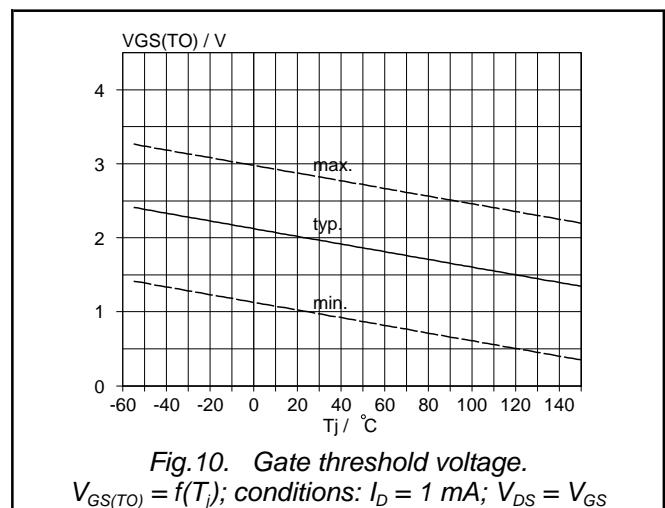
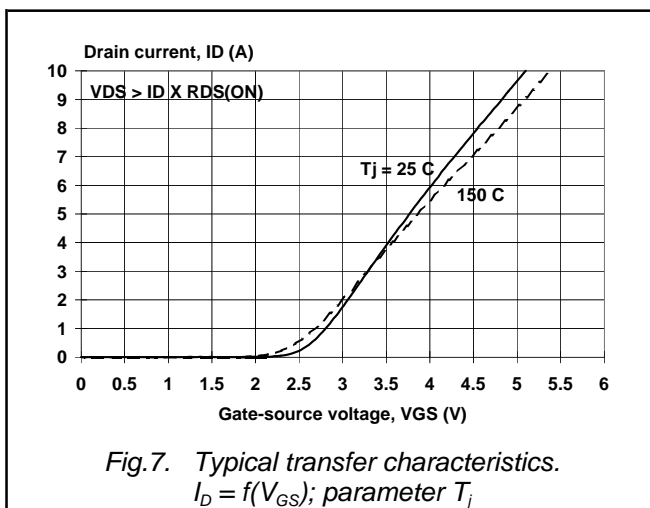
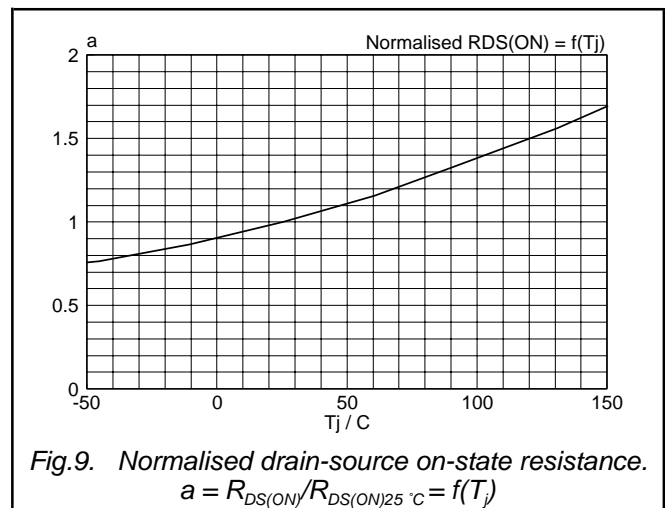
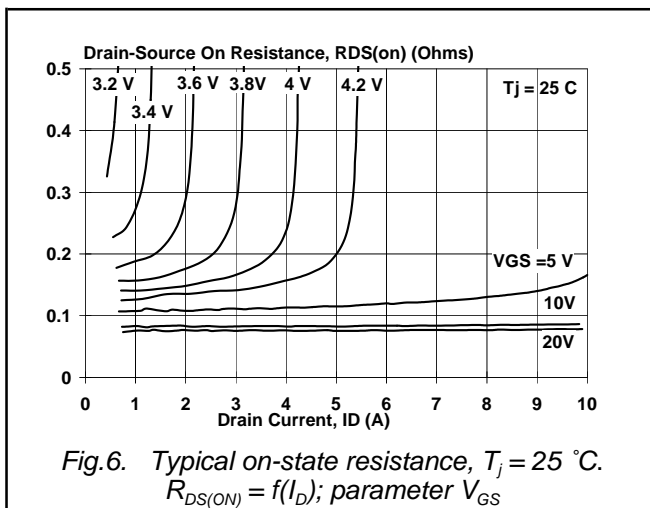
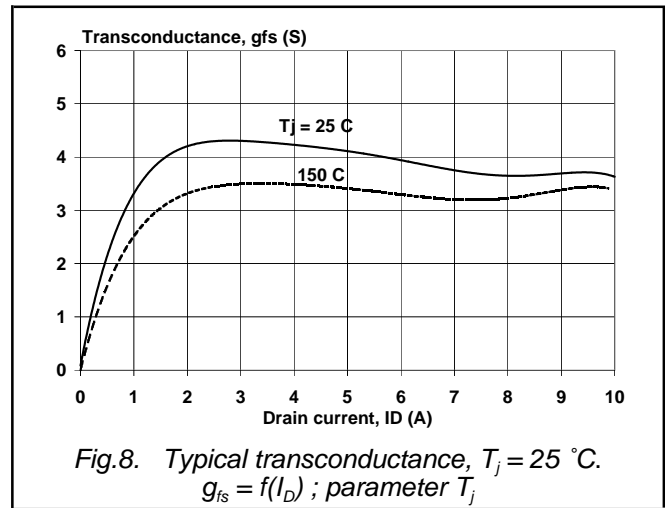
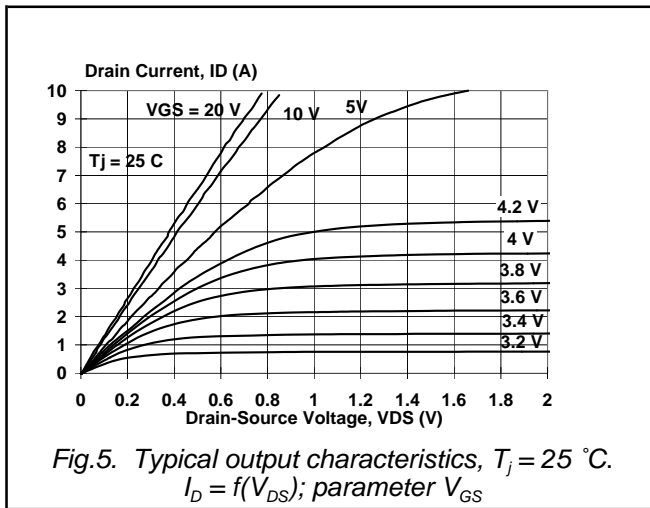
T<sub>j</sub> = 25°C, per MOSFET unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I <sub>S</sub>	Continuous source diode current (per MOSFET)	T <sub>a</sub> = 25 °C	-	-	2.2	A
I <sub>SM</sub>	Pulsed source diode current (per MOSFET)		-	-	14	A
V <sub>SD</sub>	Diode forward voltage	I <sub>F</sub> = 1.25 A; V <sub>GS</sub> = 0 V	-	0.82	1.2	V
t <sub>rr</sub>	Reverse recovery time	I <sub>F</sub> = 1.25 A; -di <sub>F</sub> /dt = 100 A/μs;	-	69	-	ns
Q <sub>rr</sub>	Reverse recovery charge	V <sub>GS</sub> = 0 V; V <sub>R</sub> = 25 V	-	55	-	nC



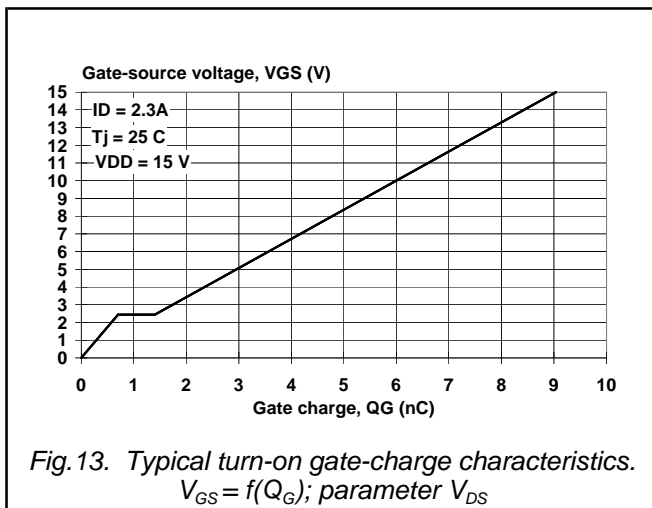
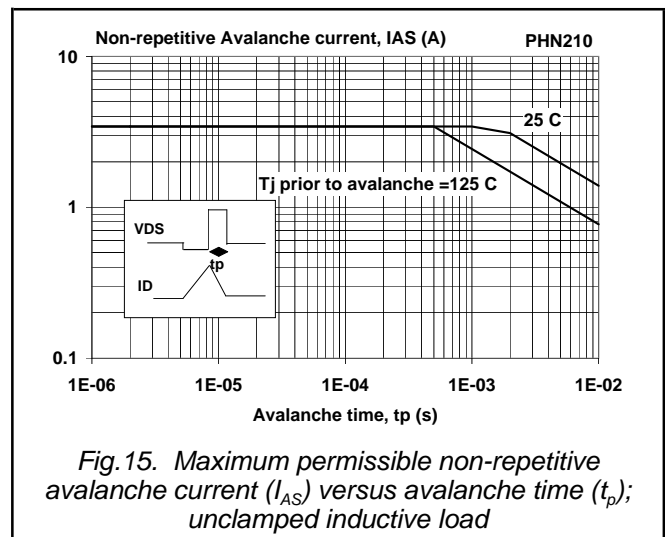
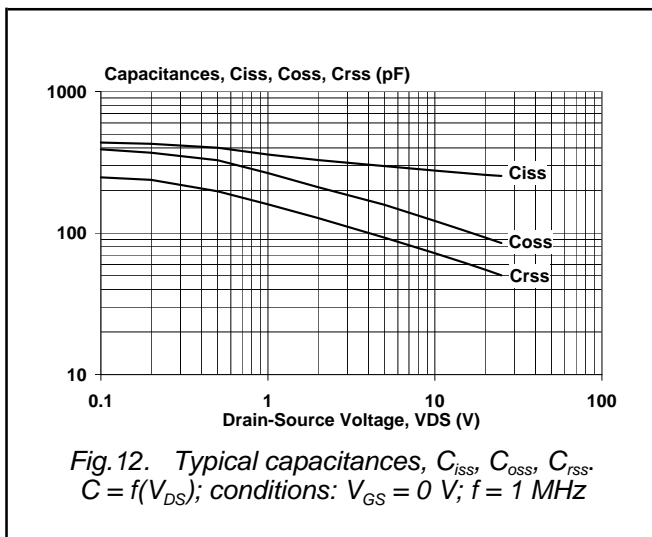
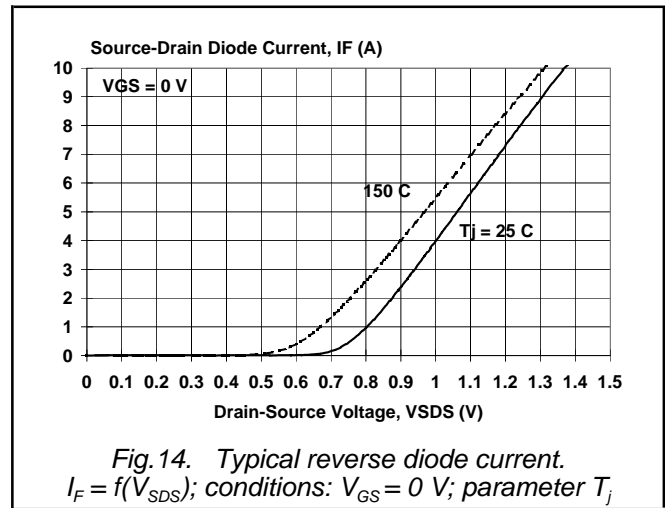
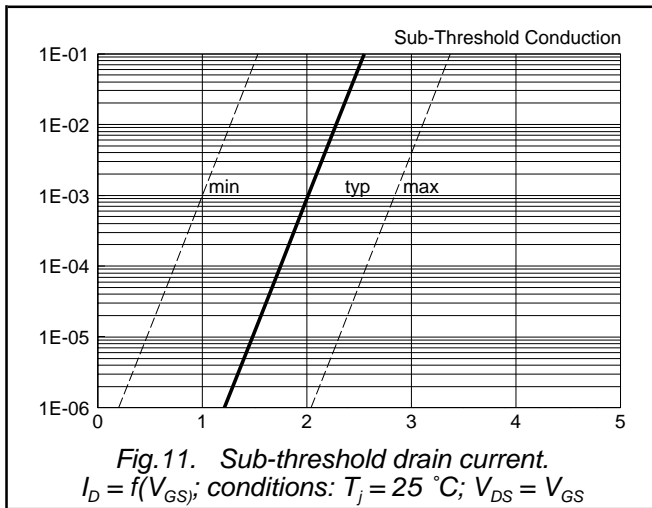
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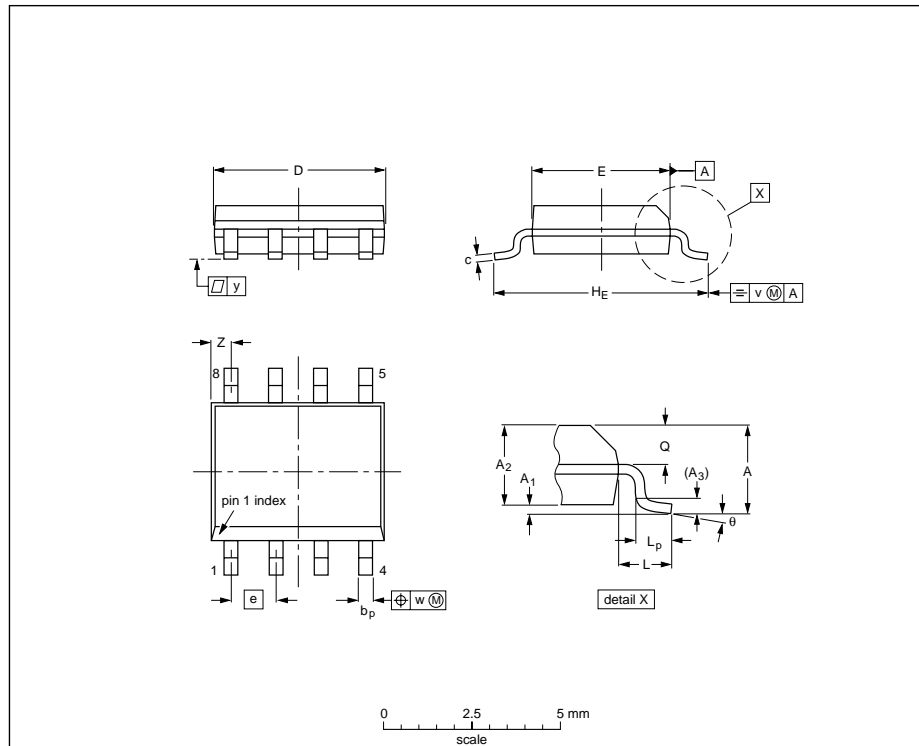
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MECHANICAL DATA

S08: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT96-1	076E03S	MS-012AA			95-02-04 97-05-22

Fig.16. SOT96 surface mounting package.

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to Integrated Circuit Packages, Data Handbook IC26.
3. Epoxy meets UL94 V0 at 1/8".

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### DEFINITIONS

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	
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