SY8600

High Efficiency High Integration PMIC for SSD System

General Description

The SY8600 is a high efficiency PMIC with 5-channel synchronous Buck converters and 2-channel LDOs. It is a single chip total power solution for SSD system.

The output voltage of channel3 and channel4 are controlled by the processor using the I²C interface. It therefore supports DVS (dynamic voltage scaling) function. The SY8600 can generate an open-drain reset output for the processor with certain delay time.

The SY8600 operates over a wide input voltage range from 2.8V to 5.5V. It is available in CSP3.23×3.23-52 package.

Ordering Information

SY8600 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY8600PZC	CSP3.23×3.23-52	----

Features

- 2.8V to 5.5V Input Voltage Range
- Channel 1 Synchronous Buck:
  - Low $R_{DS(ON)}$ for Internal Switches (PFET/NFET): 150/150mΩ
  - 0.6A Maximum Output Current Capability
  - Default Output Voltage:

PORSEL	V_{OUT1}
0	Bypass
1	3.3V

- Channel 2 LDO1:
  - 0.3A Output Current Capability
  - Default Output Voltage V_{OUT2}=1.8V
- Channel 3 Synchronous Buck:
  - Low $R_{DS(ON)}$ for Internal Switches (PFET/NFET): 45/20mΩ
  - 3.0A Maximum Output Current Capability
  - Default Output Voltage V_{OUT3}=0.91V
  - 0.7V to 1.1V Programmable, 10mV Step
- Channel 4 Synchronous Buck:
  - Low $R_{DS(ON)}$ for Internal Switches (PFET/NFET): 35/45mΩ
  - 4.0A Maximum Output Current Capability
  - 2.7V to 3.6V Programmable, 100mV Step
  - Default Output Voltage:

PORSEL	VSEL4	V_{OUT4}
0	0	2.8V
0	1	Bypass
1	0	2.8V
1	1	3.3V

- Channel 5 Synchronous Buck:
  - Low $R_{DS(ON)}$ for Internal Switches (PFET/NFET): 60/40mΩ
  - 2.0A Output Current Capability
  - Default Output Voltage:

VSEL5	V_{OUT5}
0	1.8V
1	1.2V

- Channel 6 LDO2:
  - 0.3A Output Current Capability
  - Default Output Voltage V_{OUT6}=1.8V/2.5V

VSEL6	V_{OUT6}
0	1.8V
1	2.5V

- Channel 7 Synchronous Buck:
  - Low $R_{DS(ON)}$ for Internal Switches (PFET/NFET): 60/40mΩ
  - 2.0A Output Current Capability
  - Default Output Voltage V_{OUT7}=1.2V/1.35V/1.5V

	VSEL7	V_{OUT7}
CH7	0	1.2V
	Floating	1.35V
	1	1.5V

- Reset Input/Output Function
- 2.0MHz Switching Frequency for Buck Converters
- Auto PWM/PFM Mode or Forced PWM Mode Controlled by I²C Interface
- I²C Interface Up to 3.4MHz
- Output Voltage Level of CH3/CH4 Controlled by I²C Interface with DVS Function
- 2 Kinds of Power On Reset Detection Voltage Level Selected by PORSEL Pin
- Dedicated Sleep Mode Controlled by GPIO1/GPIO2, PMRST
- Reliable Protections:
  - Over Voltage Protection (OVP)
  - Over Current Protection (OCP)
  - Short Circuit Protection (SCP)
  - Over Temperature Protection (OTP)
- Compact Package: CSP3.23×3.23-52

Applications

- SSD Power System

Typical Application

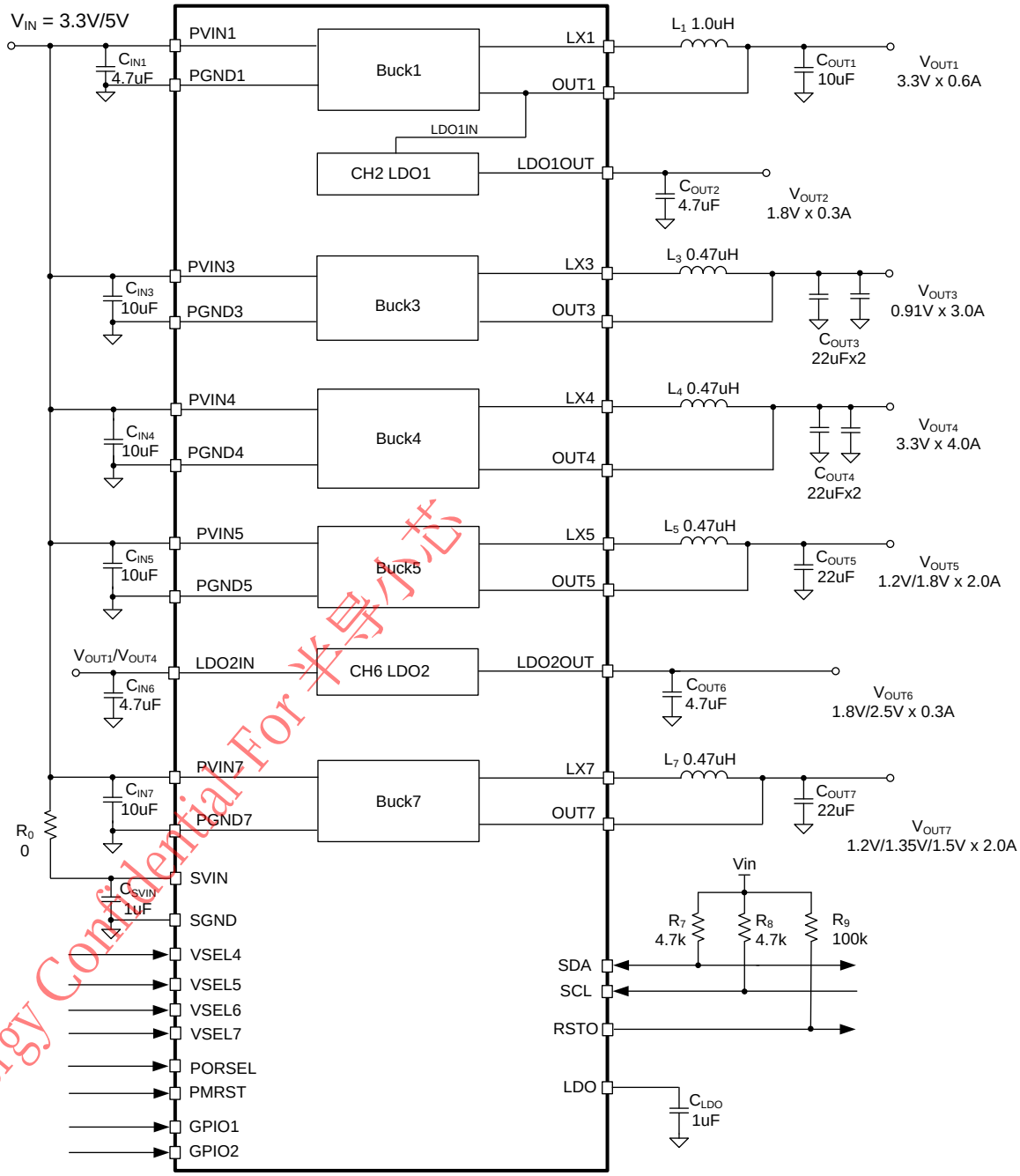
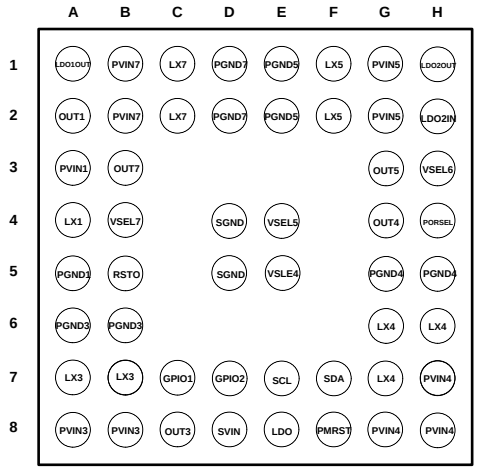


Figure1. Schematic Diagram

Pinout (Top View)



(CSP3.23×3.23-52)

Top Mark: **BWB *xyz*** (Device code: BWB, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
LDO1OUT	A1	CH2 LDO1 power output pin. Decouple this pin to GND with at least a 4.7μF MLCC capacitor.
OUT1	A2	Output feedback pin of Buck1.Connect this pin to VOUT1 to regulate the output voltage.
PVIN1	A3	Power input pin of Buck1. Decouple this pin to PGND1 with a 10μF MLCC capacitor.
LX1	A4	Switching node pin for Buck1. Connect this pin to the switching node of the inductor.
PGND1	A5	Power ground pin of Buck1.
OUT7	B3	Output feedback pin of Buck7.Connect this pin to VOUT7 to regulate the output voltage.
PVIN7	B1,B2	Power input pin of Buck7. Decouple this pin to PGND7 with a 10μF MLCC capacitor.
LX7	C1,C2	Switching node pin for Buck7. Connect this pin to the switching node of the inductor.
PGND7	D1,D2	Power ground pin of Buck7.
PGND5	E1,E2	Power ground pin of Buck5.
LX5	F1,F2	Switching node pin for Buck5. Connect this pin to the switching node of the inductor.
PVIN5	G1,G2	Power input pin of Buck5. Decouple this pin to PGND5 with a10μF MLCC capacitor.
OUT5	G3	Feedback pin of Buck5.Connect this pin to VOUT5 to regulate the output voltage.
LDO2OUT	H1	LDO2 power output pin. Decouple this pin to GND with at least a 4.7μF MLCC capacitor.
LDO2IN	H2	LDO2 power input pin. Decouple this pin to GND with at least a 2.2μF MLCC capacitor.
VSEL6	H3	Channel6 LDO2 default output voltage selection pin.
PORSEL	H4	POR threshold selection pin.
VSEL5	E4	Channel5 default output voltage selection pin.

OUT4	G4	Feedback pin of Buck4.Connect this pin to VOUT4 to regulate the output voltage.
PGND4	G5,H5	Power ground pin of Buck4.
LX4	G6,G7,H6	Switching node pin for Buck4. Connect this pin to the switching node of the inductor.
PVIN4	H7,G8,H8	Power input pin of Buck4. Decouple this pin to PGND4 with a 10μF MLCC capacitor.
SDA	F7	Data line for the I^2C interface. Open drain.
SCL	E7	Clock input for the I^2C interface. Open drain input.
LDO	E8	Internal LDO output pin, decouple this pin to PGND with a 1μF MLCC capacitor.
PMRST	F8	PMIC reset input pin. All of the channels will go back to previous value before when PMRST falling edge is detected. Internally, a 2MΩ resister is integrated to pull low this pin when it is not adopted.
SGND	D4,D5	Signal power ground pin.
VSEL4	E5	Channel4 default output voltage selection pin.
GPIO1	C7	Dedicated Sleep mode control pin1.
GPIO2	D7	Dedicated Sleep mode control pin2.
SVIN	D8	Signal power supply input pin. Decouple this pin to GND with at least a 1μF MLCC capacitor.
OUT3	C8	Output feedback pin of Buck3.Connect this pin to VOUT3 to regulate the output voltage.
PVIN3	A8,B8	Power input pin of Buck3. Decouple this pin to PGND3 with a 10μF MLCC capacitor.
LX3	A7,B7	Switching node pin for Buck3. Connect this pin to the switching node of the inductor.
PGND3	A6,B6	Power ground pin of Buck3.
RSTO	B5	Reset output pin.
VSEL7	B4	Channel7 default output voltage selection pin.

Absolute Maximum Ratings (Note 1)

All Pins ---------- -0.3V to 6.0V

Power Dissipation,

P_D @ T_A = 25℃ CSP3.23×3.23-52 ---------- 5W

Package Thermal Resistance (Note 2)

θ_{JA}, CSP3.23×3.23-52 ---------- 24W/℃

θ_{JC}, CSP3.23×3.23-52 ---------- 1W/℃

Junction Temperature Range ---------- 150℃

Lead Temperature (Soldering, 10 sec.) ---------- 260℃

Storage Temperature Range ---------- -55℃ to 150℃

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 2.8V to 5.5V

Junction Temperature Range ---------- -40℃ to 125℃

Ambient Temperature Range ---------- -40℃ to 85℃

Electrical Characteristics

(V_{IN}=5V, T_A = 25℃, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.8		5.5	V
Input Voltage UVLO Threshold	$V_{UVLO,FALLING}$	PORSEL=0 V_{IN} falling	2.561	2.6	2.639	V
		PORSEL=1 V_{IN} falling	3.546	3.6	3.654	V
Input Voltage UVLO Hysteresis	$V_{UVLO,HYS}$	Hysteresis		100		mV
POR Threshold	$V_{POR,FALLING}$	PORSEL=0 V_{IN} falling	2.561	2.6	2.639	V
		PORSEL=1 V_{IN} falling	3.546	3.6	3.654	V
POR Hysteresis	$V_{POR,HYS}$	Hysteresis		100		mV
System Delay Time From UVLO	t_{SYS}			1		ms
Quiescent Current	I_Q	No load input current, VIN=3.3V		140	170	μA
		No load input current, VIN=5.0V		180	210	μA
VSEL4,VSEL5, VSEL6, VSEL7, PORSEL, PMRST, GPIO1, GPIO2						
Logic Level High	V_{HIGH}		1.2			V
Logic Level Low	V_{LOW}				0.4	V
Power-On Reset(POR)						
POR Deglitch Delay		Vin falling		2		μs
RSTO Output Low Resistance				10		Ω
RSTO Delay Time from UVLO Threshold	$T_{POR,DEL}$	V_{IN}=5V	5.4	6	6.6	ms
I²C COMPATIBLE I/O (SDA,SCL)						
Maximum Operating Frequency	f_{SCL}		3.4			MHz
I²C Supply Voltage				1.8	5.5	V
SDA and SCL Pin Input Logic Thresholds	Logic low				0.5	V
	Logic high		1.2			V
Channel 1 Synchronous Buck Converter						
Output Voltage Default Value	$V_{OUT1,DEF}$	PORSEL=0		Bypass		
		PORSEL=1		3.3		V
Output Voltage Accuracy	ΔV_{OUT1}	PWM mode operation	-1		+1	%
Switching Frequency	F_{OSC1}			2.0		MHz
Main PFET R_{ON}	$R_{DS(ON),P1}$			150		mΩ
Synchronous NFET R_{ON}	$R_{DS(ON),N1}$			150		mΩ
High Side FET Current Limit	I_{LIM1_HS}		1.0			A
Low Side FET Current Limit	I_{LIM1_LS}		0.6			A
Max Output DC Load Current	I_{OUT1}		0.6			A
Internal Softstart Time	t_{SS1}	V_{OUT} rising from 10% to 90%		200		μs
Start-up Default Delay Time	t_{DELAY1}	After system delay		0		ms

Discharge Resistor	R_{DIS1}			10		Ω
SCP Threshold	V_{SCP1}	V_{SCP1}<V_{OUT1}×30%		30		%
SCP Deglitch Time	t_{SCP1}			10		µs
Channel 2 LDO						
Output Voltage Default Value	$V_{LDO1OUT}$			1.8		V
Output Voltage Accuracy	V_{OUT2}	I_{OUT2}=10mA	-1		+1	%
Current Limit	I_{LIM2}		0.35			A
Max Output DC Load Current	I_{OUT2}		0.3			A
Dropout Voltage		I_{OUT2}=0.3A			300	mV
Internal Softstart Time	t_{SS2}	V_{OUT} rising from 10% to 90%		200		µs
Start-up Default Delay Time	t_{DELAY2}	After system delay		0.5		ms
Discharge Resistor	R_{DIS2}			10		Ω
SCP Threshold	V_{SCP2}	V_{SCP2}<V_{OUT2}x60%		60		%
SCP Deglitch Time	t_{SCP2}			100		µs
Channel 3 Synchronous Buck Converter						
Output Voltage Default Value	$V_{OUT3,DEF}$			0.91		V
DVS Voltage Step	$V_{OUT3,DVS,STEP}$	Controllable by I²C interface		10		mV
DVS Voltage Range	$V_{OUT3,DVS}$	Controllable by I²C interface	0.7		1.1	mV
Output Voltage Accuracy	ΔV_{OUT3}	PWM mode operation	-1		+1	%
Switching Frequency	F_{OSC3}			2.0		MHz
Main PFET R_{ON}	$R_{DS(ON),P3}$			45		mΩ
Synchronous NFET R_{ON}	$R_{DS(ON),N3}$			20		mΩ
High Side FET Current Limit	I_{LIM3_HS}		4.0			A
Low Side FET Current Limit	I_{LIM3_LS}		3.0			A
Max Output DC Load Current	I_{OUT3}		3.0			A
Internal Softstart Time	t_{SS3}	V_{OUT} rising from 10% to 90%		200		µs
Start-up Default Delay Time	t_{DELAY3}	After system delay		1		ms
Discharge Resistor	R_{DIS3}			10		Ω
SCP Threshold	V_{SCP3}	V_{SCP3}<V_{OUT3}x30%		30		%
SCP Deglitch Time	t_{SCP3}			10		µs
Channel 4 Synchronous Buck Converter						
Output Voltage Default Value	$V_{OUT4,DEF}$	PORSEL=0 VSEL4=0		2.8		V
		PORSEL=0 VSEL4=1		Bypass		
		PORSEL=1 VSEL4=0		2.8		
		PORSEL=1 VSEL4=1		3.3		
DVS Voltage Step	$V_{OUT4,DVS,STEP}$	Controllable by I²C interface		100		mV
DVS Voltage Range	$V_{OUT4,DVS}$	Controllable by I²C interface	2.7		3.6	V
Output Voltage Accuracy	ΔV_{OUT4}	PWM mode operation	-1		+1	%
Switching Frequency	F_{OSC4}			2.0		MHz
Main PFET R_{ON}	$R_{DS(ON),P4}$			35		mΩ
Synchronous NFET R_{ON}	$R_{DS(ON),N4}$			45		mΩ
High Side FET Current Limit	I_{LIM4_HS}		5.0			A

Low Side FET Current Limit	I_{LIM4_LS}		4.0			A
Max Output DC Load Current	I_{OUT4}		4.0			A
Internal Softstart Time	t_{SS4}	V_{OUT} rising from 10% to 90%		200		us
Start-up Default Delay Time	t_{DELAY4}			1.5		ms
Discharge Resistor	R_{DIS4}			10		Ω
SCP Threshold	V_{SCP41}	V_{SCP4}<V_{OUT4}x30%		30		%
SCP Deglitch Time	t_{SCP4}			10		µs
Channel 5 Synchronous Buck Converter						
Output Voltage Default Value	$V_{OUT5,DEF}$	VSEL5=0		1.8		V
		VSEL5=1		1.2		
Output Voltage Accuracy	ΔV_{OUT5}	PWM mode operation	-1		+1	%
Switching Frequency	F_{OSC5}			2.0		MHz
Main PFET R_{ON}	$R_{DS(ON),P5}$			60		mΩ
Synchronous NFET R_{ON}	$R_{DS(ON),N5}$			40		mΩ
High Side FET Current Limit	I_{LIM5_HS}		3.0			A
Low Side FET Current Limit	I_{LIM5_LS}		2.0			A
Max Output DC Load Current	I_{OUT5}		2.0			A
Internal Softstart Time	t_{SS5}	V_{OUT} rising from 10% to 90%		200		µs
Start-up Default Delay Time	t_{DELAY5}	After system delay		2		ms
Discharge Resistor	R_{DIS5}			10		Ω
SCP Threshold	V_{SCP5}	V_{SCP5}<V_{OUT5}×30%		30		%
SCP Deglitch Time	t_{SCP5}			10		µs
Channel 6 LDO						
LDO Input Voltage Range	$V_{IN,LDO}$		2.8	3.3	5.5	V
Output Voltage Default Value	$V_{OUT6,DEF}$	VSEL6=0		1.8		V
		VSEL6=1		2.5		
Output Voltage Accuracy	V_{OUT6}	I_{OUT6}=10mA	-1%		+1%	
Current Limit	I_{LIM6}		0.35			A
Max Output DC Load Current	I_{OUT6}		0.3			A
Dropout Voltage		I_{OUT6}=0.3A			300	mV
Internal Softstart Time	t_{SS6}	V_{OUT} rising from 10% to 90%		200		µs
Start-up Default Delay Time	t_{DELAY6}	After system delay		2.5		ms
Discharge Resistor	R_{DIS6}			10		Ω
SCP Threshold	V_{SCP6}	V_{SCP6}<V_{OUT6}×60%		60		%
SCP Deglitch Time	t_{SCP6}			100		µs
Channel 7 Synchronous Buck Converter						
Output Voltage Default Value	$V_{OUT7,DEF}$	VSEL7=0		1.2		V
		VSEL7=floating		1.35		
		VSEL7=1		1.5		
Output Voltage Accuracy	ΔV_{OUT7}	PWM mode operation	-1		+1	%
Switching Frequency	F_{OSC5}			2.0		MHz
Main PFET R_{ON}	$R_{DS(ON),P7}$			60		mΩ
Synchronous NFET R_{ON}	$R_{DS(ON),N7}$			40		mΩ

High Side FET Current Limit	I_{LIM7_HS}		3.0			A
Low Side FET Current Limit	I_{LIM7_LS}		2.0			A
Max Output DC Load Current	I_{OUT7}		2.0			A
Internal Softstart Time	t_{SS7}	V_{OUT} rising from 10% to 90%		200		μs
Start-up Default Delay Time	t_{DELAY7}	After system delay		3		ms
Discharge Resistor	R_{DIS7}			10		Ω
SCP Threshold	V_{SCP7}	V_{SCP7}<V_{OUT7}×30%		30		%
SCP Deglitch Time	t_{SCP7}			10		μs
Protection						
Thermal Shudown Threshold	T_{SD}			155		℃
Thermal Shutdown Hysteresis				20		℃
External VIN OVP Protection Threshold		V_{IN} rising, PORSEL=0	3.7	3.85	4	V
		V_{IN} rising, PORSEL=1	5.75	6.0	6.25	
Input OVP Hysteresis		V_{IN} falling		0.15		V
External V_{IN} OVP Deglitch Time				5		μs

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25℃ on a four-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Description

1. Targeted Output Voltage

		Default Output Voltage(V)			Out Voltage Range(V)	DVS Step (mV)	$R_{DS(ON)}$ (mΩ)		I_{OUT} MAX (A)	Power On Delay Time (ms)	SS Time (μs)
							High Side	Low Side			
CH1	Buck	PORSEL=0	Bypass		Bypass	-	150	150	0.6	0	200
		PORSEL=1	3.3V		-	-					
CH2	LDO	1.8			-	-	-	-	0.3	0.5	200
CH3	Buck	0.91			0.7~1.1	10	45	20	3	1	200
CH4	Buck	PORSEL	VSEL4	V_{OUT4}		100	35	45	4	1.5	200
		0	0	2.8V	2.7~3.6						
		0	1	Bypass	-						
		1	0	2.8V	2.7~3.6						
		1	1	3.3V	2.7~3.6						
CH5	Buck	VSEL5	VSEL6	V_{OUT5}	-	-	60	40	2	2	200
		0	X	1.8V							
		1	X	1.2V							
CH6	LDO	VSEL5	VSEL6	V_{OUT6}	-	-	-	-	0.3	2.5	200
		X	0	1.8V							
		X	1	2.5V							
CH7	Buck	VSEL7	V_{OUT7}		-	-	60	40	2	3.0	200
		0	1.2V								
		Floating	1.35V								
		1	1.5V								

2. POR Threshold and RSTO Delay

POR threshold selection:

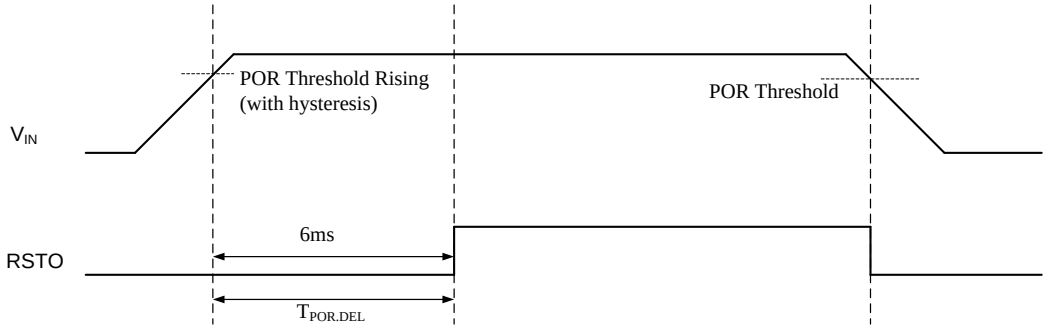
PORSEL pin is pulled low to select the default 2.6V threshold voltage for 3.3V input application;

PORSEL pin is pulled high to select the default 3.6V threshold voltage for 5.0V input application;

	Default Falling Detection Threshold
PORSEL=0	2.6V
PORSEL =1	3.6V

POR sequence:

When V_{IN} exceeds the threshold voltage, RSTO will provide a high-level output signal after a fixed 6ms delay time $t_{POR,DEL}$.



3. VIN Power-on / Power-off Sequence for DDR3/DDR3L(CH6 is Floating)

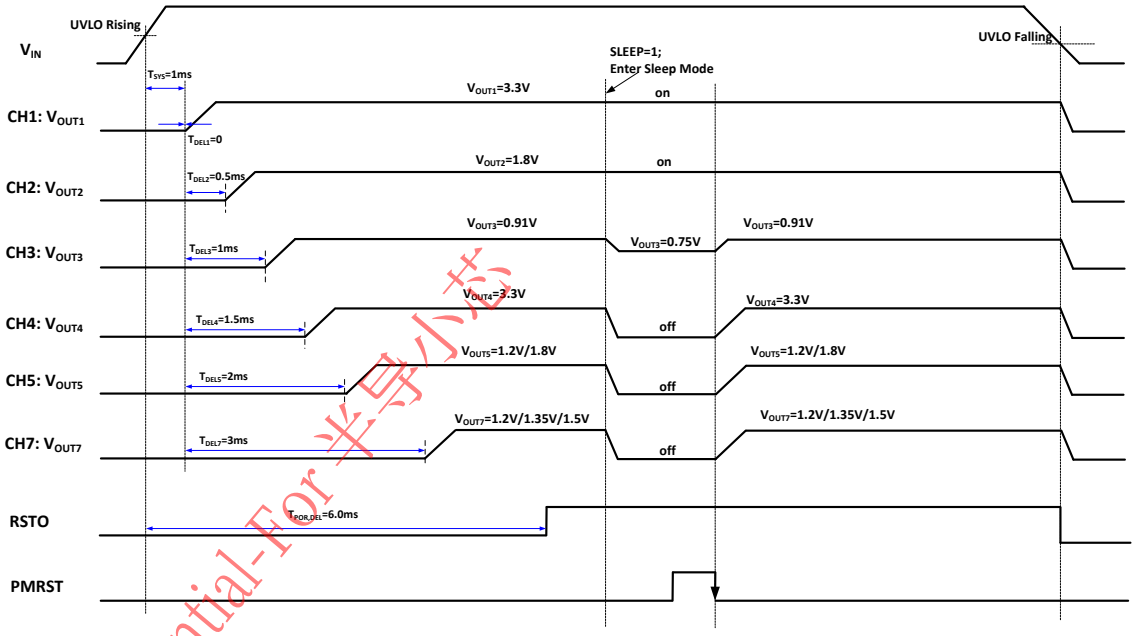


Figure2. V_{IN} Power On/Off Sequence

1. In DDR3/DDR3L model, CH6 is not used, and the input pin LDO2IN is floating, then CH6 will be disabled internally after V_{IN} power on.
2. When input voltage V_{IN} exceeds input UVLO rising threshold, after system delay t_{SYS}=1ms, each channel will power on with fixed delay time t_{DELn}.
3. When Vin exceeds input UVLO threshold, RSTO will provide a high-level output signal after fixed delay time $t_{POR,DEL}$=6ms.
4. The SY8600 could enter sleep mode to save power consumption, in sleep mode each channel can be turned off or keep alive and Ch3/Ch4 output voltage can be adjusted in sleep mode.
5. All channels would go back to previous value before sleep mode at same time when PMRST falling edge is detected.
6. Power off stage: All channels will be turned off immediately if external V_{IN} is lower than UVLO falling threshold. The discharge resister is turned on at power off stage if the corresponding discharge register bit is set to 1.

4. V_{IN} Power-on / Power-off Sequence for LPDDR3/DDR4:

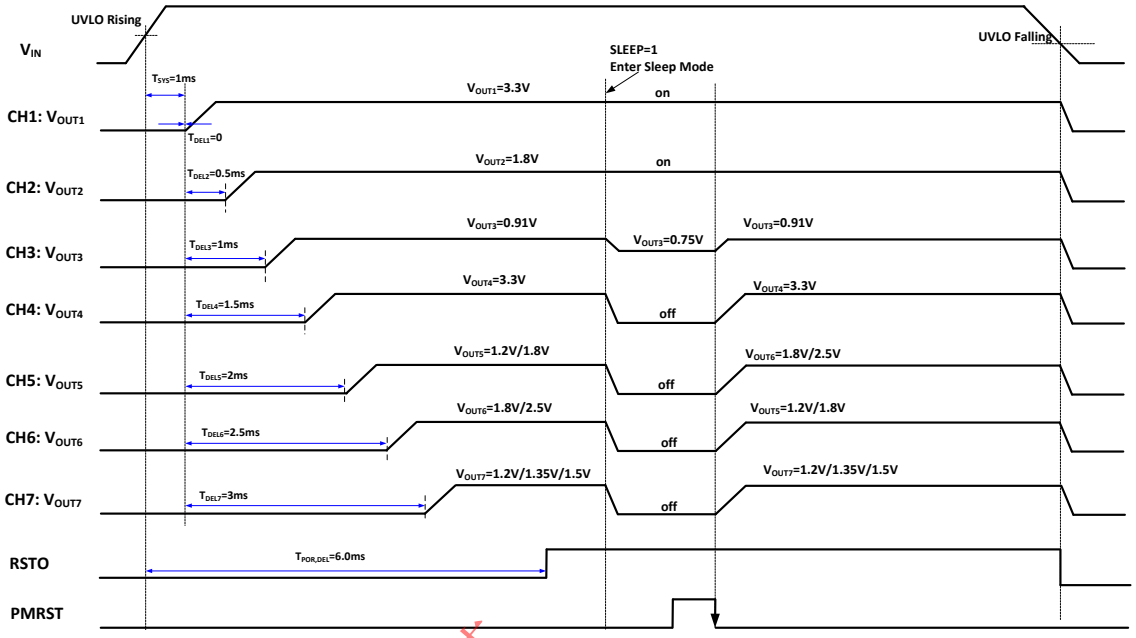


Figure3. V_{IN} Power On/Off Sequence

1. When input voltage V_{IN} exceeds input UVLO rising threshold, after system delay t_{SYS}=1ms, each channel will power on with fixed delay time T_{DELn}.
2. When V_{IN} exceeds input UVLO threshold, RSTO will provide a high-level output signal after fixed delay time $t_{DEL,RSTO}$=6ms.
3. The SY8600 could enter sleep mode to save power consumption, in sleep mode each channel can be turned off or keep alive and Ch3/Ch4 output voltage can be adjusted in sleep mode.
4. All channels would go back to previous value before sleep mode at same time when PMRST falling edge is detected.
5. Power off stage: All channels will be turned off immediately if external V_{IN} is lower than UVLO falling threshold. The discharge resister is turned on at power off stage if the corresponding discharge register bit is set to 1.

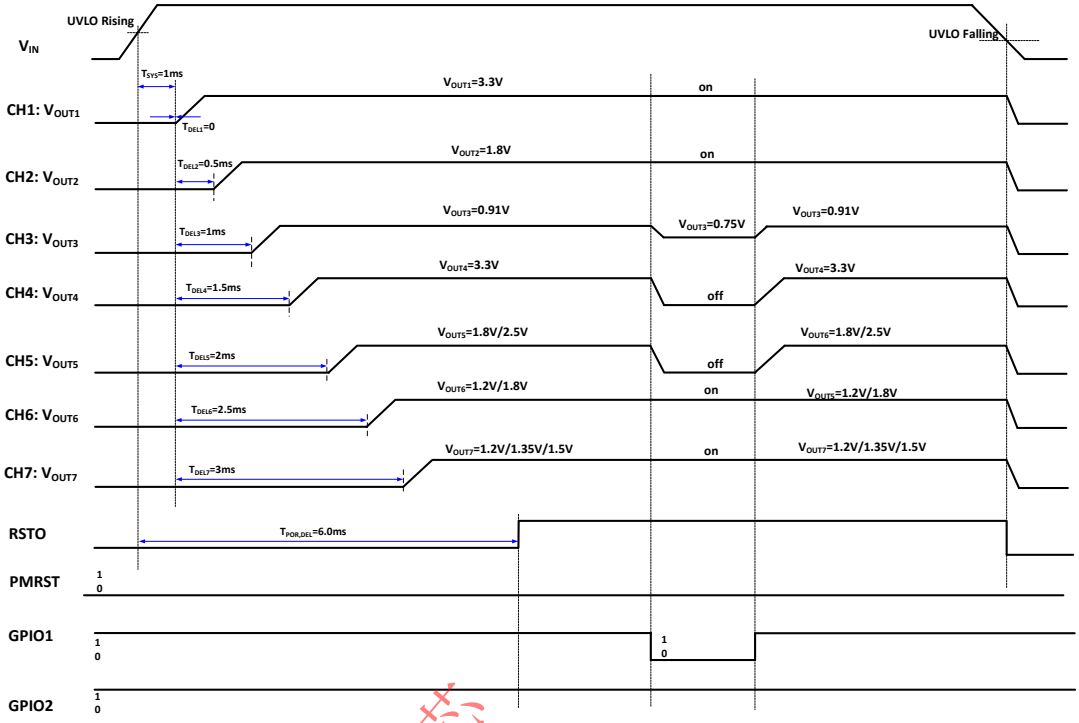
5. SLEEP Mode Controlled by GPIO1/GPIO2

GPIO1 and GPIO2 can be used for making PMIC enter dedicated sleep mode as below: GPIO1 and GPIO2 are effective after RSTO are turned high level.

	GPIO1	GPIO2	Channel on/off state
Normal MODE	1	X	ON/OFF controlled by I^2C
Low Power Mode1(PS3.5)	0	1	CH4/CH5 OFF, other channels ON, CH3: 0.91V-->0.75V
Low Power Mode2(PS4.0)	0	0	CH4/CH5/CH6/CH7 OFF, other channels ON, CH3: 0.91V -->0.75V

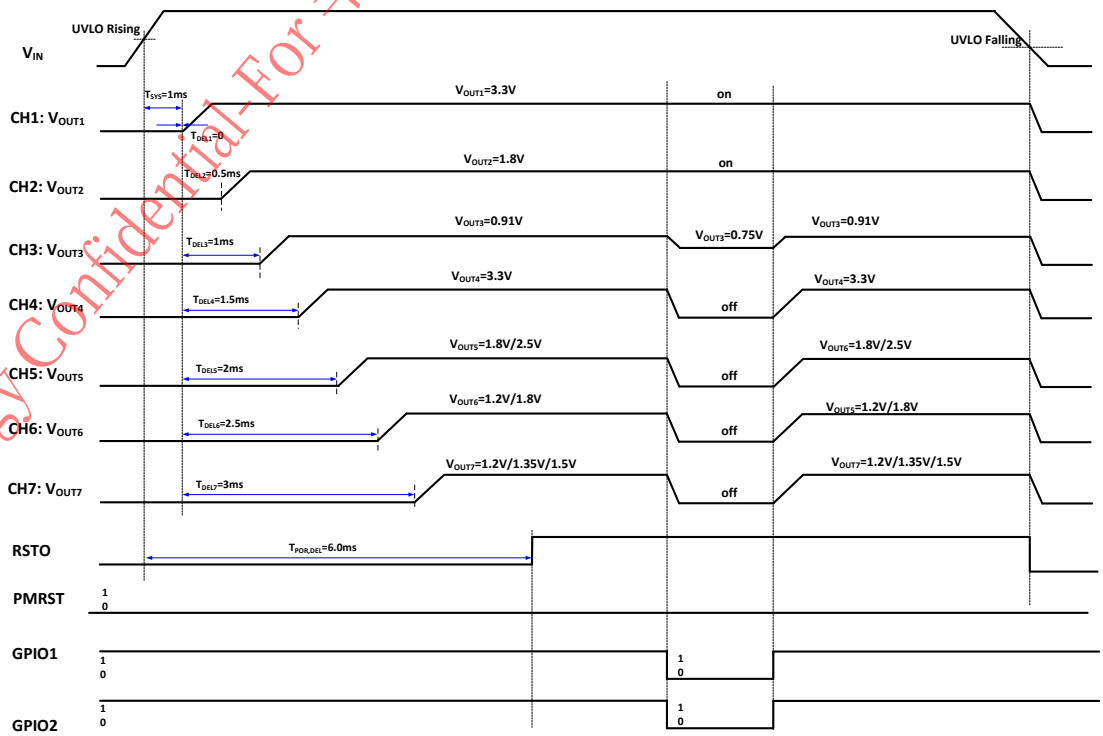
Case 1: Low Power Mode1 (PS3.5)

When GPIO2 keeps high level and GPIO1 is pulled low, PMIC enters Low Power Mode1(PS3.5), all channels keep ON and Ch3 output voltage changes to 0.75V.



Case 2: Low Power Mode2 (PS4.0)

When GPIO1 and GPIO2 are pulled low at same time, PMIC will enter Low Power Mode2(PS4.0), CH4/CH5/CH6/CH7 are turned off and CH3 output voltage changes to 0.75V. When GPIO1 and GPIO2 are pulled high at same time, PMIC exist sleep mode and CH4/CH5/CH6/CH7 are turned on at same time.



6. Default Output Voltage selection

CH1 output voltage selection:

	Default Output Voltage(V)		Output Voltage Range(V)	Note
CH1	PORSEL=0	Bypass	Bypass	PORSEL=0, select $3.3V_{IN}$ model system
	PORSEL=1	3.3	-	PORSEL=1, select $5V_{IN}$ model system

CH4 output voltage selection:

CH4	Default Output Voltage(V)			Output Voltage Range(V)	DVS Step(mV)	Note
	PORSEL	VSEL4	V_{OUT4}			
	0	0	2.8V	2.7V~3.6V	100mV	PORSEL=0, select 3.3Vin model system
	0	1	Bypass	-	-	
	1	0	2.8V	2.7V~3.6V	100mV	PORSEL=1, select 5Vin model system
	1	1	3.3V	2.7V~3.6V	100mV	

In CH4 Bypass mode, the inductor should be removed to avoid the voltage drop.

CH5 output voltage selection:

CH5	VSEL5	V_{OUT5}
	0	1.8V
	1	1.2V

CH6 output voltage selection:

CH6	VSEL6	V_{OUT6}
	0	1.8V
	1	2.5V

CH7 output voltage selection:

Connect VSEL7 pin to GND directly to set VSEL7=0 and set V_{OUT7}=1.2V;

Connect VSEL7 pin to V_{IN} directly to set VSEL7=1 and set V_{OUT7}=1.5V;

Else leave VSEL7 pin floating to set VSEL7=floating and set V_{OUT7}=1.35V.

CH7	VSEL7	V_{OUT7}
	0	1.2V
	Floating	1.35V
	1	1.5V

7. Protection Function

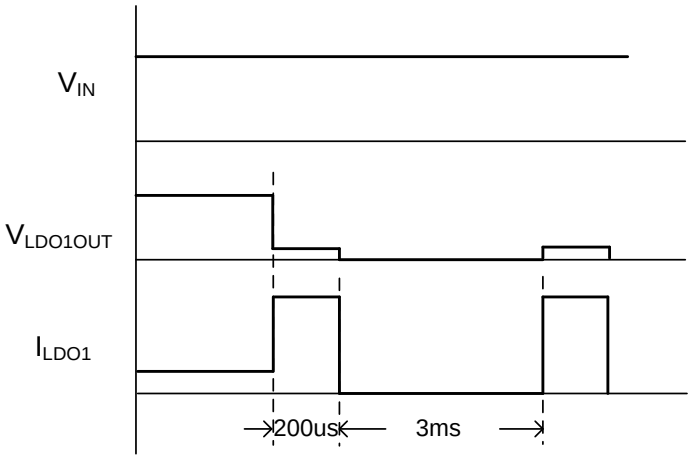
7.1. Buck and LDO Under Voltage Protection and Hard Short Protection:

All of the buck channel and LDO work in hic-cup and auto retry mode in hard short protection mode.

LDO1, LDO2 will internally counter 200μs when hard short condition happens, if hard short condition lasts longer

than 200μs, the related channel will turn off for 3ms to avoid the thermal increase, and start again.

LDO1, LDO2 hard short condition will not affect other channels normal operation.



7.2. V_{IN} Over Voltage Protection:

If input voltage exceeds the input OVP threshold 6.0V when PORSEL=1 or 3.85V when PORSEL=0, over voltage protection will be triggered and then all of the channels will be turned off. And if V_{IN} falls below the threshold, it could exit protection status and all channels start up again with pre-defined delay time.

7.3. Over Temperature Protection:

If the temperature of the junction exceeds 155 ℃, SY8600 will turn off all of the channels. And when junction temp falls below the threshold, it could exit protection status and all channels start up again with pre-defined delay time.

PMIC protection table:

	Threshold	Action
DC/DC SCP	30%	Auto-retry
Input OVP	PORSEL=1, 6.0V	Whole chip turn off and recover when Vin falls below OVP threshold.
	PORSEL=0, 3.85V	
Thermal Shut Down	155 degree	Whole chip turn off and recover when Vin falls below OTP threshold.

I²C Compatible Interface

The SY8600 features an I²C interface that allows the HOST processor to control the output voltage level of all channels to achieve the DVS function. The I²C interface supports clock speeds of up to 3.4MHz and uses standard I²C commands. The SY8600 always operates as a slave device, and is addressed using a 7-bit slave address followed by an 8th bit, which indicates whether the transaction is a read-operation or a write-operation.

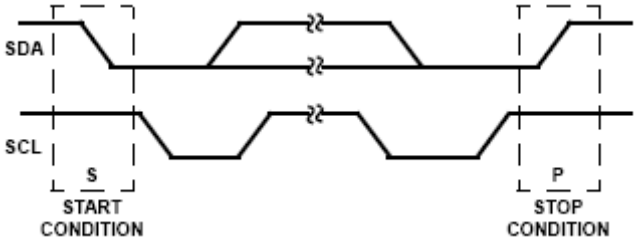
The I²C address of the SY8600 consists of 8-bit data, and the LSB determines the read or write mode, and LSB=0 indicates Write mode and LSB=1 indicates Read mode.

The SY8600 Slave address is as below table:

Binary	Hex	Read/Write
0110 0000	0x60	Write
0110 0001	0x61	Read

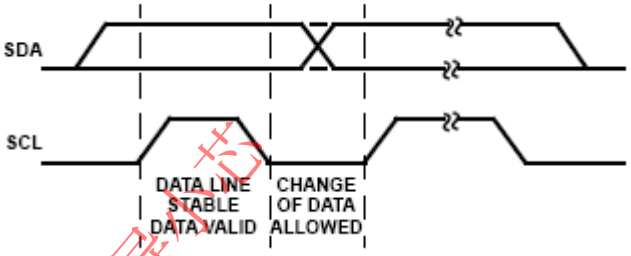
START and STOP Conditions:

The SY8600 is controlled via an I²C compatible interface. The START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition. The I²C master always generates the START and STOP conditions.



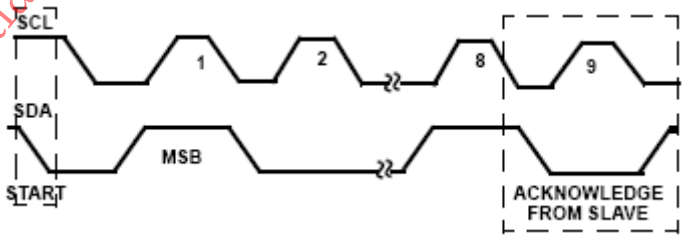
Data Validity:

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.



Acknowledge:

Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the master sends 7-slave address bits and an R/$\overline{W}$ bit during the next 8-clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.

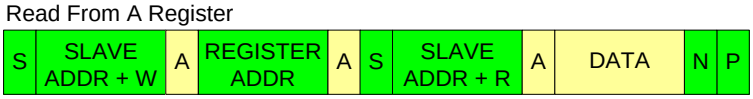


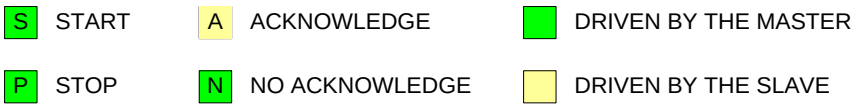
Data Transactions:

All transactions start with a control byte sent from the I²C master device. The control byte begins with a START condition, followed by 7-bits of slave address (0110000x) for the SY8600, this address can be changed if necessary) followed by the 8th bit, R/$\overline{W}$ bit. The R/$\overline{W}$ bit is 0 for a write or 1 for a read. If any slave devices on the I²C BUS recognize their address, they will acknowledge by pulling the SDA line low for the last clock cycle in the control byte. If no slaves exist at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition. Once the control byte is sent, and the SY8600 acknowledges it, the 2nd byte sent by the master must be a register address byte. The register address byte tells the SY8600 which register the master will write or read. Once the SY8600 receives a register address byte it will respond with an Acknowledge.

Write To A Register

Read From A Register





Register Map Summary:

Register Address	Register name	Default Description	Default Value (HEX)	Register Description
0x01	OUT3_SET	0.91V	0x15	Voltage setting for Buck Channel3
0x02	OUT4_SET	2.8V/3.3V	0x01 or 0x06	Voltage setting for Buck Channel4
0x03	Enable_REG	All channels ON	0x3F	Channel Enable/Disabled
0x04	Discharge_REG	Discharge ON	0x3F	Channel Discharge Enable/Disabled
0x05	Mode_REG	Auto PWM/PFM	0x1F	Auto PWM/PFM mode or forced PWM mode control
0x06	SLP_OUT3_SET	0.75V	0x05	Sleep mode Voltage setting for Buck Channel3
0x07	SLP_OUT4_SET	2.8V/3.3V	0x01 or 0x06	Sleep mode Voltage setting for Buck Channel4
0x08	SLP_Enable_REG	CH1/CH2/CH3 ON, other channels OFF.	0x07	Sleep mode Channel Enable/Disabled, and Sleep mode control.

Register Settings:

1. Channel3 Output Voltage Setting Register (0x01)

This register set Channel3 output voltage. $V_{OUT3\_DEFAULT}$=0.91V

Register Name	OUT3_REG			Output voltage setting register for channel 3			
Address				0x01			
Field	Bit	R/W	Default	Output voltage setting for OUT3. DVS from 0.7V to 1.1V in 10mV steps.			
VOUT3_SET	5:0	R/W	Default 0x15=0.91V	0x00=0.70V	0x01=0.71V	0x02=0.72V	0x03=0.73V
				0x04=0.74V	0x05=0.75V	0x06=0.76V	0x07=0.77V
				0x08=0.78V	0x09=0.79V	0x0A=0.80V	0x0B=0.81V
				0x0C=0.82V	0x0D=0.83V	0x0E=0.84V	0x0F=0.85V
				0x10=0.86V	0x11=0.87V	0x12=0.88V	0x13=0.89V
				0x14=0.90V	0x15=0.91V	0x16=0.92V	0x17=0.93V
				0x18=0.94V	0x19=0.95V	0x1A=0.96V	0x1B=0.97V
				0x1C=0.98V	0x1D=0.99V	0x1E=1.00V	0x1F=1.01V
				0x20=1.02V	0x21=1.03V	0x22=1.04V	0x23=1.05V
				0x24=1.06V	0x25=1.07V	0x26=1.08V	0x27=1.09V
				0x28=1.10V	0x29=1.10V	0x2A=1.10V	0x2B=1.10V
				0x2C=1.10V	0x2D=1.10V	0x2E=1.10V	0x2F=1.10V
Reserved	7:6	R/W	0	Reserved			

2. Channel4 Output Voltage Setting Register (0x02)

This register set Channel4 output voltage. $V_{OUT4\_DEFAULT}$=2.8V/3.30V, CH4 default output voltage and register value table is as below:

PORSEL	VSEL4	V_{OUT4}	Register default value
0	0	2.8V	0x01
0	1	Bypass	-
1	0	2.8V	0x01
1	1	3.3V	0x06

Register Name	OUT4_REG			Output voltage setting register for channel 4
Address				0x02
Field	Bit	R/W	Default	Output voltage setting for OUT4. DVS from 2.7V to 3.6V in 100mV steps.

VOUT4_SET	3:0	R/W	Default 0x01=2.8V or 0x06=3.30V	0x00=2.70V	0x01=2.80V	0x02=2.90V	0x03=3.00V
				0x04=3.10V	0x05=3.20V	0x06=3.30V	0x07=3.40V
				0x08=3.50V	0x09=3.60V	0x0A=3.60V	0x0B=3.60V
				0x0C=3.60V	0x0D=3.60V	0x0E=3.60V	0x0F=3.60V
Reserved	7:4	R/W	0	Reserved			

3. ON/OFF Control Register. (0x03)

Register Name	ON/OFF_Control			Channel ON/OFF Control register	
Address				0x03	
	Bit	**R/W**	**Default**	**Description**	
EN1	0	R/W	1	CH1 ON/OFF control	
				0: Disable	1: Enable
EN2	1	R/W	1	CH2 ON/OFF control	
				0: Disable	1: Enable
EN3	2	R/W	1	CH3 ON/OFF control	
				0: Disable	1: Enable
EN4	3	R/W	1	CH4 ON/OFF control	
				0: Disable	1: Enable
EN5	4	R/W	1	CH5 ON/OFF control	
				0: Disable	1: Enable
EN6	5	R/W	1	CH6 ON/OFF control	
				0: Disable	1: Enable
EN7	6	R/W	1	CH7 ON/OFF control	
				0: Disable	1: Enable
Reserved	7	R/W	0	Reserved	

4. Discharge Function Control Register. (0x04)

This register controls the output discharge function during PMIC shutdown mode. DCDC converter discharge function still works during power-off procedure at VIN off when the value is set to 1.

Register Name	Discharge Control			Channel Discharge Control	
Address				0x04	
	Bit	**R/W**	**Default**	**Description**	
ENDIS_CH1	0	R/W	1	CH1 discharge control	
				0: Disable	1: Enable

ENDIS_CH2	1	R/W	1	CH2 discharge control	
				0: Disable	1: Enable
ENDIS_CH3	2	R/W	1	CH3 discharge control	
				0: Disable	1: Enable
ENDIS_CH4	3	R/W	1	CH4 discharge control	
				0: Disable	1: Enable
ENDIS_CH5	4	R/W	1	CH5 discharge control	
				0: Disable	1: Enable
ENDIS_CH6	5	R/W	1	CH6 discharge control	
				0: Disable	1: Enable
ENDIS_CH7	6	R/W	1	CH7 discharge control	
				0: Disable	1: Enable
Reserved	7	R/W	0	Reserved	

5. DCDC Mode Control Register. (0x05)

This register controls the DCDC operation mode.

This register controls Buck DC/DC Regulator PWM/PFM mode operation at light load condition. If MODE(n) bit is set to1, CH(n) will always works in forced PWM mode. If MODE(n) bit is set to 0, CH(n) will always work in PFM mode at light load condition.

Register Name	PWM/PFM_REG			PWM/PFM mode selection Register	
Address				0x05	
	Bit	**R/W**	**Default**	**Description**	
MODE1	0	R/W	1	Channel 1 mode Control bit	
				0=Forced PWM	1= Auto PFM/PWM
MODE3	1	R/W	1	Channel 3 mode Control bit	
				0=Forced PWM	1= Auto PFM/PWM
MODE4	2	R/W	1	Channel 4 mode Control bit	
				0=Forced PWM	1= Auto PFM/PWM
MODE5	3	R/W	1	Channel 5 mode Control bit	
				0=Forced PWM	1= Auto PFM/PWM
MODE7	4	R/W	1	Channel 7 mode Control bit	
				0=Forced PWM	1= Auto PFM/PWM
Reserved	7:5	R/W	0	Reserved	

6. Sleep Mode Channel3 Output Voltage Setting Register (0x06)

This register set Channel3 sleep mode output voltage. $V_{OUT3\_DEFAULT}$=0.75V

Register Name	SLP_OUT3_REG			Output voltage setting register for channel 3			
Address				0x06			
Field	Bit	R/W	Default	Output voltage setting for OUT3. DVS from 0.7V to 1.1V in 10mV steps.			
SLP_VOUT3_SET	5:0	R/W	Default 0x05=0.75V	0x00=0.70V	0x01=0.71V	0x02=0.72V	0x03=0.73V
				0x04=0.74V	0x05=0.75V	0x06=0.76V	0x07=0.77V
				0x08=0.78V	0x09=0.79V	0x0A=0.80V	0x0B=0.81V
				0x0C=0.82V	0x0D=0.83V	0x0E=0.84V	0x0F=0.85V
				0x10=0.86V	0x11=0.87V	0x12=0.88V	0x13=0.89V
				0x14=0.90V	0x15=0.91V	0x16=0.92V	0x17=0.93V
				0x18=0.94V	0x19=0.95V	0x1A=0.96V	0x1B=0.97V
				0x1C=0.98V	0x1D=0.99V	0x1E=1.00V	0x1F=1.01V
				0x20=1.02V	0x21=1.03V	0x22=1.04V	0x23=1.05V
				0x24=1.06V	0x25=1.07V	0x26=1.08V	0x27=1.09V
				0x28=1.10V	0x29=1.10V	0x2A=1.10V	0x2B=1.10V
				0x2C=1.10V	0x2D=1.10V	0x2E=1.10V	0x2F=1.10V
Reserved	7:6	R/W	0	Reserved			

7. Sleep Mode Channel4 Output Voltage Setting Register (0x07)

This register set Channel4 output voltage. $V_{OUT4\_DEFAULT}$=2.8V/3.30V, CH4 default output voltage and register value table is as below:

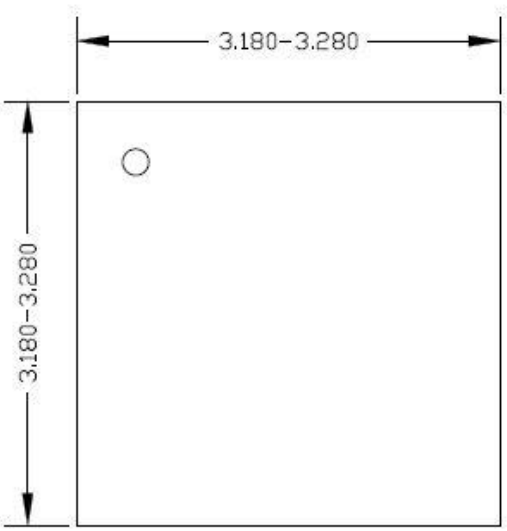
PORSEL	VSEL4	V_{OUT4}	Register default value
0	0	2.8V	0x01
0	1	Bypass	-
1	0	2.8	0x01
1	1	3.3	0x06

Register Name	SLP_OUT4_REG			Output voltage setting register for channel 4			
Address				0x07			
Field	Bit	R/W	Default	Output voltage setting for OUT4. DVS from 2.7V to 3.6V in 100mV steps.			
SLP_VOUT4_SET	3:0	R/W	Default 0x01=2.8V or 0x06=3.30V	0x00=2.70V	0x01=2.80V	0x02=2.90V	0x03=3.00V
				0x04=3.10V	0x05=3.20V	0x06=3.30V	0x07=3.40V
				0x08=3.50V	0x09=3.60V	0x0A=3.60V	0x0B=3.60V
				0x0C=3.60V	0x0D=3.60V	0x0E=3.60V	0x0F=3.60V
Reserved	7:4	R/W	0	Reserved			

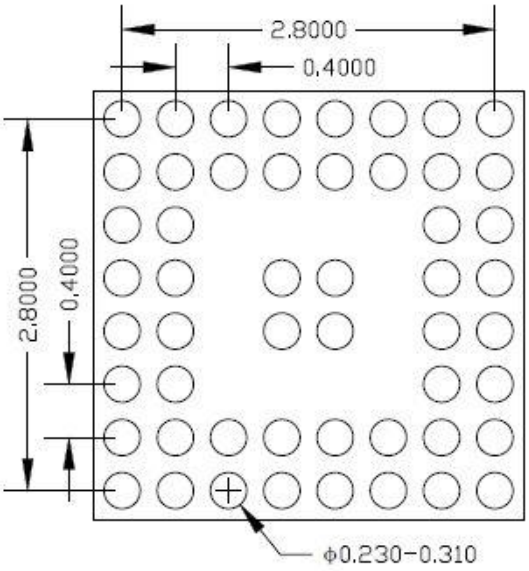
8. Sleep Mode ON/OFF Control Register. (0x08)

Register Name	SLP_ON/OFF_Control			Channel sleep mode ON/OFF Control register	
Address				0x08	
	Bit	**R/W**	**Default**	**Description**	
SLP_EN1	0	R/W	1	Sleep mode CH1 ON/OFF control	
				0: Disable	1: Enable
SLP_EN2	1	R/W	1	Sleep mode CH2 ON/OFF control	
				0: Disable	1: Enable
SLP_EN3	2	R/W	1	Sleep mode CH3 ON/OFF control	
				0: Disable	1: Enable
SLP_EN4	3	R/W	0	Sleep mode CH4 ON/OFF control	
				0: Disable	1: Enable
SLP_EN5	4	R/W	0	Sleep mode CH5 ON/OFF control	
				0: Disable	1: Enable
SLP_EN6	5	R/W	0	Sleep mode CH6 ON/OFF control	
				0: Disable	1: Enable
SLP_EN7	6	R/W	0	Sleep mode CH7 ON/OFF control	
				0: Disable	1: Enable
SLEEP	7	R/W	0	Sleep mode control bit	
				0: PMIC exist sleep mode	1: PMIC enter sleep mode

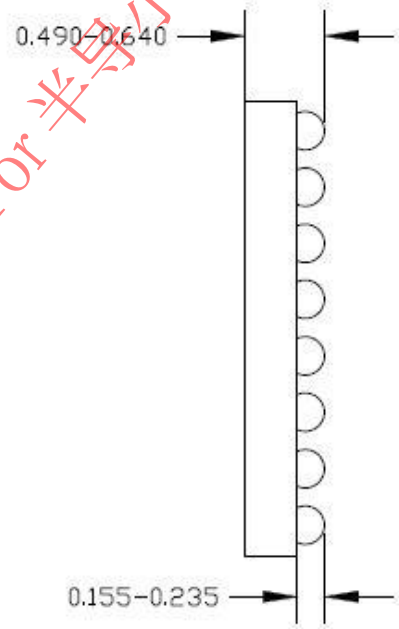
CSP3.23×3.23-52 Package Outline Drawing



Top view



Bottom view



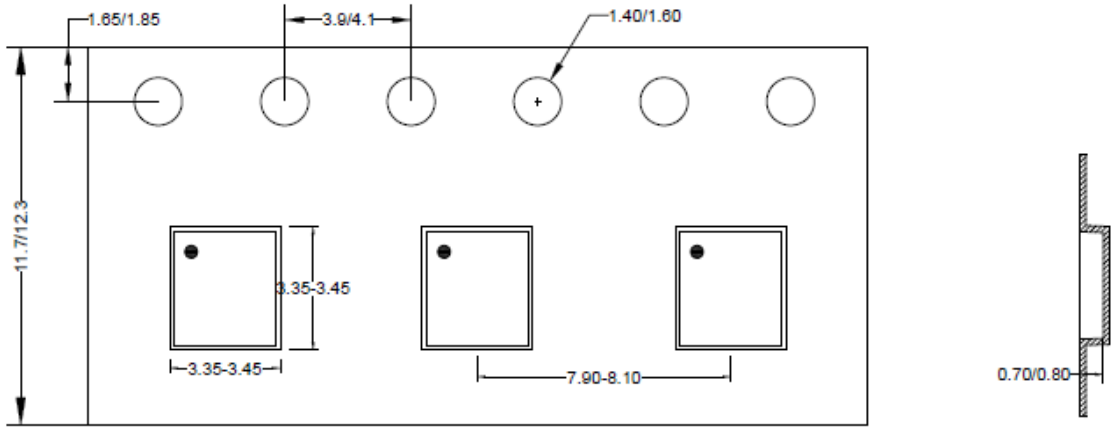
Side View

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

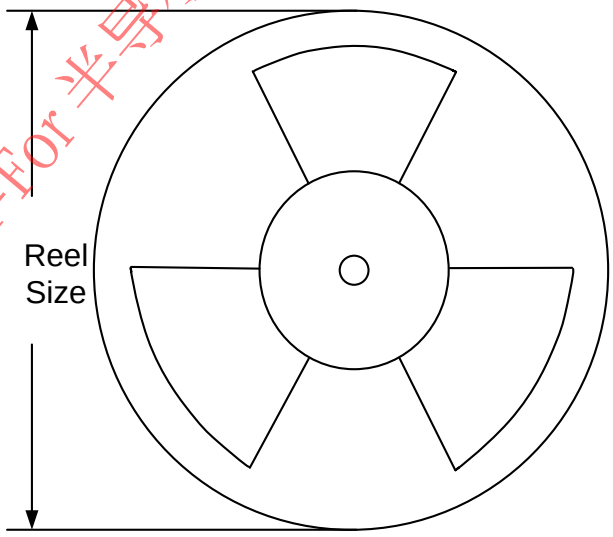
1. Taping orientation

CSP3.23×3.23



Feeding direction

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
CSP3.23×3.23	12	8	13"	400	400	5000

3. Others: NA