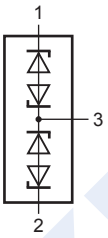
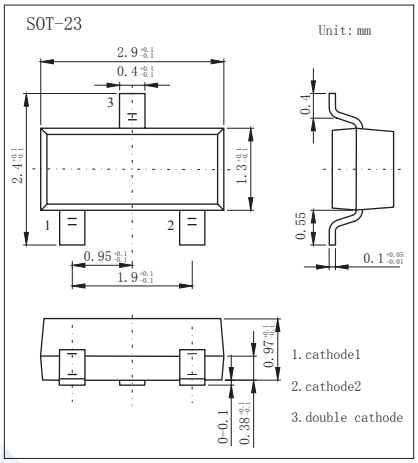
ESD Protection Diodes

PESDxL2BT series

■ Features

- ESD protection of two lines
- Max. peak pulse power: P_{PP}=350W
- Low clamping voltage: V_{CL}=26V
- Small SMD plastic package
- Ultra low leakage current: I_{RM}<90nA
- ESD protection up to 23 kV
- IEC61000-4-2, level4 (ESD)
- IEC61000-4-5 (surge); I_{PP}=15A





■ Absolute Maximum Ratings

Parameter		Symbol	PESD 3V3L2BT	PESD 5V0L2BT	PESD 12VL2BT	PESD 15VL2BT	PESD 24VL2BT	Unit
Electrostatic dischargevoltage	IEC61000-4-2 (Note 2,3) (contact discharge)	V_{ESD}	30				23	KV
	HBM MIL-STD883		10					
Peak pulse power t_p=8/20 μs (Note 1,2)		P_{PP}	350		200			W
Peak pulse current t_p=8/20 μs (Note 1,2)		I_{PP}	15	13	5		3	A
Junction temperature		T_j	150					℃
Ambient temperature		T_{amb}	-65 to +150					
Storage temperature		T_{stg}	-65 to +150					

Note 1: Non-repetitive current pulse 8/20μs exponential decay waveform according to IEC61000-4-5.

Note 2: Measured from pin 1 to 3 or 2 to 3.

Note 3: Device stressed with ten non-repetitive ESD pulses.

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■ Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reverse standoff voltage						
PESD3V3L2BT	V_{RWM}				3.3	V
PESD5V0L2BT					5.0	V
PESD12VL2BT					12	V
PESD15VL2BT					15	V
PESD24VL2BT					24	V
Reverse leakage current						
PESD3V3L2BT	I_{RM}	V_{RWM}=3.3V			2	μA
PESD5V0L2BT		V_{RWM}=5.0V			1	μA
PESD12VL2BT		V_{RWM}=12V			50	nA
PESD15VL2BT		V_{RWM}=15V			50	nA
PESD24VL2BT		V_{RWM}=24V			50	nA
Breakdown voltage	V_{BR}	I_R=5mA				
PESD3V3L2BT			5.8	6.4	6.9	V
PESD5V0L2BT			7.0	7.6	8.2	V
PESD12VL2BT			14.2	15.8	16.7	V
PESD15VL2BT			17.1	18.8	20.3	V
PESD24VL2BT			25.4	27.8	30.3	V
Diode capacitance	C_d	V_R=0V; f=1MHz				
PESD3V3L2BT					101	pF
PESD5V0L2BT					75	pF
PESD12VL2BT					19	pF
PESD15VL2BT					16	pF
PESD24VL2BT					11	pF
Clamping voltage (Note 1,2)	V_{CL}					
PESD3V3L2BT		I_{PP}=1A			8	V
		I_{PP}=15A			26	V
PESD5V0L2BT		I_{PP}=1A			10	V
		I_{PP}=13A			28	V
PESD12VL2BT		I_{PP}=1A			20	V
		I_{PP}=5A			37	V
PESD15VL2BT		I_{PP}=1A			25	V
		I_{PP}=5A			44	V
PESD24VL2BT		I_{PP}=1A			40	V
		I_{PP}=3A			70	V
Differential resistance	r_{dif}	I_R=1mA				
PESD3V3L2BT					400	Ω
PESD5V0L2BT					80	Ω
PESD12VL2BT					200	Ω
PESD15VL2BT					225	Ω
PESD24VL2BT					300	Ω

Note 1: Non-repetitive current pulse 8/20μs exponential decay waveform according to IEC61000-4-5.

Note 2: Measured from pin 1 to 3 or 2 to 3.

■ Marking

Type	PESD3V3L2BT	PESD5V0L2BT	PESD12VL2BT	PESD15VL2BT	PESD24VL2BT
Marking	V3W	V4W	V5W	V6W	V7W

ESD Protection Diodes

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■ Typical Characterisitics

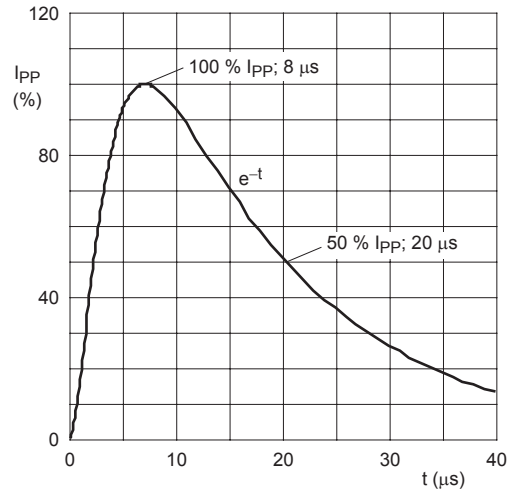


Fig 1. 8/20 µs pulse waveform according to IEC 61000-4-5

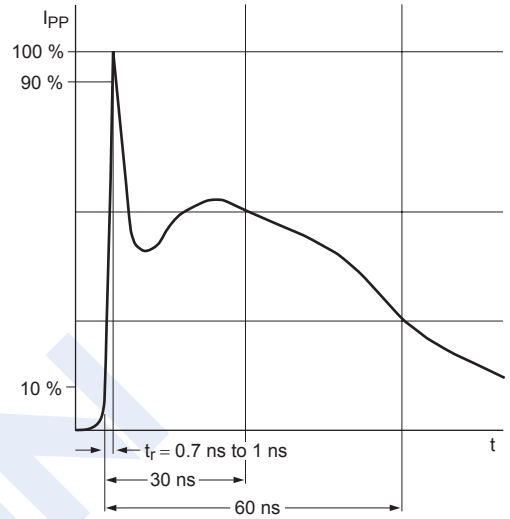
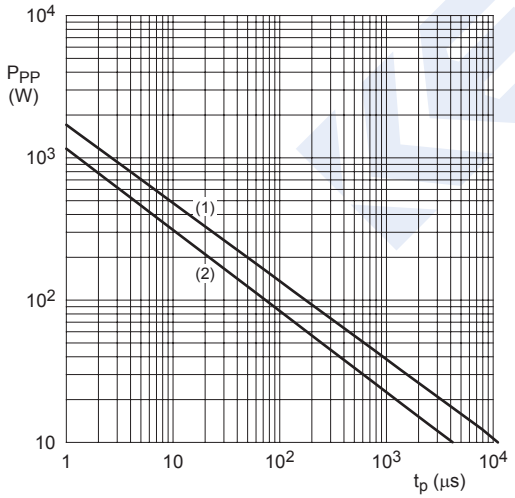


Fig 2. ESD pulse waveform according to IEC 61000-4-2



T_{amb} = 25 °C

(1) PESD3V3L2BT and PESD5V0L2BT

(2) PESD12VL2BT, PESD15VL2BT, PESD24VL2BT

Fig 3. Peak pulse power as a function of exponential pulse duration t_p; typical values

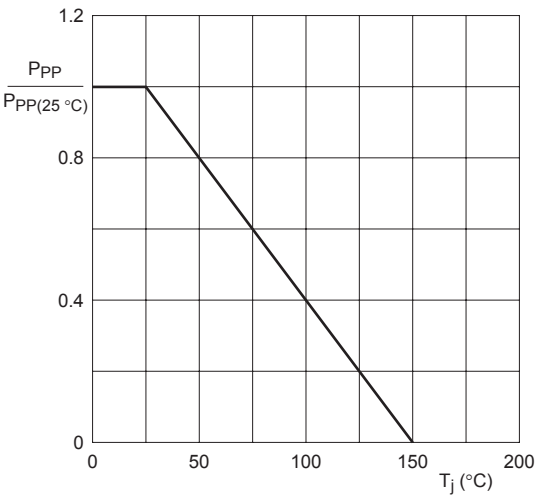
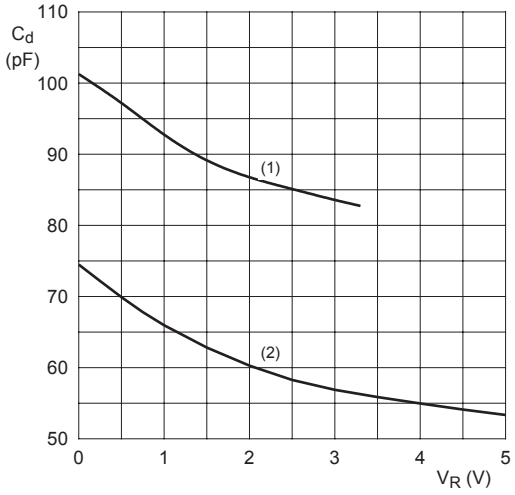


Fig 4. Relative variation of peak pulse power as a function of junction temperature; typical values

ESD Protection Diodes

PESDxL2BT series

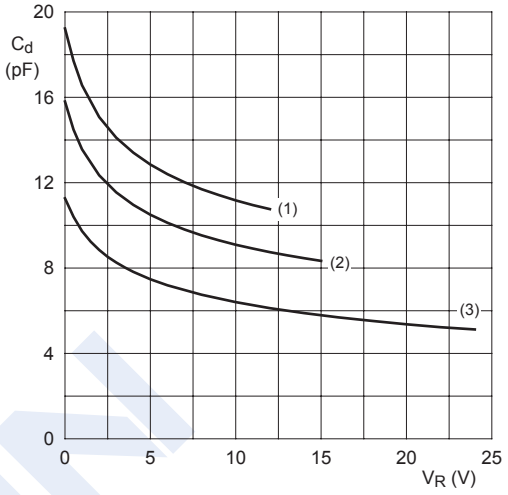


T_{amb} = 25 °C; f = 1 MHz

(1) PESD3V3L2BT

(2) PESD5V0L2BT

Fig 5. Diode capacitance as a function of reverse voltage; typical values



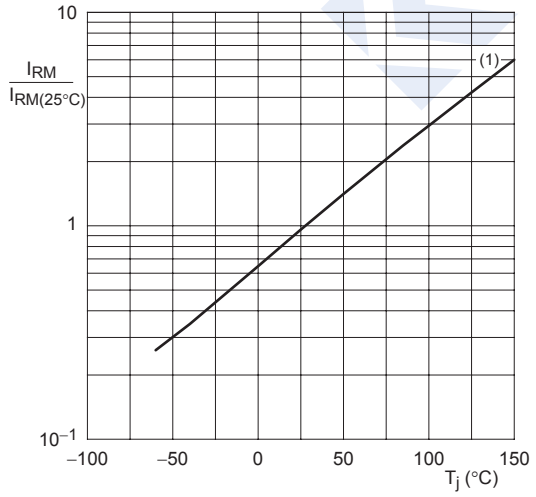
T_{amb} = 25 °C; f = 1 MHz

(1) PESD12VL2BT

(2) PESD15VL2BT

(3) PESD24VL2BT

Fig 6. Diode capacitance as a function of reverse voltage; typical values



(1) PESD3V3L2BT, PESD5V0L2BT

PESD12VL2BT, PESD15VL2BT and PESD24VL2BT: I_{RM} < 20 nA; T_j = 150 °C

Fig 7. Relative variation of reverse leakage current as a function of junction temperature; typical values

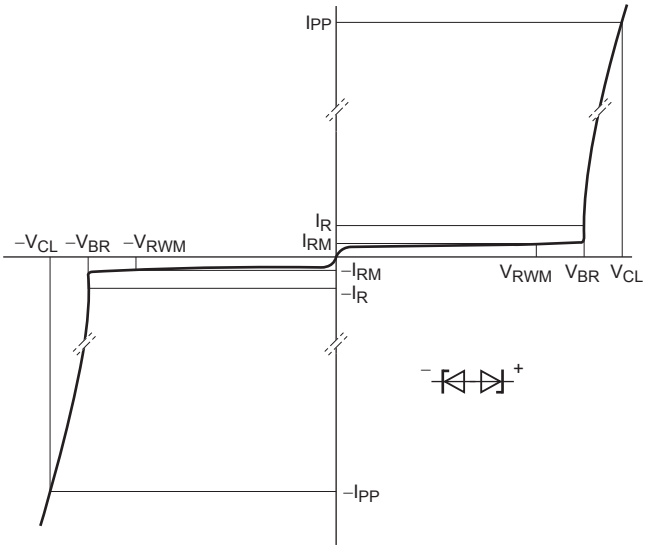


Fig 8. V-I characteristics for a bidirectional ESD protection diode

ESD Protection Diodes

PESDxL2BT series

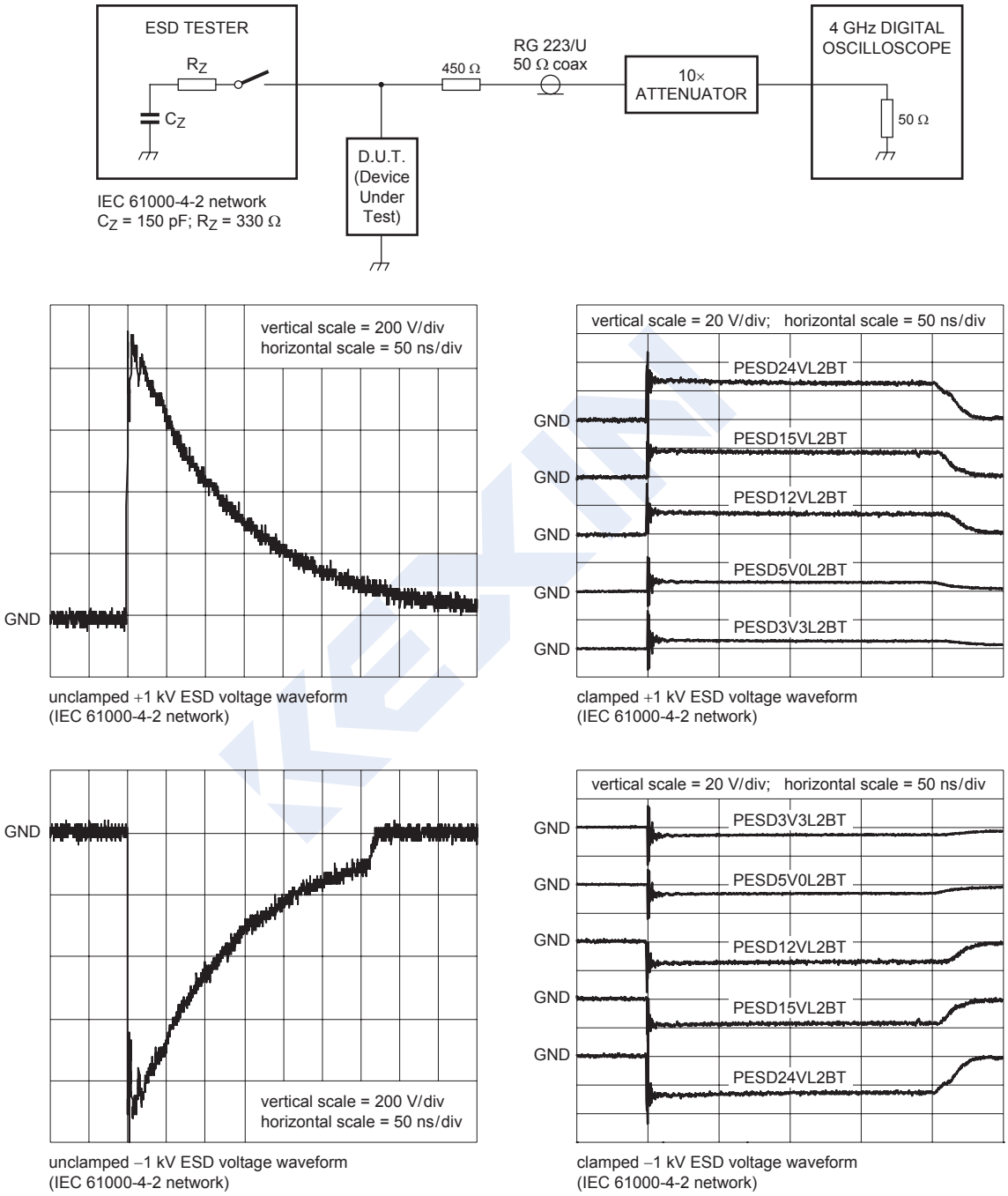


Fig 9. ESD clamping test setup and waveforms

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PESDxL2BT series

■ Application information

The PESDxL2BT series is designed for the protection of two bidirectional signal lines from the damage caused by ESD and surge pulses. The PESDxL2BT series may be used on lines where the signal polarities are above and below ground. The PESDxL2BT series provides a surge capability of up to 350 W per line for an 8/20 μs waveform.

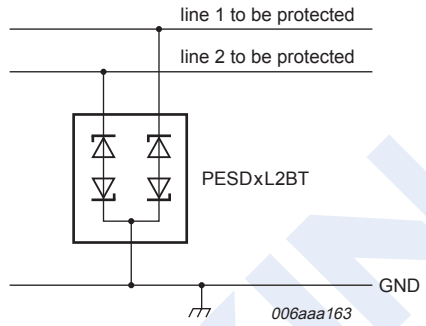

Fig 10. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the PESDxL2BT as close to the input terminal or connector as possible.
2. The path length between the PESDxL2BT and the protected line should be minimized.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.