

DATA SHEET

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AG1KLP

Low power and low cost FPGA

General Description

AG1KLP family provides low cost, ultra-low power, SRAM-based FPGAs, with density is ranging from 640 up to 1280 Look-Up Tables (LUTs). The devices feature Embedded Block Memory (EBR), Distributed RAM, and Phase Locked Loops (PLLs), while offering small footprint package WLSCP and ucBGA. The devices are designed for ultra low power and cost while providing programmable solutions for a wide range of applications, especially in consumer and mobile device products.

Features

- Low power and low cost FPGA.
- Flexible logic architecture based on LUT.
- Ultra-low power, as low as 50 μ A standby typical I_{cc} (1.2V V_{cc}).
- Broad range of package options, small footprint package for consumer and mobile application.
- Provides PLL per device provide clock multiplication and phase shifting
- 3.3-V, 2.5-V, 1.8-V, 1.5-V LVCMOS and LVTTTL standards
- Flexible device configuration through SPI interface.
- Table 1-1 Shows AG1KLP family features

Feature	AG1KLP
LUTs	640, 1280
Distributed RAM (Kbits)	10
EBR SRAM (Kbits)	68
Maximum User I/O pins	40
Number of PLLs	1
Package	16-Pin WLCSP 36-Pin ucBGA 49-Pin ucBGA 48-Pin QFN

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1. AG1KLP Architecture Overview

1.1. Functional Description

The AG1KLP devices contain an industrial state-of-the-art two-dimensional row- and column-based architecture to implement custom logic. Column and row interconnects of various speeds provide signal interconnects between logic blocks (LBs) and IOs.

The logic array consists of LBs, with 16 logic slices (LS) in each LB. A slice is a small unit of logic providing efficient implementation of user logic functions. LBs are grouped into rows and columns across the device. The AG1KLP devices' density is ranging from 640 to 1280 slices.

The device global clock network consists of up to 8 global clock lines that drive through the entire device. The global clock network can provide clocks for all resources within the device, such as input/output elements (IOEs), slices. The global clock lines can also be used for other high fan-out signals.

Each device I/O pin is fed by an IOE located at the ends of LB rows and columns around the periphery of the device. I/O pins support various single-ended standards. Each IOE contains a bidirectional I/O buffer.

1.2. Logic Array Blocks

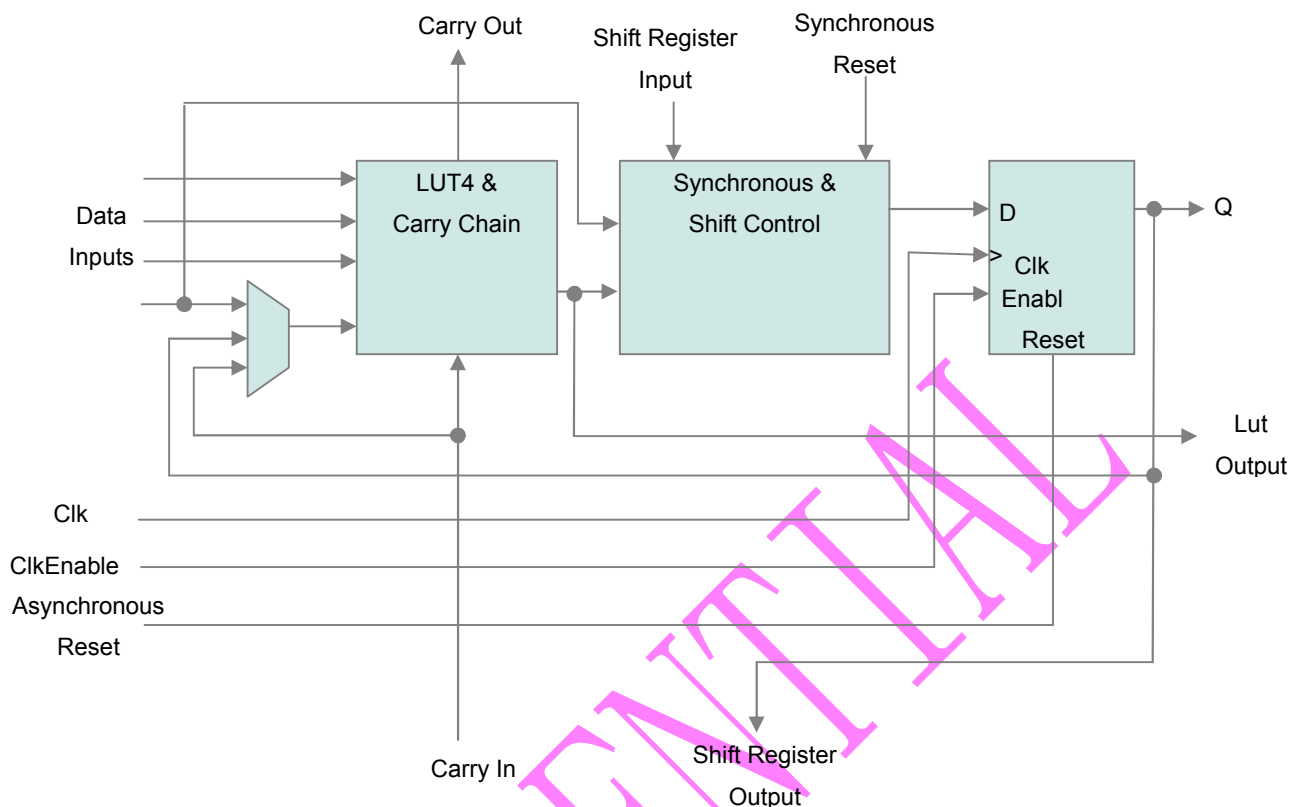
Each Logic Block consists of 16 slices, SLICE carry chains, SLICE control signals, a local interconnect, a look-up table (LUT) chain, and register chain connection lines. There are 32 possible unique inputs into an SLICE. Register chain connections transfer the output of one SLICE's register to the adjacent SLICE's register within a block. The AG1KLP software places associated logic within an SLICE or adjacent SLICES, allowing the use of local, LUT chain, and register chain connections for performance and area efficiency.

1.3. Logic Element

The smallest unit of logic in AG1KLP architecture, the slice, is compact and provides advanced and flexible features with efficient logic utilization. Each slice features:

- Industrial standard four-input look-up table (LUT4), which is a function generator that can implement any combinatorial logic function of four inputs.
- A programmable register
- A carry chain connection
- A register chain connection
- The ability to drive all types of interconnects: local, row, column, register chain, and inter-tile connections
- Support for efficient packing of LUT and register
- Support for register feedback

Figure 1-1 AG1KLP Logic SLICE



Each slice’s register has data, clock, clock enable, and clear inputs. Signals that from global clock network, general-purpose I/O pins, or any internal logic outputs can drive the register’s clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable. For combinational functions, the LUT output bypasses the register and drives directly to the slice outputs resources. The slice is architected so that LUT and register can drive to separate outputs.

1.4. FlexTrack Interconnect

In AG1KLP device architecture, FlexTrack interconnect consists of continuous, performance-optimized routing lines used for inter- and intra- design block connectivity. The FlexTrack connects to LEs, and IO pins with row and column connection that span fixed distances.

1.5. Global Signals

Each device has eight dual-purpose dedicated clock pins. The eight global clock lines drive throughout the entire device. The global clock network can provide clocks for all resources within the device including LEs, local interconnect. The global lines can be used for global signals distribution.

1.6. Phase Locked Loops (PLLs)

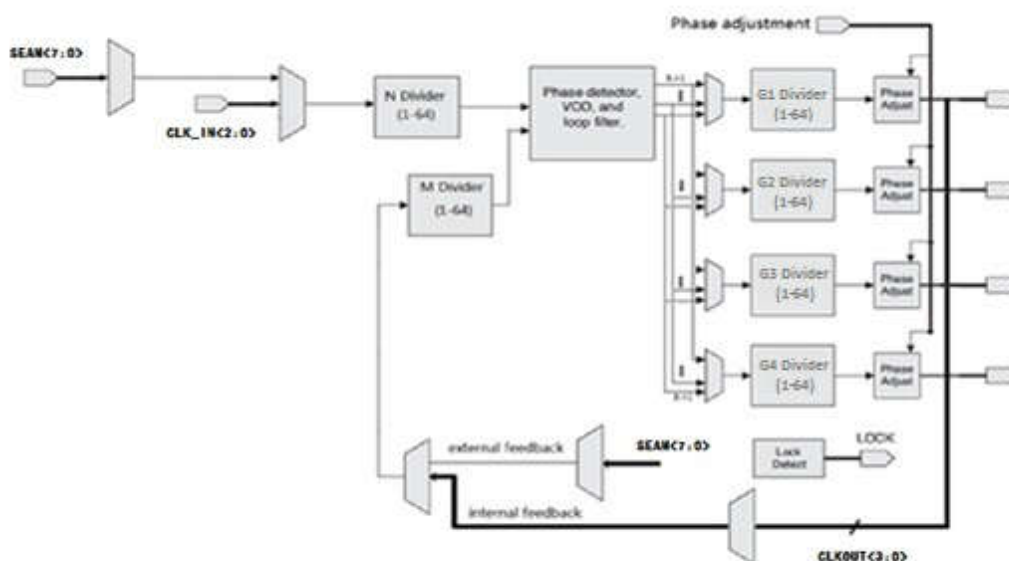
The AG1KLP provides PLL support. The PLL has four output The source of the PLL input divider can come from an external pin or from internal routing. There are four sources of feedback signals to the

feedback divider: from CLKINTFB (internal feedback port), from the global clock nets, from the output of the post scalar divider, and from the routing (or from an external pin). There is a PLL_LOCK signal to indicate that the PLL has locked on to the input clock signal. Figure 1-2 shows the PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after adjustment and not relock until the tLOCK parameter has been satisfied. Additionally, the phase and duty cycle block allows the user to adjust the phase and duty cycle of the CLKOS output.

The PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider, post scalar divider, and secondary clock divider. The input clock divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal. The post scalar divider allows the VCO to operate at higher frequencies than the clock output, thereby increasing the frequency range. The secondary divider is used to derive lower frequency outputs.

Figure 1-2. PLL Diagram



PLL Output Features:

- Output frequency is 16MHz-275MHz.
- VCO range 533MHz – 1066MHz
- Jitter is about 5%.
- Static current <1uA
- Operating Temperature Range:- 25°C ~ 125°C
- Operation Voltage: 1.2V ± 5%

PLL Input Features:

- 10MHz-133MHz.
- Power down PLL.
- A reset input.

1.7.Embedded Block RAM

AG1KLP contains 14 Embedded Block RAMs (EBRs). The EBR consists of a 4.5Kbit RAM, with dedicated input and output registers. This memory can be used for a wide variety of purposes including data buffering and FIFO. The EBR block can implement single port, dual port, simple dual port, or FIFO memories. Each block can be used in a variety of depths and widths as shown in Table 1-1.

Memory Mode	Configurations
Single Port	4096 x 1 2048 x 2 1024 x 4 512 x 9 256 x 18 128 x 36
True Dual Port	4096 x 1 2048 x 2 1024 x 4 512 x 9 256 x 18
Pseudo Dual Port	4096 x 1 2048 x 2 1024 x 4 512 x 9 256 x 18 128 x 36
FIFO	4096 x 1 2048 x 2 1024 x 4 512 x 9 256 x 18 128 x 36

If desired, the contents of the RAM can be pre-loaded during device configuration.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the EBR block can also be utilized as a ROM.

Larger and deeper blocks of RAM can be created using EBR Blocks.

In all the RAM modes, the input data and addresses for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the memory array output.

The EBR memory supports three forms of write behavior for single or dual port operation:

1. Normal: Data on the output appears only during the read cycle.

2. Write Through: A copy of the input data appears at the output of the same port.
3. Read-Before-Write: When new data is being written, the old data of the address appears at the output.

1.8. I/O Pin

I/O supported features:

- Supports 3.3-V, 2.5-V, 1.8-V, and 1.5-V logic levels
- Programmable drive strength, bus-hold, pull-up resistors, open-drain output, and Schmitt triggers input.
- 3.3-V, 2.5-V, 1.8-V, 1.5-V LVCMOS and LVTTTL standards

2. Device Configuration

AG1KLP device supports SPI master or slave mode configuration. External Flash provides a non-volatile storage for the configuration data. Additionally, the configuration data can be downloaded from an external processor, microcontroller, or DSP processor using the SPI interface.

2.1. Configuration Mode Selection

The AG1KLP configuration mode is selected according to the following priority described below.

- After exiting the Power-On Reset (POR) state or when CRESET_B returns High after being held Low, the AG1KLP device samples the logical value on its SPI_SS_B pin. Like other programmable I/O pins, the SPI_SS_B pin has an internal pull-up resistor.
- If the SPI_SS_B pin is sampled as a logic '1' (High), then the device configures using the SPI Master Configuration Interface.
- If the SPI_SS_B pin is sampled as a logic '0' (Low), then the device waits to be configured from an external controller or from another device in SPI Master Configuration Mode using an SPI-like interface.

2.2. CONFIG Pins

The AG1KLP has a set of CONFIG pins that are used to program and configure the device.

The CONFIG pins are dual-function, meaning they can be recovered as user I/O after configuration is complete. Table 2-1 shows the CONFIG pins.

Table 2-1. CONFIG Pins

Pin Name	Pin Direction	Description
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CRESET_B	Input	Configuration Reset input, active-low. No internal pull-up resistor.
CDONE	Output	Configuration Done output. The pin has a permanent, weak internal pull-up resistor to the VCCIO_2 rail. Depending on the frequency of configuration and the capacitance on CDONE node, then CDONE pin must be tied to an external pullup resistor connected to the VCCIO_2 supply. The SWG16 package CDONE pin can be used as a user output.
SPI_SS_B	Input/Output	An important dual-function, active-low slave select pin. After the device exits POR or CRESET_B is toggled (High-Low- High), it samples the SPI_SS_B to select the configuration mode (an output in Master mode and an input in Slave mode).
SPI_SI	Input	A dual-function, serial input pin in both configuration modes.
SPI_SO	Output	A dual-function, serial output pin in both configuration modes.
SPI_SCK	Input/Output	A dual-function clock signal. An output in Master mode and input in Slave mode.

3. Power-On Reset Circuitry

3.1. Power-On Reset Circuitry

When power is applied to AG1KLP devices, the POR circuit monitors V_{CC} and begins SRAM download at an approximate voltage of 1.2V AG1KLP devices.

Entry into user mode is gated by whether V_{CCIO} bank2 are powered with sufficient operating voltage. If V_{CC} and V_{CCIO} are powered simultaneously, the device enters user mode.

For AG1KLP when in user mode, the POR circuitry continues to monitor the V_{CC} (but not V_{CCIO}) voltage level to detect a brown-out condition. If there is a V_{CC} voltage sag at during user mode, the POR circuit resets the SRAM and tri-states the I/O pins. Once V_{CC} rises back to approximately 1.2V, the SRAM download restarts and the device begins to operate.

3.2. Power Saving Options

AG1KLP devices have been designed with features that allow users to meet the static and dynamic power requirements of their applications by controlling various device subsystems power-on-reset circuitry, PLLs, etc.

4. DC Electrical Characteristics

Table 4-1 Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
VCC	Core Supply Voltage	1.14	1.26	V

VCCPLL	PLL Supply Voltage		1.14	1.26	V
VCCIO	I/O Driver Supply Voltage	VCCIO0,2	1.71	3.46	V
		VCC_SPI	1.71	3.46	V

Table 4-2 Recommended Operating Conditions

Symbol	Parameter	Typ.	Units
IIL, IIH	Input or I/O Leakage	+/-1	μ A
C1	I/O Capacitance	6	pF
C2	Global Input Buffer Capacitance	6	pF
VHYST	Input Hysteresis	200	mV
IPU	Internal PIO Pull-up Current	-35 (VCCIO = 1.8V)	μ A
		-49 (VCCIO = 2.5V)	μ A
		-65 (VCCIO = 3.3V)	μ A
ICC	Core Power Supply	50	μ A
ICCPLL	PLL Power Supply	1	μ A

Table 4-3 Peak Startup Supply Current

Symbol	Parameter	Max.	Units
ICCPEAK	Core Power Supply	6.5	mA
ICCPLLPEAK	PLL Power Supply	1.5	mA
ICCIOPEAK, ICC_SPIPEAK	Bank Power Supply	3.4	mA

Table 4-4 IO Single-Ended DC Electrical Characteristics

Input/ Output Standard	VIL		VIH		VOL Max. (V)	VOH Min. (V)	IOL Max. (mA)	IOH Max. (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVC MOS 3.3	-0.3	0.8	2.0	VCCIO +0.2V	0.4	VCCIO -0.5	8,16,24	-8,-16,-24
LVC MOS 2.5	-0.3	0.7	1.7	VCCIO +0.2V	0.4	VCCIO -0.5	6,12,18	-6,-12,-18
LVC MOS 1.8	-0.3	0.35 VCCIO	0.65 VCCIO	VCCIO +0.2V	0.4	VCCIO -0.4	4, 8,12	-4, -8,-12

Table 4-5 Power-On-Reset Voltage Levels

Symbol	Parameter		Min.	Max	Units
VPORUP	Power-On-Reset ramp-up trip point (band gap based circuit monitoring VCC, VCCIO_2, VCC_SPI)	VCC	0.55	0.8	V
		VCCIO_2	0.9	1.1	V
		VCC_SPI	0.9	1.1	V

5. Timing Characteristics

Table 5-1 Typical Building Block Function Performance

Register-to-Register Performance		
Function	Timing	Units
16-bit counter	250	MHz
64-bit counter	100	MHz

Table 5-2 External Switching Characteristics

Parameter	Description	Min.	Max.	Units
Global Clocks				
f _{MAX_GBUF}	Frequency for Global Buffer Clock network	-	300	MHz
f _{MAX_GBUF}	Frequency for Global Buffer Clock network	-	200	ps
Pin-LUT-Pin Propagation Delay				
t _{PD}	Best case propagation delay through one LUT-4	-	6.5	ns
General I/O Pin Parameters (Using Global Buffer Clock without PLL)				
t _{CO}	Clock to Output - PIO Output Register	-	6.5	ns
t _{SU}	Clock to Data Setup - PIO Input Register	-0.3	-	ns
t _H	Clock to Data Hold - PIO Input Register	1.9	-	ns

Table 5-3 Maximum sysIO Buffer Performance

I/O Standard	Max. Speed	Units
Inputs		
LVC MOS33	250	MHz
LVC MOS25	250	MHz
LVC MOS18	250	MHz
Outputs		
LVC MOS33	250	MHz
LVC MOS25	250	MHz
LVC MOS18	155	MHz

6. Pin-Outs

Refer to Pin-Outs printouts for AG1KLP device family.

Pin name	Ball List(BGA36)	Pin name	Ball List(BGA36)
IOL_2B	A1	IOL_7A_GBIN6	D1
IOT_89	A2	GNDPLL	D2
IOT_84_GBIN1	A3	GND	D2
VDDIO_0_1	A4	GND	D3
VPP_FAST	A5	GND	D3
VPP_2V5	A6	GND	D4
IOL_2A	B1	IOB_47_SS	D5
VCC	B2	IOR_55	D6
VCCPLL	B2	IOL_7B	E1
VCC	B2	IOB_34	E2
IOT_85_GBIN0	B3	IOB_42_CBSEL0	E3
IOR_61_GBIN2	B4	IOB_44_SDO	E4
Pin name	Ball List(BGA36)	Pin name	Ball List(BGA36)
IOR_63	B5	IOB_46_SCK	E5
IOR_64	B6	IOR_54	E6
IOL_6B_GBIN7	C1	VDDIO_2_3	F1
IOL_6A	C2	IOB_35_GBIN5	F2
IOT_90	C3	IOB_43_CBSEL1	F3
CDONE	C4	CRESET_B	F4
IOR_60_GBIN3	C5	IOB_45_SDI	F5
IOR_65	C6	VCC_SPI	F6

7. Reference and Ordering Information

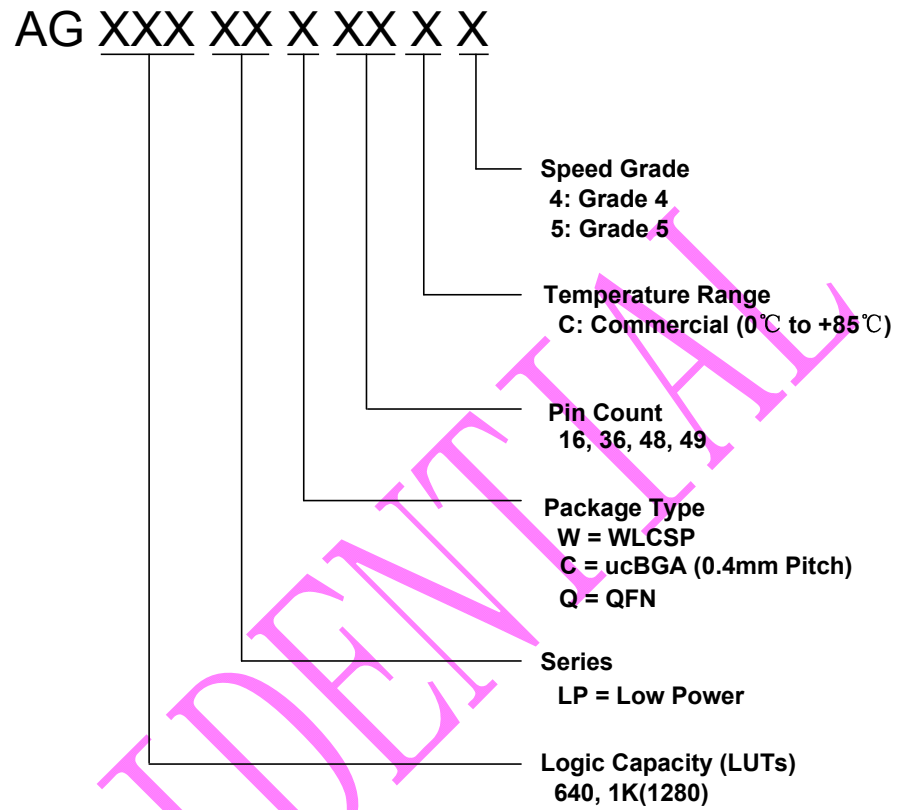
7.1. Software

AG1KLP Software tools support from RTL to bit stream configuration implementation and programming. Supported operating system platforms include Microsoft Windows and Linux.

7.2. Ordering Information

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Table 7-1 Device Part Number Description



8. Recommended Reflow Profile

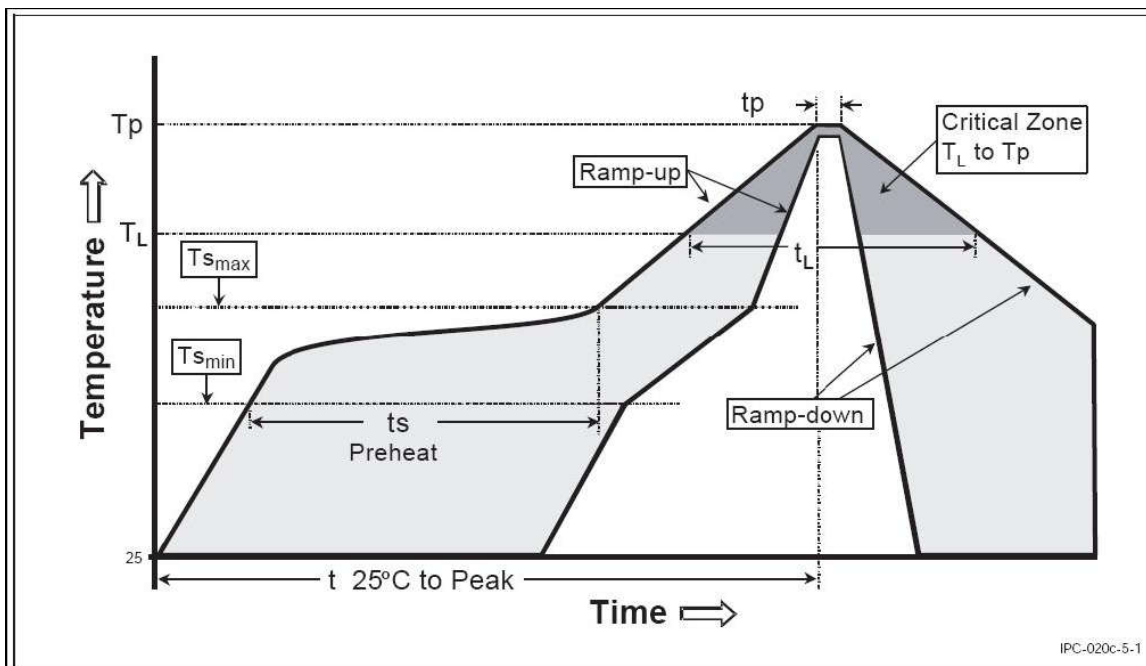


Figure. 8-1 Classification Reflow Profile

Table 8-1 Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (Tsmmax to Tp)	3 °C/second max.	3 °C/second max.
Preheat		
-Temperature Min (Tsmmin)	100 °C	150 °C
-Temperature Max (Tsmmax)	100 °C	200 °C
-Time (tsmin to tsmax)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (TL)	183 °C	217°C
-Time (tL)	60-150seconds	60-150 seconds
Peak /Classification Temperature(Tp)	See Table 10	See Table 11
Time within 5 oC of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/seconds max.
Time 25 oC to Peak Temperature	6 minutes max.	8 minutes max.

Table 8-2 Sn-Pb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm3	
	<350	≥350
<2.5mm	240 + 0/-5 °C	225 + 0/-5 °C
≥2.5mm	225 + 0/-5 °C	225 + 0/-5 °C

Table 8-3 Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm3 <350	Volume mm3 350-2000	Volume mm3 >2000
<1.6mm	260 + 0 °C *	260 + 0 °C *	260 + 0 °C *
1.6mm – 2.5mm	260 + 0 °C *	250 + 0 °C *	245 + 0 °C *
≥2.5mm	250 + 0 °C *	245 + 0 °C *	245 + 0 °C *

*Tolerance : The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature(this mean Peak reflow temperature + 0 °C. For example 260+ 0 °C) at the rated MSL Level.

Note 1: All temperature refer topside of the package. Measured on the package body surface.

Note 2: The profiling tolerance is + 0 °C , - X °C (based on machine variation capability)whatever is required to control the profile process but at no time will it exceed – 5 °C. The producer assures process compatibility at the peak reflow profile temperatures defined in Table 9-3.

Note 3: Package volume excludes external terminals(balls, bumps, lands, leads) and/or non integral heat sinks.

Note 4: The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package may sill exist.

Note 5: Components intended for use in a “lead-free” assembly process shall be evaluated using the “lead free” classification temperatures and profiles defined in Table8-1, 8-2, 8-3 whether or not lead free.

9. Change List

The following table summarizes revisions to this document.

REV	DATE	AUTHER	CHANGE DESCRIPTION
V1.0	03/27/2014		Release Version 1.0
V1.1	04/10/2014		Delete lvds function
V1.2	04/30/2014		Add contents as below - DC electrical characteristics - Timing Characteristics - SPI configuration
V1.3	07/03/2014		Add contents as below

			-Pinouts -Package diagram
V1.4	10/10/2014		
V1.5	9/10/2015		-QFN package

10. RoHS Compliant

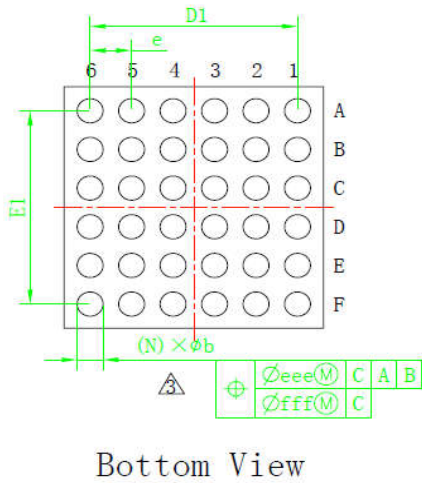
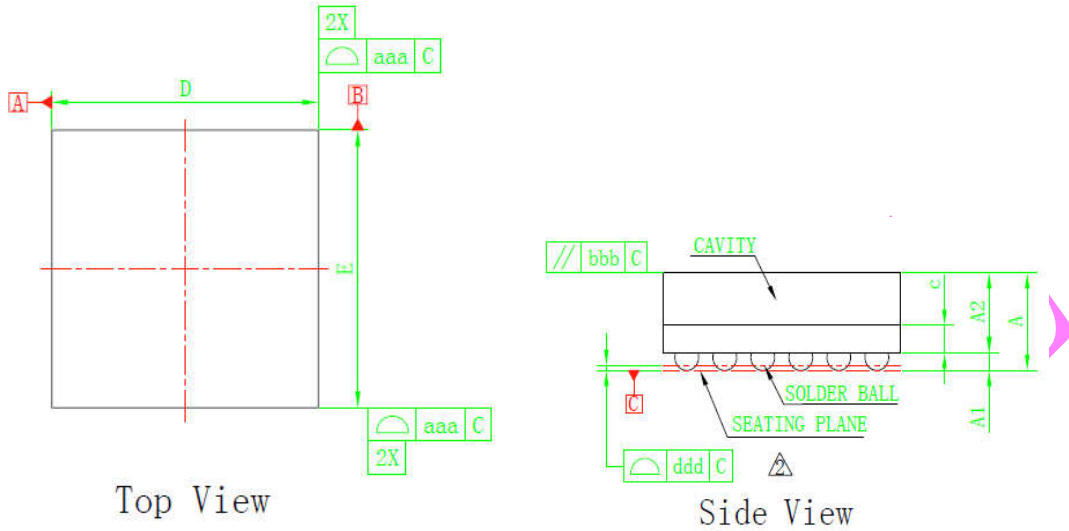
The product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE), and are therefore considered RoHS compliant.

11. ESD Precautions

ESD protection circuitry is contended in this device, but special handling precautions are required.

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Package Diagram(BGA36)



symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	0.980	—	—	0.039
A1	0.120	0.170	0.220	0.005	0.007	0.009
A2	0.660	0.710	0.760	0.026	0.028	0.030
c	0.170	0.210	0.250	0.007	0.008	0.010
D	2.450	2.500	2.550	0.096	0.098	0.100
E	2.450	2.500	2.550	0.096	0.098	0.100
D1	—	2.000	—	—	0.079	—
E1	—	2.000	—	—	0.079	—
e	—	0.400	—	—	0.016	—
b	0.200	0.250	0.300	0.008	0.010	0.012
aaa	—	0.100	—	—	0.004	—
bbb	—	0.200	—	—	0.008	—
ddd	—	0.080	—	—	0.003	—
eee	—	0.150	—	—	0.006	—
fff	—	0.050	—	—	0.002	—
N	—	36	—	—	36	—
MD/ME	—	6/6	—	—	6/6	—