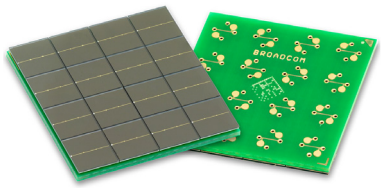
Data Sheet

AFBR-S4N44P163

4×4 NUV-HD Silicon Photo Multiplier Array



Description

The Broadcom® AFBR-S4N44P163 is a 4×4 Silicon Photo Multiplier (SiPM) array used for ultra-sensitive precision measurements of single photons. The pitch of SiPMs is 4 mm in both directions. High packing density of the single chips is achieved using trough-silicon-via (TSV) technology. Larger areas can be covered with a pitch of 16 mm by tiling multiple AFBR-S4N44P163 arrays almost without any edge losses. The passivation layer is made by a glass highly transparent down to UV wavelengths, resulting in a broad response in the visible light spectrum with high sensitivity towards blue- and near-UV region of the light spectrum. The array is best suited for the detection of low-level pulsed light sources, especially for detection of Cherenkov- or scintillation light from the most common organic (plastic) and inorganic scintillator materials (for example, LSO, LYSO, BGO, NaI, CsI, BaF, LaBr). This product is lead free and compliant with RoHS.

Features

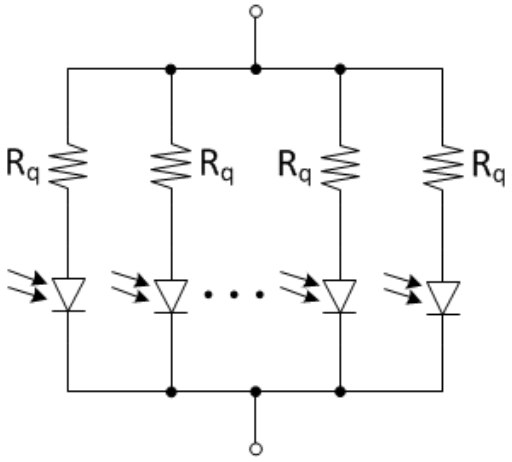
- High PDE
- Four-side tileable
- Highly transparent glass protection layer
- Operating temperature range from –20°C to +50°C
- RoHS and REACH compliant

Applications

- X-ray and gamma ray detection
- Nuclear medicine
- Positron emission tomography
- Safety and security
- Physics experiments

Block Diagram

Figure 1: AFBR-S4N44P163 Block Diagram of Single SiPM Element

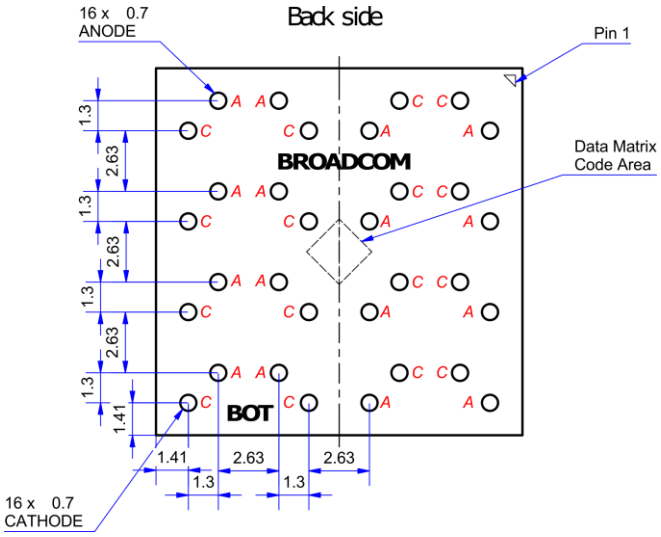


Pad Layout

The AFBR-S4N44P163 has 32 signal pins.

The anode and the cathode of each SiPM chip can be connected separately. The cathodes do not have a common connection on the module. The pad layout is shown in Figure 2.

Figure 2: Pad Layout



NOTE:

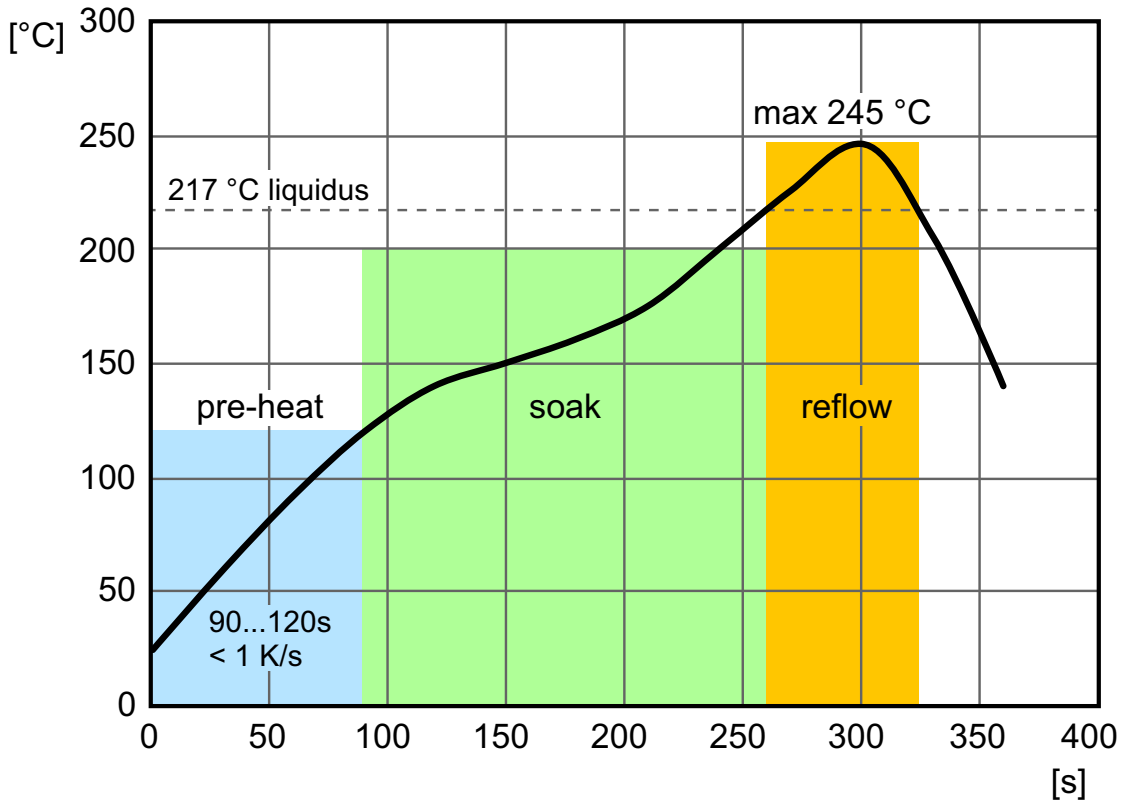
1. Dimensions: mm.
2. A stands for anode, C stands for cathode.

Regulatory Compliance Table

Feature	Test Method	Performance
Electrostatic discharge (ESD) to the electrical pins, Human Body Model (contact ESD)	JESD22-A114	Refer to Absolute Maximum Ratings (2 kV)
Electrostatic discharge (ESD) to the electrical pins, Charged Device Model	JESD22-C101F	Refer to Absolute Maximum Ratings (500V)
Storage compliance MSL	J-STD-020D	3 (168 hours floor life time)
Restriction of hazardous substances directive	RoHS Directive 2011/65/EU Annex II	Certified compliant

Reflow Soldering Diagram

Figure 3: Recommended Reflow Soldering Profile



Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause damage to the devices. Limits apply to each parameter in isolation. Absolute maximum ratings are those values beyond which damage to the device may occur if these limits are exceeded for other than a short period of time.

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_{STG}	–20	+60	°C
Operating Temperature[a]	T_A	–20	+50	°C
Soldering Temperature[b, c]	T_{SOLD}	—	245	°C
Lead Soldering Time[b, c]	t_{SOLD}	—	60	s
Electrostatic Discharge Voltage Capability HBM	ESD_{HBM}	—	2	kV
Electrostatic Discharge Voltage Capability CDM	ESD_{CDM}	—	500	V
Operating Over Voltage	V_{OV}	—	12	V

a. Biased at constant voltage = 5V above breakdown.

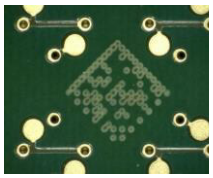
b. The tile is reflow solderable according to the solder diagram shown in Figure 3.

c. According to JEDEC J-STD-020D, the moisture sensitivity classification is MSL3.

Device Identification

Each device can be identified and tracked by a unique Data Matrix code (DMC) on the back of the PCB. The code is structured as follows: YYWWNNNNNN (Y – year, W – week, N – running number). An example DMC is shown in Figure 4.

Figure 4: Example Data Matrix Code for Tile Identification



Single Device Specification

Features measured at 20°C unless otherwise specified.

Geometric Features

Parameter	Symbol	Value	Units
Single device area	DA	3.88 × 3.88	mm^2
Active area	AA	3.72 × 3.72	mm^2
Micro cell pitch	L_{cell}	30	µm
Number of micro cells	N_{cells}	15060	
Fill factor	FF	70	%

Optical and Electrical Features

Two recommended working points: "Typical" (“Typ.”) for general purpose applications and "Performance" (“Perf.” for best timing performance.

Parameter	Symbol	Min.	Typ.[a]	Max.	Perf.[a]	Units	Reference Plots
Spectral range	λ	300	—	900	—	nm	Figure 5
Peak sensitivity wavelength	λ_{PK}	—	420	—	—	nm	Figure 5
Photo detection efficiency[b]	PDE	—	43	—	54	%	Figure 6
Dark current	I_D	—	0.4	—	2.5	µA	Figure 7
Dark count rate[c]	DCR	—	1.1	—	2.3	MHz	Figure 8, Figure 11
Dark count rate per unit area	DCR_{mm2}	—	77	—	170	kHz/mm^2	
Gain	G	—	1.6	—	3.1	× 10^6	Figure 9, Figure 12
Optical crosstalk	P_{Xtalk}	—	9	—	25	%	Figure 10, Figure 13
After pulsing probability	P_{AP}	—	<1	—	1	%	Figure 10, Figure 13
Recharge time constant[d]	τ_{fall}	—	55	—	50	ns	Figure 15
Breakdown voltage	V_{BD}	—	26.8	—	—	V	Figure 6
Overvoltage	V_{OV}	—	3.0	—	6.5	V	
Nominal terminal capacitance[e]	C_T	—	610	—	540	pF	
Temperature coefficient of breakdown voltage (23…27°C)	$\Delta V_{BR}/\Delta T$	—	25	—	25	mV/K	
Temperature coefficient of gain (23…27°C)[f]	$\Delta G/\Delta T$	—	1.2	—	0.9	× 10^4/K	

a. Typical values are measured at 3V above breakdown, performance at 6.5V above breakdown.

b. Measured at peak sensitivity wavelength. Measurement does not include correlated noise, such as after-pulsing or optical cross-talk.

c. Measured at 0.5 p.e. amplitude. Measurement does not include delayed correlated events.

d. Measured on 1 × 1 mm^2 devices with an input impedance of 20Ω.

e. Measured using input sine wave with f = 100 kHz and V_{in} = 100 mV.

f. Calculated from gain dependence on V and breakdown voltage temperature coefficient: $dG/dT = dG/dV \times dV_{Bd}/dT$.

Reference Plots

Features measured at 20°C unless otherwise specified.

Figure 5: Typical PDE vs. Wavelength

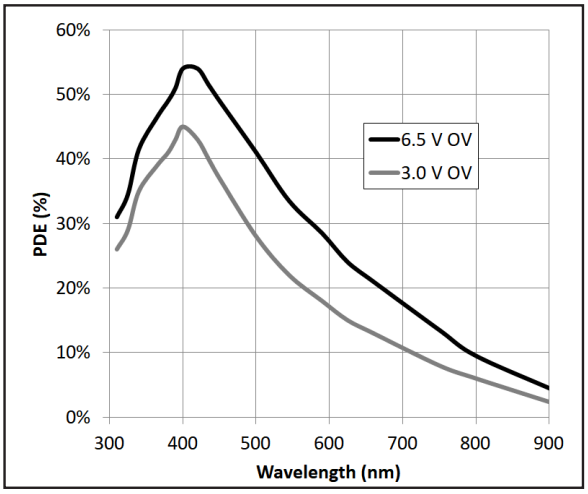


Figure 6: Typical PDE at Peak λ vs. OV

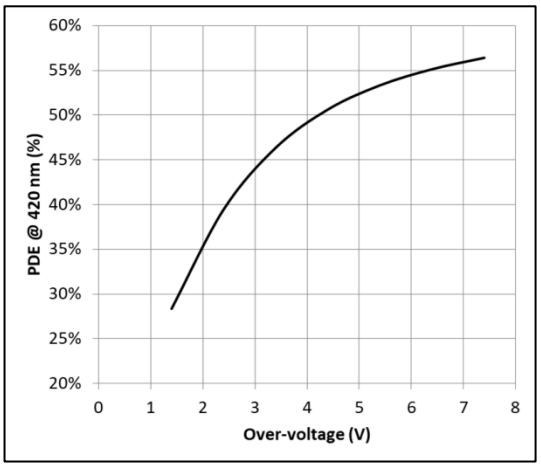


Figure 7: Typical Reverse IV Curve[1]

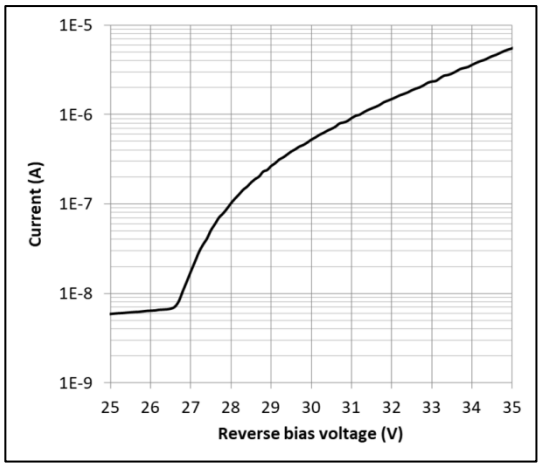
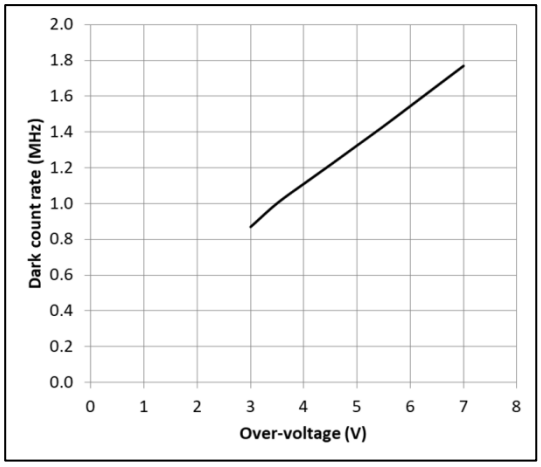


Figure 8: Typical Dark Count Rate vs. OV[1]



1. Measured on a single SiPM.

Figure 9: Typical Gain vs. OV

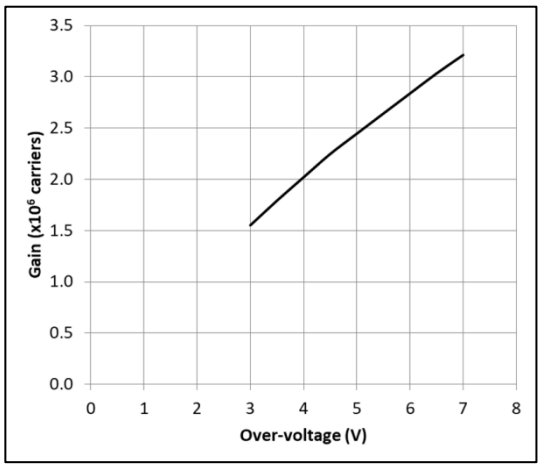


Figure 10: Typical Correlated Noise vs. OV

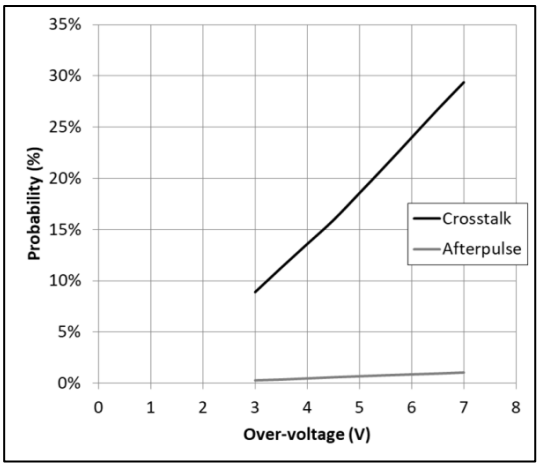


Figure 11: Typical Dark Count Rate vs. PDE at Peak λ

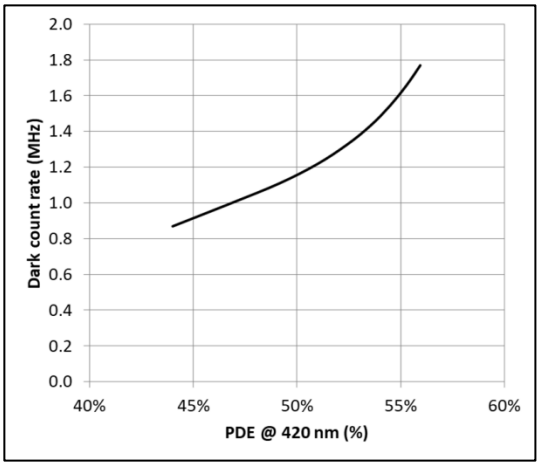


Figure 12: Typical Gain vs. PDE at Peak λ

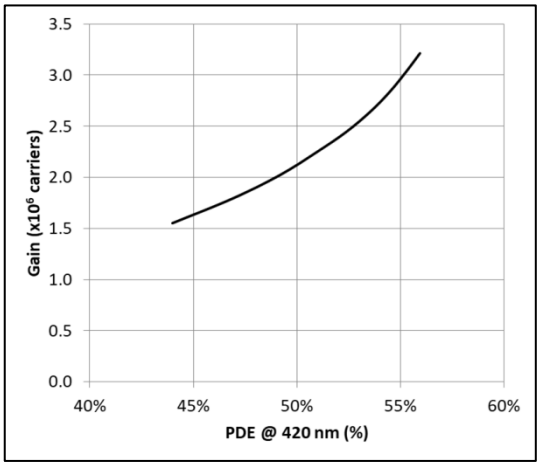


Figure 13: Typical Correlated Noise vs. PDE at Peak λ

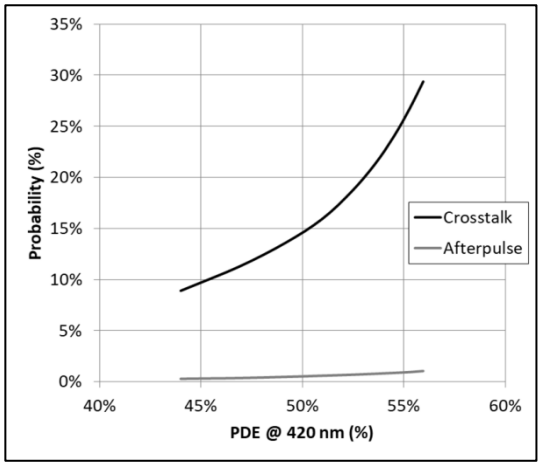
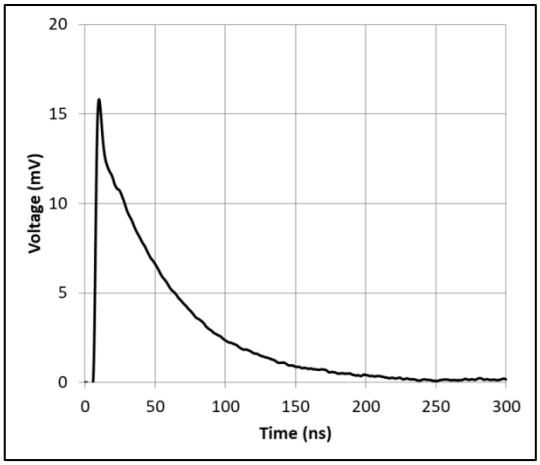


Figure 14: Typical Example Signal Measured at 3V OV



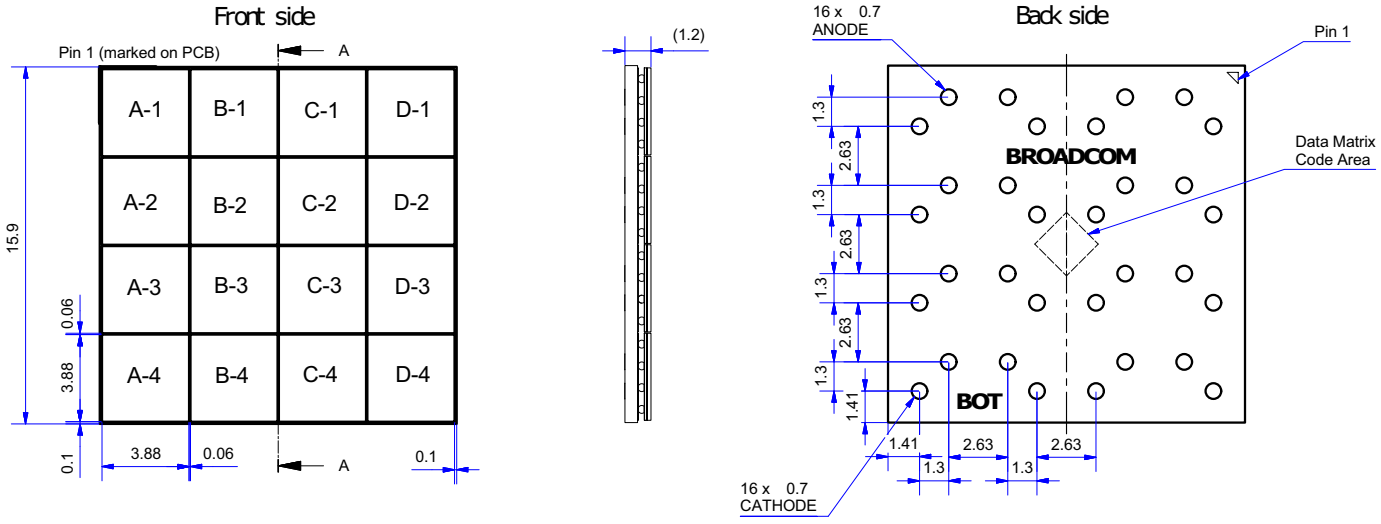
Array Specification

Two recommended operating voltages: "Typical" (“Typ.”) for general purpose applications and "Performance" (“Perf.”) for best timing performance.

Parameter	Symbol	Min.	Typ.	Max.	Perf.	Units	Reference Plot
Number of SiPMs per array		16			—		
Array arrangement		4 × 4 chips			—		
Package fill factor		95			—	%	
Breakdown voltage spread	ΔV_{BD}	—	200	—	—	mV	
Dark current sum	ΣI_{DK}	—	22	—	100	µA	

Mechanical Data – Package Outline

Figure 15: Package Outline Drawing. Dimensions in mm, numbers rounded to two decimal places.



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