DATA SHEET

74AVC16373; 74AVCH16373
16-bit D-type transparent latch; 3-state

Objective specification
File under Integrated Circuits, IC24

1998 Dec 11

Philips Semiconductors

PHILIPS

16-bit D-type transparent latch; 3-state

74AVC16373; 74AVCH16373

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **Complies with JEDEC standard no. 8-1A/5/7**
- **CMOS low power consumption**
- **Input/Output tolerant up to 3.6 V**
- **DCO (Dynamic Controlled Output) Circuit dynamically changes output impedance, resulting in noise reduction without speed degradation**
- **Low inductance multiple V_{CC} and GND pins for minimize noise and ground bounce.**
- **All data inputs have bushold. (only 74AVCH16373)**
- **Power off disables 74AVC16373; 74AVCH16373 outputs, permitting Live Insertion.**

DESCRIPTION

The 74AVC(H)16373 is a 16-bit D-type transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. Incorporates bushold data inputs which eliminate the need for external pull-up resistors to hold unused inputs. One latch enable(LE) input and one enable $\overline{OE}$ are provided per 8-bit section.

This product is designed to have an extremely fast propagation delay and a minimum amount of power consumption.

To ensure the high-impedance output state during power up or power down, $\overline{OE}_n$ should be tied to V_{CC} through a pullup resistor (Live insertion).

A Dynamic Controlled Output (DCO) circuitry is implemented to support termination line drive during transient. See graphs at this page for typical curves.

The 74AVCH16373 consist of 2 sections of eight D-type transparant latches with 3-State true outputs.

QUICK REFERENCE DATA

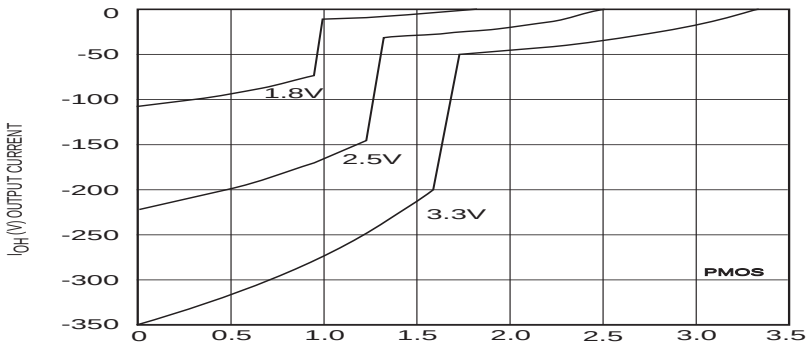
GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.0$ ns; C_L = 30 pF.

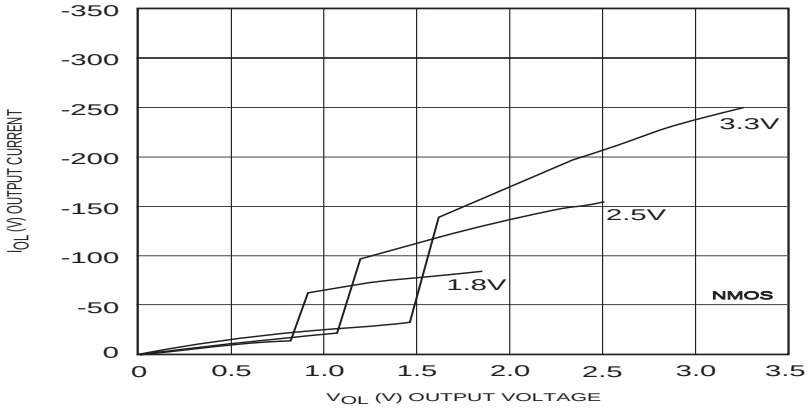
SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/ t_{PLH}	propagation delay D_n to Q_n	V_{CC} = 1.8 V	1.6	ns
		V_{CC} = 2.5 V	1.3	ns
		V_{CC} = 3.3 V	1.1	ns
t_{PHL}/ t_{PLH}	propagation delay LE to Q_n	V_{CC} = 1.8 V[3]	1.7	ns
		V_{CC} = 2.5 V[3]	1.4	ns
		V_{CC} = 3.3 V[3]	1.2	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2		
		outputs enabled	22	pF
		output disabled	5	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.
3. For type with bushold.





FUNCTION TABLE

See Note 1.

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUT
	$\overline{OE}$	LE	Dn		nY
enable and read register	L	H	L	L	L
(Transparent mode)	L	H	H	H	H
latch and read register	L	L	L	L	L
(Hold mode)	H	H	h	H	H
latch register and disable outputs	H	L	I	L	Z
	H	L	h	H	Z

Note

1. H - HIGH voltage level;
   h - HIGH voltage level one set-up time prior to the HIGH-to-LOW LO transition;
   L - LOW voltage level;
   l - LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition;
   X- don't care;
   Z - high impedance OFF-state.

ORDERING AND PACKAGE INFORMATION

OUTSIDE NORTH AMERICA	NORTH AMERICA	PACKAGES				
		TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74AVC16373DGG		–40 to +85 °C	48	TSSOP	plastic	SOT362-1
74AVCH16373DGG		–40 to +85 °C	48	TSSOP	plastic	SOT362-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	1$\overline{OE}$	Output enable input (active LOW)
2, 3, 5, 6, 8, 9, 11 and 12	$1Q_0$ to 1Q7	Data outputs
4, 10, 15, 21, 28, 34, 39 and 45	GND	Ground (0 V)
7,18, 31 and 42	V_{CC}	Positive supply voltage
13, 14, 16, 17, 19, 20, 22 and 23	2Q0 to 2Q7	Data outputs
24	2$\overline{OE}$	Output enable input (active LOW)
25	2LE	Latch enable input (active HIGH)
36, 35, 33, 32, 30, 29, 27 and 26	$2D_0$ to 2D7	Data inputs
47, 46, 44, 43, 41, 40, 38 and 37	$1D_0$ to $1D_7$	Data inputs
48	1LE	Latch enable input (active HIGH)

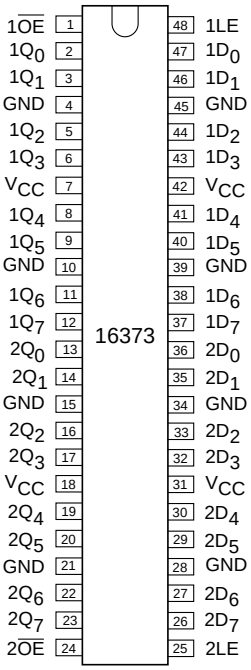


Fig.1 Pin configuration.

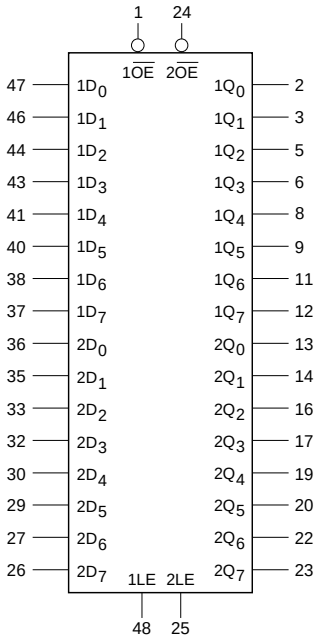


Fig.2 Logic symbol.

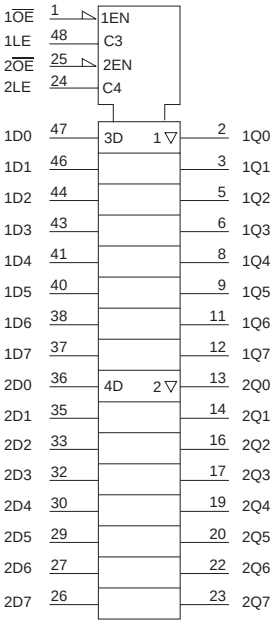


Fig.3 IEEE/IEC logic symbol

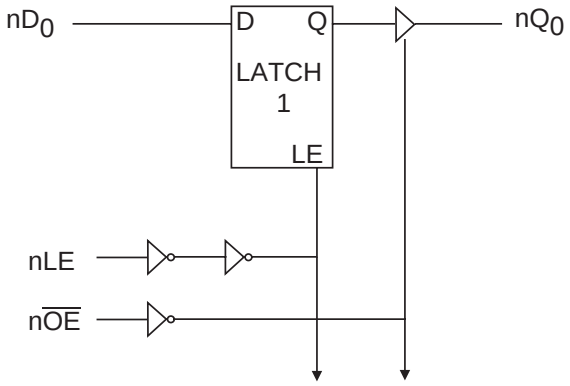


Fig.4 Logic Diagram.

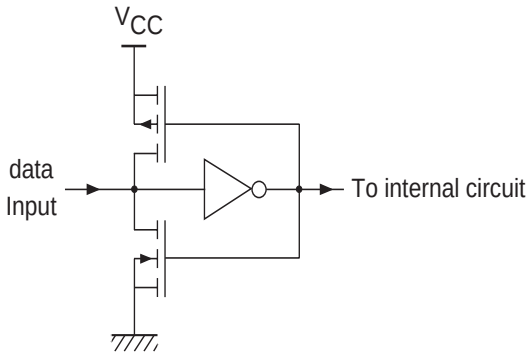


Fig.5 Bushold circuit.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage				
	According JEDEC Low Voltage Standards		1.65	1.95	V
			2.3	2.7	V
			3.0	3.6	V
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC input voltage range		0	3.6	V
V_O	DC output voltage range; output 3-state		0	3.6	V
V_O	DC output voltage range; output High or Low state		0	V_{CC}	V
T_{amb}	operating ambient temperature range	in free air	–40	+85	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.65 to 2.3 V	0	30	ns/V
		V_{CC} = 2.3 to 3.0 V	0	20	ns/V
		V_{CC} = 3.0 to 3.6 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage		–0.5	+4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–	–50	mA
V_I	DC input voltage	for inputs; note 1	–0.5	4.6	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	–	±50	mA
V_O	DC output voltage; output High or Low state	note 1	–0.5	V_{CC} + 0.5	V
V_O	DC output voltage; output 3-state	note 1	–0.5	4.6	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	–	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature range		–65	+150	°C
P_{tot}	power dissipation per package	for temperature range: –40 to +125 °C			
	plastic thin-medium-shrink (TSSOP)	above +55 °C derate linearly with 8 mW/K	–	600	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	T_{amb} = −40 TO +85 °C			UNIT	TEST CONDITIONS		
		MIN.	TYP.(1)	MAX.		V_{CC} (V)	V_I (V)	OTHER
V_{IH}	HIGH level input voltage	V_{CC}	–	–	V	1.2		
		$0.65V_{CC}$	0.9	–	V	1.65 to 1.95		
		1.7	1.2	–	V	2.3 to 2.7		
		2.0	1.5	–	V	3.0 to 3.6		
V_{IL}	LOW level input voltage	–	–	GND	V	1.2		
		–	0.9	$0.35V_{CC}$	V	1.65 to 1.95		
		–	1.2	0.7	V	2.3 to 2.7		
		–	1.5	0.8	V	3.0 to 3.6		
V_{OH}	HIGH level output voltage	V_{CC}–0.20	V_{CC}	–	V	1.65 to 3.6	V_{IH} or V_{IL}	I_O = –100 µA
		V_{CC}–0.45	V_{CC}–0.10	–	V	1.65		I_O = –4 mA
		V_{CC}–0.55	V_{CC}–0.28	–	V	2.3		I_O = –8 mA
		V_{CC}–0.70	V_{CC}–0.32	–	V	3.0		I_O = –12 mA
V_{OL}	LOW level output voltage	–	GND	0.20	V	1.65 to 3.6	V_{IH} or V_{IL}	I_O = 100 µA
		–	0.10	0.45	V	1.65		I_O = 4 mA
		–	0.26	0.55	V	2.3		I_O = 8 mA
		–	0.36	0.70	V	3.0		I_O = 12 mA
I_I	input leakage current per pin	–	0.1	2.5	µA	1.65 to 3.6	V_{CC} or GND	
I_{OFF}	power off leakage current	–	0.1	±10	µA	0		V_I or V_O = 3.6
I_{IHZ}/I_{ILZ}	input current for common I/O pins	–	0.1	12.5	µA	1.65 to 3.6	V_{CC} or GND	
I_{OZ}	3-state output OFF–state current	–	0.1	5	µA	1.65 to 2.7	V_{IH} or V_{IL}	V_O = V_{CC} or GND
		–	0.1	10	µA	3.0 to 3.6		
I_{CC}	quiescent supply current	–	0.1	20	µA	1.65 to 2.7	V_{CC} or GND	I_O = 0
		–	0.2	40	µA	3.0 to 3.6		

Note

1. All typical values are measured at T_{amb} = 25 °C.

OPTIONAL: BUSHOLD SPECIFICATION FOR 74AVCH16373 ONLY

DC CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	T_{amb} = −40 TO +85 °C			UNIT	TEST CONDITIONS		
		MIN.	TYP.(1)	MAX.		V_{CC} (V)	V_I (V)	OTHER
I_{BHL}	bushold LOW sustaining current	25	–	–	µA	1.65	$0.35V_{CC}$	see note 2.
		45	–	–	µA	2.3	0.7 V	
		75	–	–	µA	3.0	0.8 V	

SYMBOL	PARAMETER	T_{amb} = −40 TO +85 °C			UNIT	TEST CONDITIONS		
		MIN.	TYP.(1)	MAX.		V_{CC} (V)	V_I (V)	OTHER
I_{BHH}	bushold HIGH sustaining current	−25	–	–	µA	1.65	$0.65V_{CC}$	see note 2.
		−45	–	–	µA	2.3	1.7 V	
		−75	–	–	µA	3.0	2.0 V	
I_{BHLO}	bushold LOW overdrive current	200	–	–	µA	1.95		see note 2.
		300	–	–	µA	2.7		
		450	–	–	µA	3.6		
I_{BHHO}	bushold HIGH overdrive current	−200	–	–	µA	1.95		see note 2.
		−300	–	–	µA	2.7		
		−450	–	–	µA	3.6		

Note

1. All typical values are measured at T_{amb} = 25 °C.
2. Valid for data inputs of bushold parts.

AC CHARACTERISTICS 74AVC16373

GND = 0 V; $t_r = t_f \leq 2.0$ ns; $C_L = 30$ pF.

SYMBOL	PARAMETER	T_{amb} = −40 to +85 °C			UNIT	TEST CONDITIONS	
		MIN.	TYP.(1)	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay nD_n to nY_n	1.6	2.6	4.8	ns	1.2	see Fig.6, Fig.10
		0.9	1.7(2)	3.5	ns	1.65 to 1.95	
		0.8	1.3(2)	2.2	ns	2.3 to 2.7	
		0.7	1.1(2)	1.9	ns	3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay nLE to nY_n	1.6	2.8	5.0	ns	1.2	see Fig.7, Fig.10
		0.9	1.7(2)	3.6	ns	1.65 to 1.95	
		0.8	1.4(2)	2.3	ns	2.3 to 2.7	
		0.7	1.2(2)	2.0	ns	3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}_n$ to nY_n	–	5.0	–	ns	1.2	see Fig.9, Fig.10
		1.6	3.0(2)	5.5	ns	1.65 to 1.95	
		1.3	2.1(2)	4.5	ns	2.3 to 2.7	
		1.2	1.8(2)	4.0	ns	3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}_n$ to nY_n	–	5.0	–	ns	1.2	see Fig.9, Fig.10
		2.2	3.5(2)	5.0	ns	1.65 to 1.95	
		1.1	1.8(2)	4.0	ns	2.3 to 2.7	
		1.2	1.8(2)	3.5	ns	3.0 to 3.6	
t_W	nLE pulse width HIGH	3.3	–	–	ns	1.2	see Fig.8, Fig.10
		2.0	–	–	ns	1.65 to 1.95	
		1.6	–	–	ns	2.3 to 2.7	
		1.4	–	–	ns	3.0 to 3.6	
t_{SU}	Set-up time nDn to nLE	0.5	–	–	ns	1.2	see Fig.8, Fig.10
		0.3	–	–	ns	1.65 to 1.95	
		0.2	–	–	ns	2.3 to 2.7	
		0.1	–	–	ns	3.0 to 3.6	
t_h	hold time nDn to nLE	0.5	–	–	ns	1.2	see Fig.8, Fig.10
		0.3	–	–	ns	1.65 to 1.95	
		0.2	–	–	ns	2.3 to 2.7	
		0.1	–	–	ns	3.0 to 3.6	

Note

1. All typical values are measured at T_{amb} = 25 °C.
2. Typical value is measured at V_{CC} = 1.8 V,V_{CC} = 2.5 V,V_{CC} = 3.3 V.

AC CHARACTERISTICS 74AVCH16373

GND = 0 V; $t_r = t_f \leq 2.0$ ns; $C_L = 30$ pF.

SYMBOL	PARAMETER	T_{amb} = −40 to +85 °C			UNIT	TEST CONDITIONS	
		MIN.	TYP.(1)	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay nA_n to nY_n	1.6	2.6	4.9	ns	1.2	see Fig.6, Fig.10
		0.9	1.7(2)	3.6	ns	1.65 to 1.95	
		0.8	1.3(2)	2.3	ns	2.3 to 2.7	
		0.7	1.1(2)	2.0	ns	3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay nLE to nY_n	1.6	2.8	5.0	ns	1.2	see Fig.7, Fig.10
		0.9	1.7(2)	3.6	ns	1.65 to 1.95	
		0.8	1.4(2)	2.3	ns	2.3 to 2.7	
		0.7	1.2(2)	2.0	ns	3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}_n$ to nY_n	–	5.0	–	ns	1.2	see Fig.9, Fig.10
		1.6	3.0(2)	5.5	ns	1.65 to 1.95	
		1.3	2.1(2)	4.5	ns	2.3 to 2.7	
		1.2	1.8(2)	4.0	ns	3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}_n$ to nY_n	–	5.0	–	ns	1.2	see Fig.9, Fig.10
		2.2	3.5(2)	5.0	ns	1.65 to 1.95	
		1.1	1.8(2)	4.0	ns	2.3 to 2.7	
		1.2	1.8(2)	3.5	ns	3.0 to 3.6	
t_W	nLE pulse width HIGH	3.3	–	–	ns	1.2	see Fig.8, Fig.10
		2.0	–	–	ns	1.65 to 1.95	
		1.6	–	–	ns	2.3 to 2.7	
		1.4	–	–	ns	3.0 to 3.6	
t_{SU}	Set-up time nDn to nLE	0.5	–	–	ns	1.2	see Fig.8, Fig.10
		0.3	–	–	ns	1.65 to 1.95	
		0.2	–	–	ns	2.3 to 2.7	
		0.1	–	–	ns	3.0 to 3.6	
t_h	hold time nDn to nLE	0.5	–	–	ns	1.2	see Fig.8, Fig.10
		0.3	–	–	ns	1.65 to 1.95	
		0.2	–	–	ns	2.3 to 2.7	
		0.1	–	–	ns	3.0 to 3.6	

Note

1. All typical values are measured at T_{amb} = 25 °C.
2. Typical value is measured at V_{CC} = 1.8 V,V_{CC} = 2.5 V,V_{CC} = 3.3 V.

AC WAVEFORMS

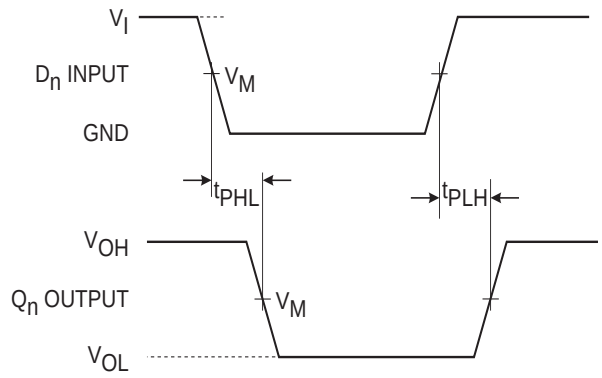


Fig.6 The input (D_n) to output (Q_n) propagation delay.

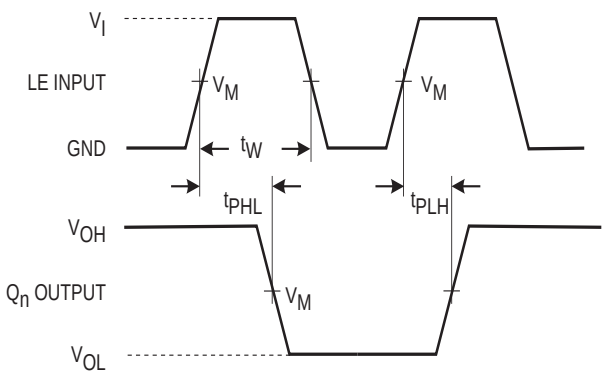


Fig.7 The latch enable input (LE) pulse widt, the latch enable input to output (Q_n) propagation delays

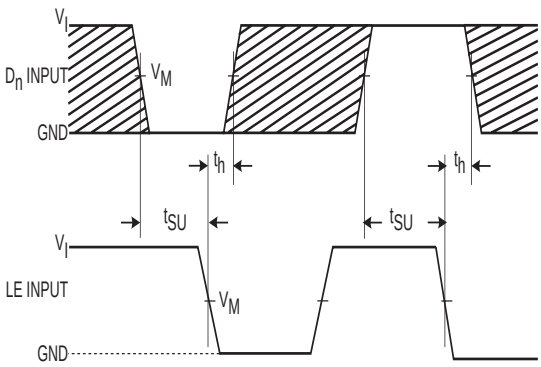


Fig.8 The data set-up time and hold times for the D_n input to the LE input

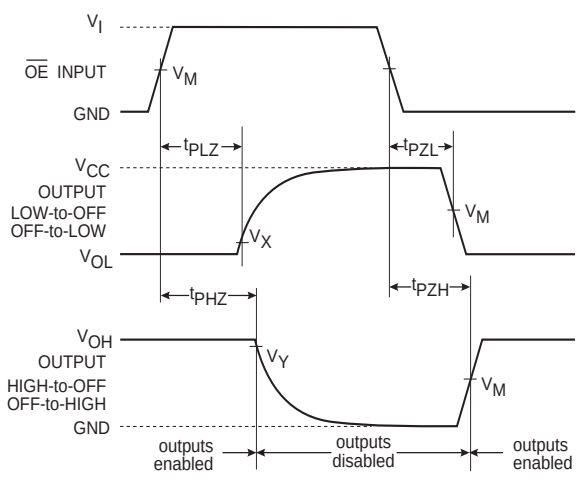
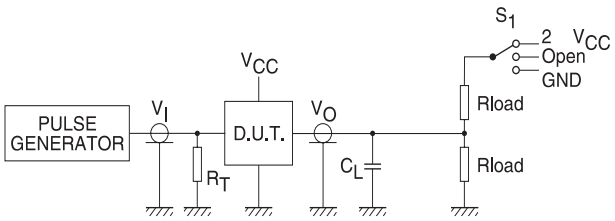


Fig.9 The 3-state enable and disable times.



TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I	R_{LOAD}
< 2.3 V	V_{CC}	1000Ω
2.3 - 2.7 V	Vcc	500Ω
3.0 - 3.6 V	2.7 V	500Ω

Fig.10 Load circuitry for switching times.

NOTES: V_{CC} = 2.3 TO 2.7 V RANGE AND V_{CC} < 2.3 V

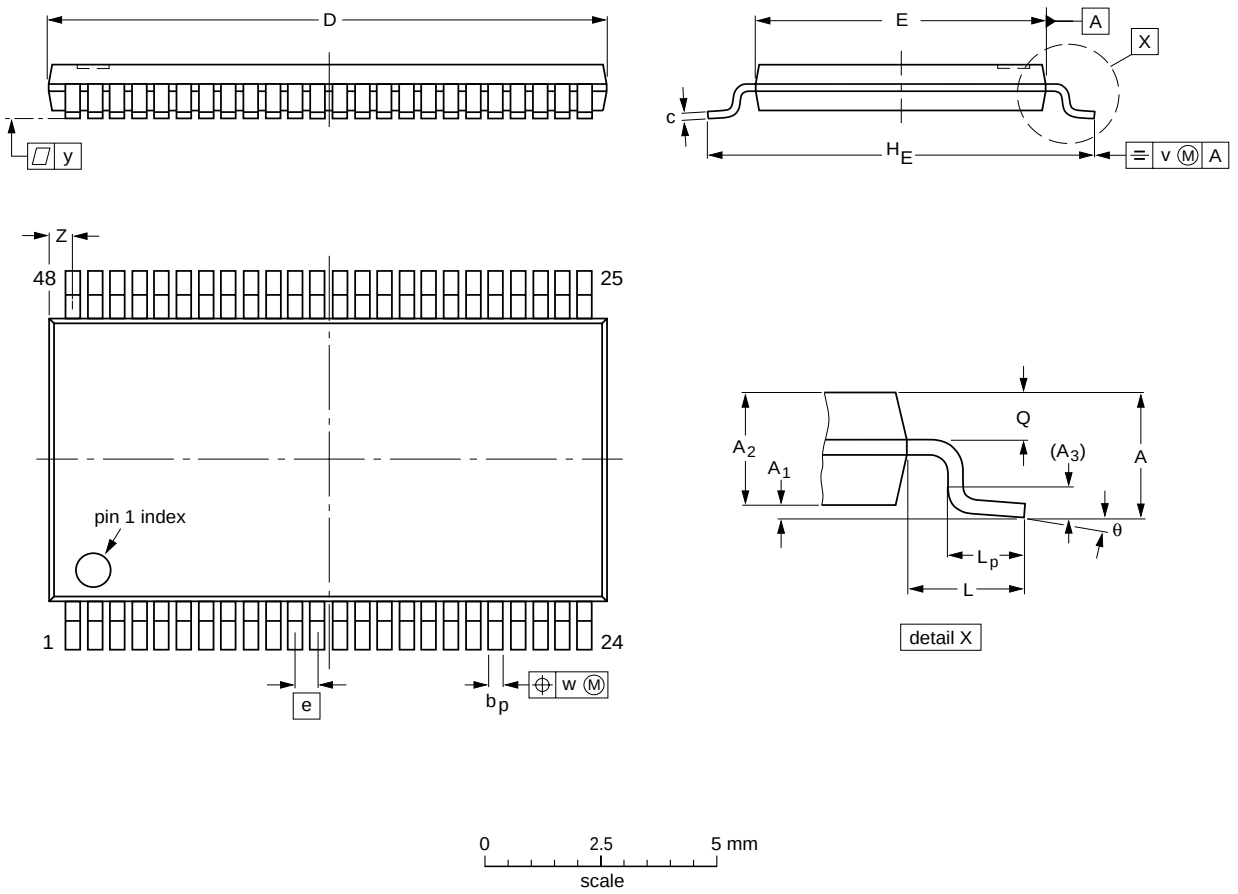
1. $V_M = 0.5V_{CC}$
2. $V_X = V_{OL}$ + 150 mV
3. $V_Y = V_{OH}$ - 150 mV
4. $V_I = V_{CC}$
5. V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

NOTES: V_{CC} = 3.0 TO 3.6 V RANGE

1. $V_M = 0.5V_{CC}$
2. $V_X = V_{OL}$ + 300 mV
3. $V_Y = V_{OH}$ - 300 mV
4. V_I = 2.7 V
5. V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

PACKAGE OUTLINE

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	**0.2** **0.1**	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT362-1		MO-153ED					~~93-02-03~~ 95-02-10

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010,
Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax.+381 11 635 777

For all other countries apply to: Philips Semiconductors,
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,
5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com

Printed in The Netherlands 245112/00/01/pp13 Date of release: 1998 Dec 11 Document order number: 9397 750 04914

Let's make things better.

Philips Semiconductors

PHILIPS