1.5A Dual High Speed MOSFET Drivers

AS4426 / AS4427 / AS4428

FEATURES

- **High Peak Output Current . . . . . >1.5A**
- **Fast Switching . . . . . t_D = 40ns**
- **Wide Operating Range . . . . . 4.5V to 18V**
- **Matched Rise and Fall Times**
- **ESD Protected 4kV**

APPLICATIONS

- **Motor Controls**
- **Switch Mode Power Supplies**
- **Pulse Transformer Driver**
- **Class D Switching Amplifiers**

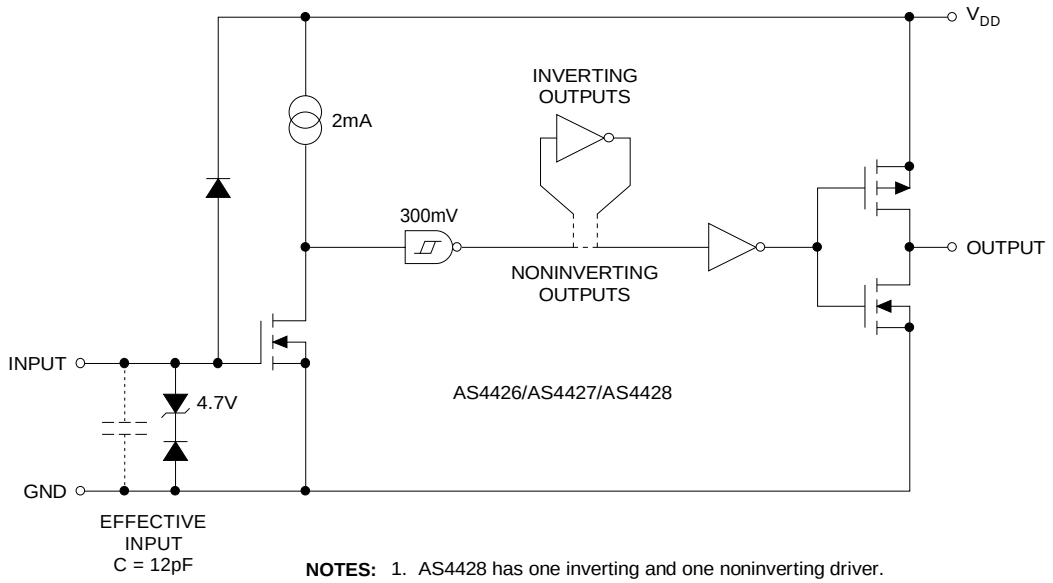
DESCRIPTION

The AS4426 series are dual CMOS drivers are designed to drive capacitive, resistive and inductive loads switching 1000pF gate capacitances in under 30ns while providing low impedances in both the ON and OFF states to insure the MOSFET's intended state will not be affected. All terminals are fully protected up to 4kV of ESD.

ORDERING INFORMATION

Part	Logic	Package	Temperature
AS4426P	Inverting	8 Pin PDIP	-40°C to 85°C
AS4426S	Inverting	8 Pin SOIC	-40°C to 85°C
AS4427P	Noninverting	8 Pin PDIP	-40°C to 85°C
AS4427S	Noninverting	8 Pin SOIC	-40°C to 85°C
AS4428P	Differential	8 Pin PDIP	-40°C to 85°C
AS4428S	Differential	8 Pin SOIC	-40°C to 85°C

FUNCTIONAL DIAGRAM



NOTES: 1. AS4428 has one inverting and one noninverting driver.
2. Ground any unused driver input.

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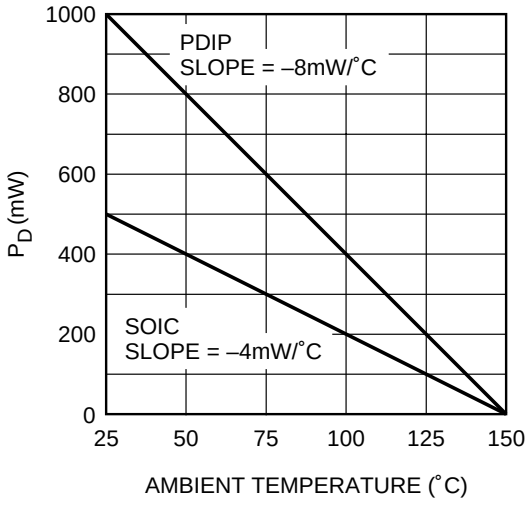
ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . +22V
Input Voltage, IN A or IN B . . . . . V_{DD}+0.3V to GND-5.0V
Maximum Chip Temperature . . . . . +150°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Package Thermal Resistance
PDIP $R_{\theta J-A}$ . . . . . 125°C/W
PDIP $R_{\theta J-C}$ . . . . . 42°C/W
SOIC $R_{\theta J-A}$ . . . . . 250°C/W
SOIC $R_{\theta J-C}$ . . . . . 75°C/W
Operating Temperature Range

Both Versions . . . . . -40°C to +85°C
Power Dissipation
Plastic 1000mW
SOIC 500mW

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE POWER DISSIPATION



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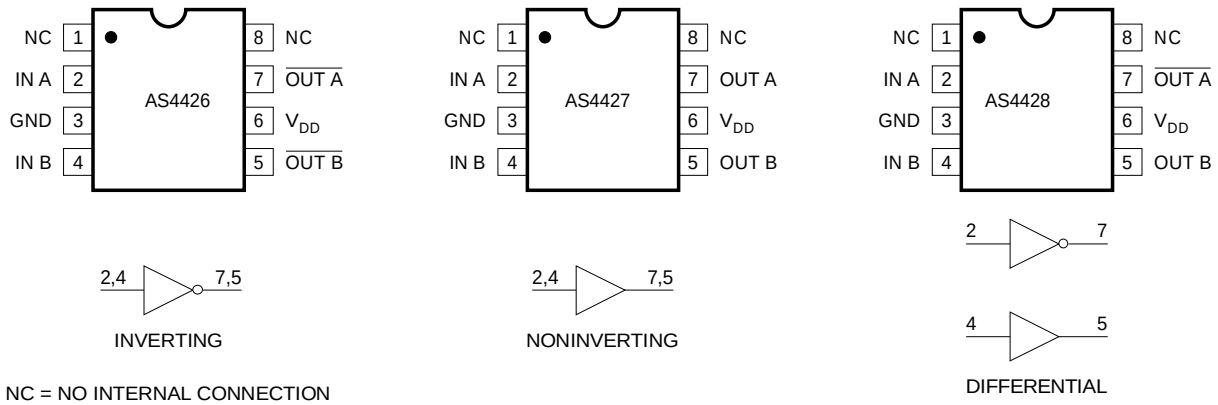
ELECTRICAL CHARACTERISTICS T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
INPUT						
V_{IH}	Logic 1 High Input Voltage	2.4	-	-	V	
V_{IL}	Logic 0 Low Input Voltage	-	-	0.8	V	
I_{IN}	Input Current	-1	-	1	µA	0V ≤ V_{IN} ≤ V_{DD}
OUTPUT						
V_{OH}	High Output Voltage	V_{DD}-0.025	-	-	V	
V_{OL}	Low Output Voltage	-	-	0.025	V	
R_O	Output Resistance	-	7	10	Ω	V_{DD} = 18V, I_O = 10mA
I_{PK}	Peak Output Current	-	1.5	-	A	
I_{REV}	Latch-Up Protection Withstand Reverse Current	>0.5	-	-	A	Duty Cycle ≤ 2% t ≤ 300µs
SWITCHING TIME (Note 1)						
t_R	Rise Time	-	25	30	ns	Figure 1
t_F	Fall Time	-	25	30	ns	Figure 1
t_{D1}	Delay Time	-	-	30	ns	Figure 1
t_{D2}	Delay Time	-	-	50	ns	Figure 1
POWER SUPPLY						
I_S	Power Supply Current	- -	- -	4.5 0.4	mA mA	V_{IN} = 3V (Both Inputs) V_{IN} = 0V (Both Inputs)

Note: 1. Switching times are guaranteed by design.

PIN CONFIGURATIONS



NOTE: SOIC pinout is identical to DIP.

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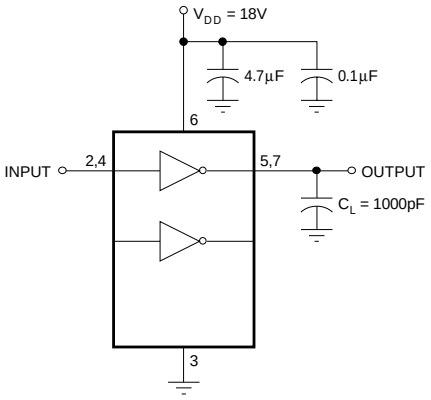
ELECTRICAL CHARACTERISTICS

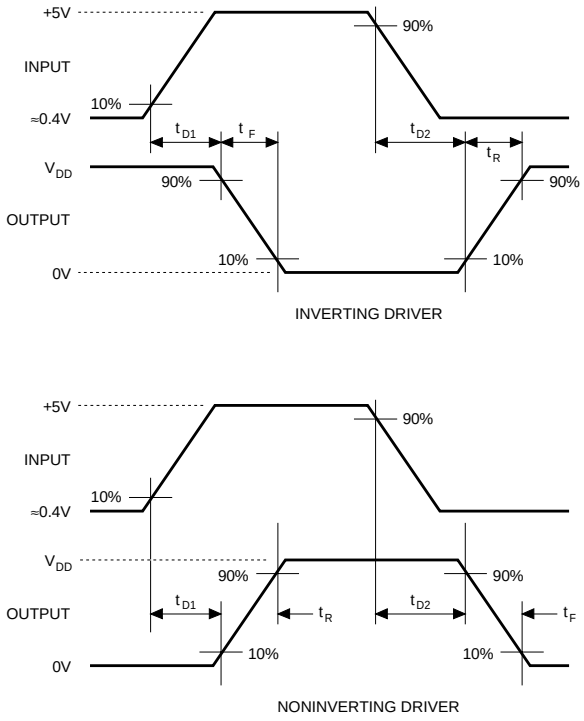
Specifications measured over temperature range with $4.5V \le V_{DD} \le 18V$, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
INPUT						
V_{IH}	Logic 1 High Input Voltage	2.4	-	-	V	
V_{IL}	Logic 0 Low Input Voltage	-	-	0.8	V	
I_{IN}	Input Current	-1	-	1	µA	$0V \le V_{IN} \le V_{DD}$
OUTPUT						
V_{OH}	High Output Voltage	V_{DD}-0.025	-	-	V	
V_{OL}	Low Output Voltage	-	-	0.025	V	
R_O	Output Resistance	-	9	12	Ω	V_{DD} = 18V, I_O = 10mA
I_{PK}	Peak Output Current	-	1.5	-	A	
I_{REV}	Latch-Up Protection Withstand Reverse Current	>0.5	-	-	A	Duty Cycle ≤ 2% t ≤ 300µs
SWITCHING TIME (Note 1)						
t_R	Rise Time	-	-	40	ns	Figure 1
t_F	Fall Time	-	-	40	ns	Figure 1
t_{D1}	Delay Time	-	-	40	ns	Figure 1
t_{D2}	Delay Time	-	-	60	ns	Figure 1
POWER SUPPLY						
I_S	Power Supply Current	- -	- -	8 0.6	mA mA	V_{IN} = 3V (Both Inputs) V_{IN} = 0V (Both Inputs)

Note: 1. Switching times are guaranteed by design.

FIGURE 1. SWITCHING TIME TEST CIRCUIT





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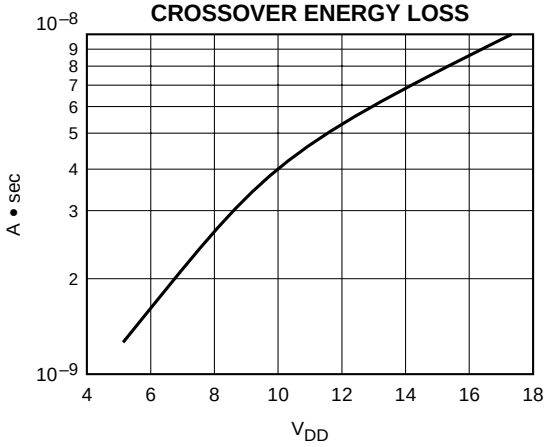
CROSSOVER ENERGY LOSS



NOTE: The values on this graph represent the loss seen by both drivers in a package during one complete cycle. For a single driver, divide the stated values by 2. For a single transition of a single driver, divide the stated value by 4.

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