

# DATA SHEET

## **BST100**

P-channel enhancement mode  
vertical D-MOS transistor

Product specification  
File under Discrete Semiconductors, SC13b

April 1995

# P-channel enhancement mode vertical D-MOS transistor

**BST100**

**DESCRIPTION**

P-channel vertical D-MOS transistor TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

**FEATURES**

- Very low  $R_{DS(on)}$
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

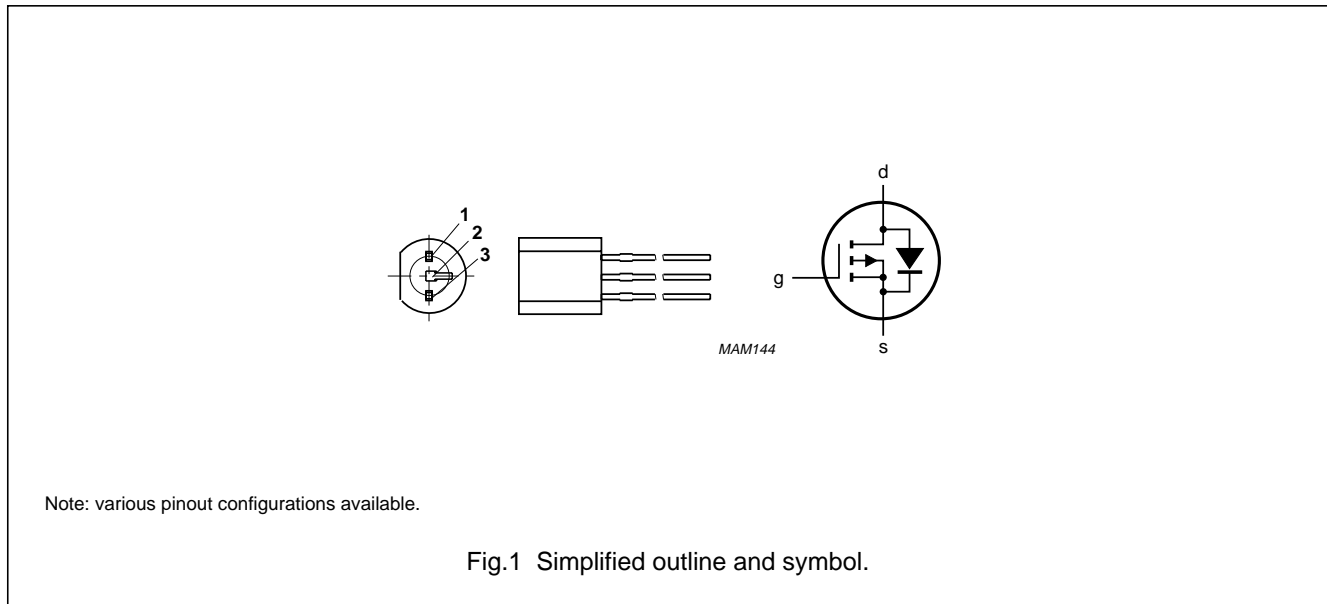
**QUICK REFERENCE DATA**

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.3 A
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	1 W
Drain-source ON-resistance $-I_D = 200\text{ mA}; -V_{GS} = 10\text{ V}$	$R_{DS(on)}$	typ.	4,5 $\Omega$
		max.	6 $\Omega$
Transfer admittance $-I_D = 200\text{ mA}; -V_{DS} = 15\text{ V}$	$ Y_{fs} $	typ.	200 mS

**PINNING - TO-92 VARIANT**

- 1 = source
- 2 = gate
- 3 = drain

**PIN CONFIGURATION**



## P-channel enhancement mode vertical D-MOS transistor

## BST100

### RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.3 A
Drain current (peak)	$-I_{DM}$	max.	0.8 A
Total power dissipation up to $T_{amb} = 25\text{ °C}$ (note 1)	$P_{tot}$	max.	1 W
Storage temperature range	$T_{stg}$		-65 to + 150 °C
Junction temperature	$T_j$	max.	150 °C

### THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j-a}$	=	125 K/W
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### Note

1. Transistor mounted on printed-circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

## P-channel enhancement mode vertical D-MOS transistor

### BST100

#### CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage

$-I_D = 10\text{ }\mu\text{A}; V_{GS} = 0$   $-V_{(BR)DSS}$  min. 60 V

Drain-source leakage current

$-V_{DS} = 48\text{ V}; V_{GS} = 0$   $-I_{DSS}$  max. 1  $\mu\text{A}$

Gate-source leakage current

$-V_{GS} = 20\text{ V}; V_{DS} = 0$   $-I_{GSS}$  max. 100 nA

Gate threshold voltage

$-I_D = 1\text{ mA}; V_{DS} = V_{GS}$   $-V_{GS(th)}$  min. 1.5 V  
max. 3.5 V

Drain-source ON-resistance

$-I_D = 200\text{ mA}; -V_{GS} = 10\text{ V}$   $R_{DS(on)}$  typ. 4.5  $\Omega$   
max. 6  $\Omega$

Transfer admittance

$-I_D = 200\text{ mA}; -V_{DS} = 15\text{ V}$   $|Y_{fs}|$  typ. 200 mS

Input capacitance at  $f = 1\text{ MHz}$

$-V_{DS} = 10\text{ V}; V_{GS} = 0$   $C_{iss}$  typ. 55 pF  
max. 70 pF

Output capacitance at  $f = 1\text{ MHz}$

$-V_{DS} = 10\text{ V}; V_{GS} = 0$   $C_{oss}$  typ. 30 pF  
max. 45 pF

Feedback capacitance at  $f = 1\text{ MHz}$

$-V_{DS} = 10\text{ V}; V_{GS} = 0$   $C_{rss}$  typ. 8 pF  
max. 12 pF

Switching times (see Figs 2 and 3)

$-I_D = 200\text{ mA}; -V_{DD} = 50\text{ V}; -V_{GS} = 0\text{ to }10\text{ V}$   $t_{on}$  typ. 4 ns  
 $t_{off}$  typ. 20 ns

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BST100

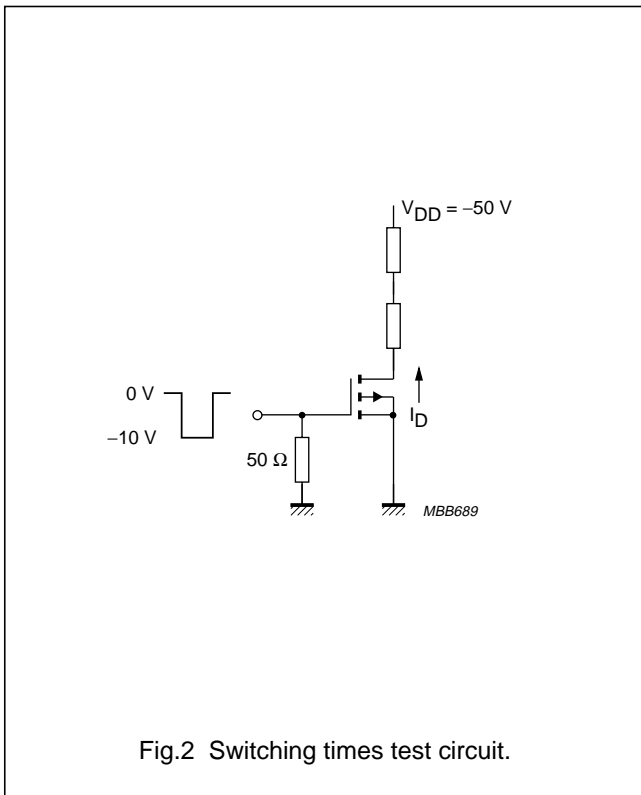


Fig.2 Switching times test circuit.

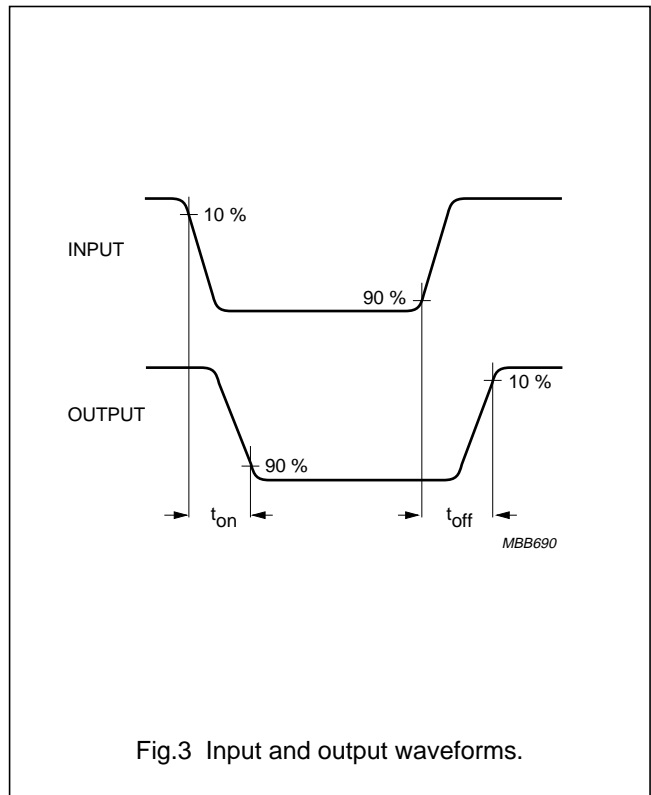


Fig.3 Input and output waveforms.

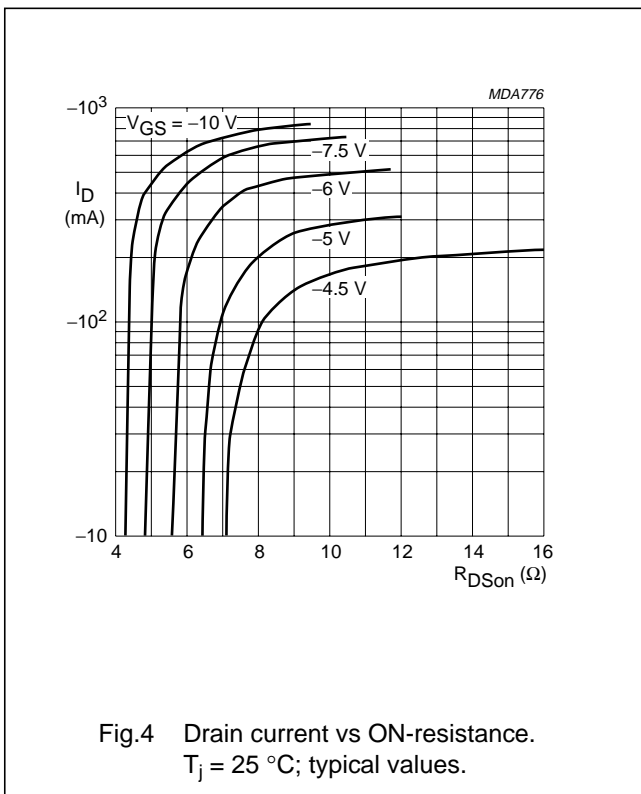


Fig.4 Drain current vs ON-resistance.  
 $T_j = 25\text{ }^\circ\text{C}$ ; typical values.

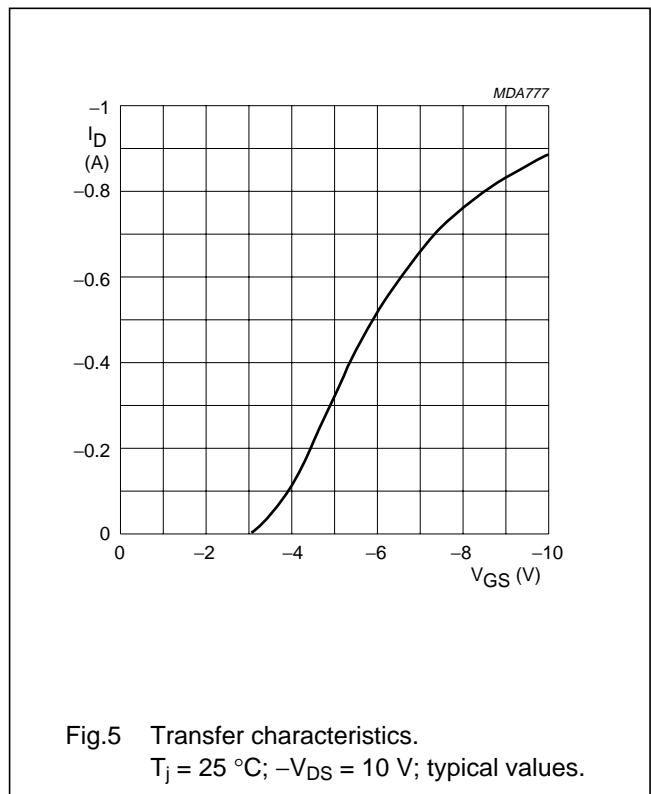
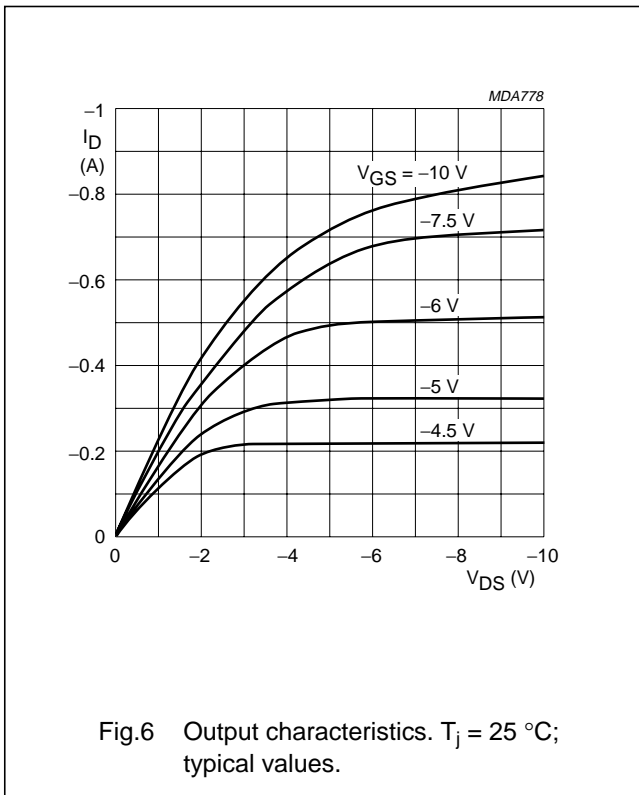


Fig.5 Transfer characteristics.  
 $T_j = 25\text{ }^\circ\text{C}$ ;  $-V_{DS} = 10\text{ V}$ ; typical values.

P-channel enhancement mode vertical  
D-MOS transistor

BST100



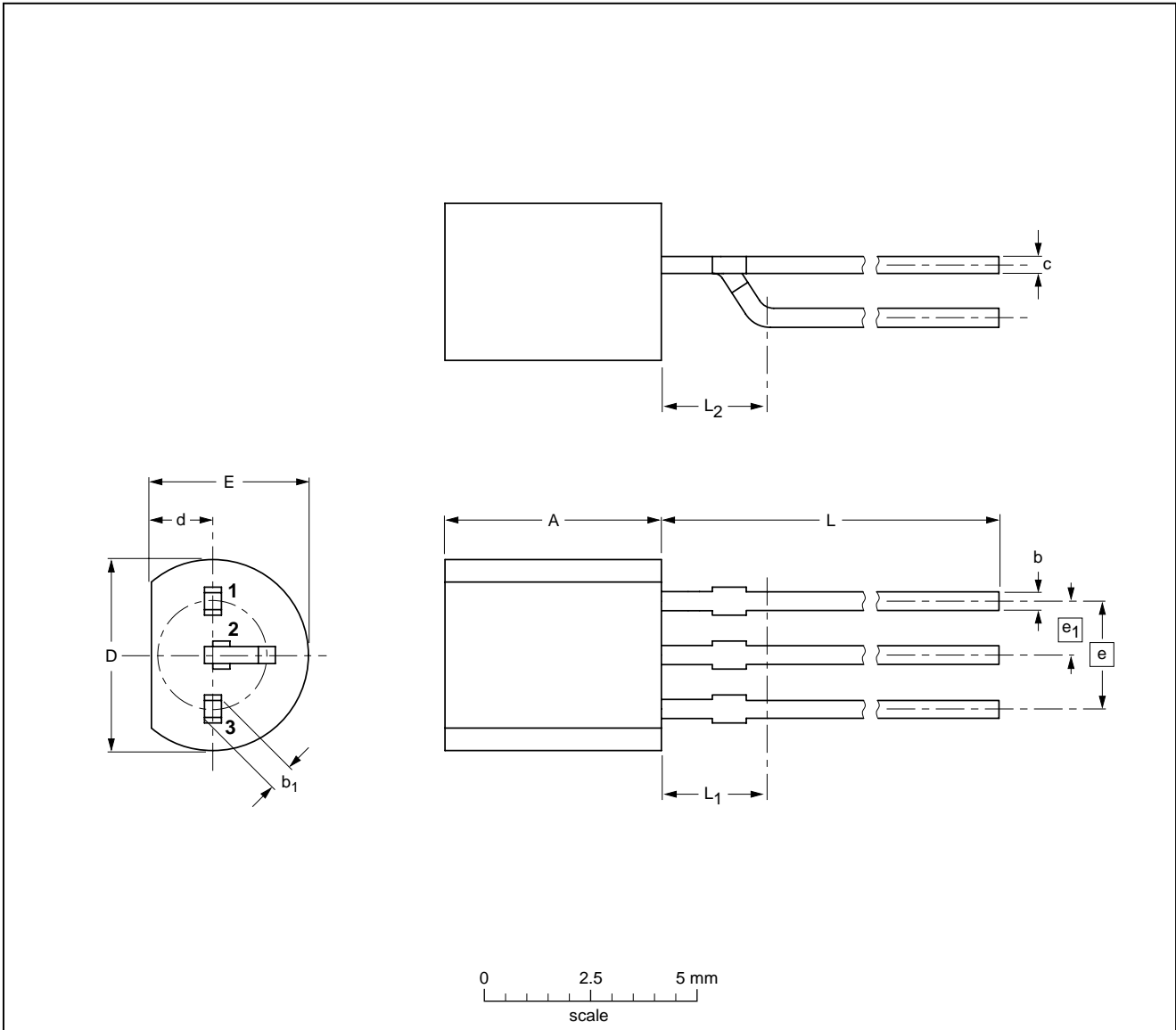
P-channel enhancement mode vertical  
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BST100

PACKAGE OUTLINES

Plastic single-ended leaded (through hole) package; 3 leads (on-circle)

SOT54 variant



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	$b_1$	c	D	d	E	e	$e_1$	L	$L_1^{(1)}$ max	$L_2$ max
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5	2.5

Notes

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT54 variant		TO-92	SC-43		97-04-14

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**BST100****DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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BST100

**NOTES**

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BST100

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P-channel enhancement mode vertical  
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**NOTES**

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