3-Phase + 1-Phase VR12/IMVP-7 PWM Control IC with Hypergear™ features IDTP63131/IDTP63133

DESCRIPTION

The IDTP63131/IDTP63133 is a dual output, step down Intel VR12/IMVP-7 compliant PWM controller for CPU and GPU core voltage regulation. The primary output (Rail 1) can be configured for 1 to 3 phase operation. The secondary output (Rail 2) provides single phase operation. In conjunction with IDTP67001, IDTP67002, IDTP67111 MOSFET drivers and external MOSFETs, the IDTP63131/IDTP63133 forms a complete core voltage regulator for Intel microprocessors.

Both rails use true differential output voltage and inductor DCR current sensing to improve load-line and current limit accuracy. The IDTP63131/IDTP63133 allows programmable per phase switching frequency from 200KHz to 1MHz with a single resistor which reduces the output filter size.The IDTP63133 is optimized for use with coupled inductors and has a reduced Rail1 switching frequency relative to Rail2. The IDTP63131/IDTP63133 uses voltage mode control for fast transient response with excellent PWM stability.

Both rails of the IDTP63131/IDTP63133 are fully compliant with Intel VR12/IMVP-7 serial VID (SVID) communication requirements. The IDTP63131/IDTP63133 satisfies static load-line (droop), load transient response and Dynamic VID specifications of a VR12/IMVP-7 voltage regulator. Dynamic Efficiency Control (DEC) enables all Rail 1 configured phases to operate when full current output is required and dynamically reduces the number of active phases at reduced output current levels.

IDT Proprietary Hypergear™ dynamic control features provide programmable scaling of CPU voltage and clock frequency to enable CPU performance and efficiency improvements. Complete Hypergear™ implementation includes an IDT SCPC (system clock power console) IC and related software.

An SMBus interface allows programming of IC configuration parameters and provides extensive diagnostic and operational telemetry data to the host system. The IDTP63131/IDTP63133 has output overvoltage protection (OVP), under voltage protection (UVP), over current protection (OCP), and over temperature protection (OTP) to ensure safe effective relaible operation of system. When any of these protection features detect a fault, the IDTP63131 shuts down the corresponding rail and informs the host system through telemetry. The IDTP63131/IDTP63133 is available in a 40-pin 5mm X 5mm QFN package with bottom metal paddle.

FEATURES

- Dual output Intel VR12/IMVP-7 serial VID compliant controller
- Satisfies static load-line,load transient and dynamic VID control functions of VR12/IMVP-7 specifications
- Programmable 1 to 3-phase count on Rail1 and single phase on Rail 2 to form CPU and GPU core voltage regulators
- IDTP63131 operates with discrete inductor and IDTP63133 operates with coupled inductor
- Resistor programmable, thermally compensated load-line (droop) current limit for each rail. Has both per phase current limit and total output current limit
- Resistor programmable per phase switching frequency from 200Khz to 1MHz for less output filter size and system efficiency
- True differential output voltage and loss less inductor DCR current sensing for accurate load-line and current limit
- Hypergear™ Dynamic Voltage Control (DVC) and Dynamic Frequency Control (DFC)
- Serial Interface (SIF) for communication with CPU clock subsystem
- Dynamic Efficiency Control (DEC) automatically drops and adds phases to optimize efficiency.Includes power saving PS1 and PS2 modes in addition to full power mode PS0
- SMBus interface provides extensive programmability and telemetry data to the host system
- Voltage mode control provides fast load transient response with excellent PWM stability
- Under Voltage Lockout for both IC & System
- Output OVP, UVP, OCP protections and OTP protection for system. Thermal alert VRHOT# signal to host system
- Rail1 power good monitors VR_READY1.Enable input to satisfy VR12/IMVP-7 specifications
- RoHS compliant 40-pin 5mm x 5mm QFN package

APPLICATIONS

- Mobile PC
- Voltage Regulator Modules
- Industrial PCs

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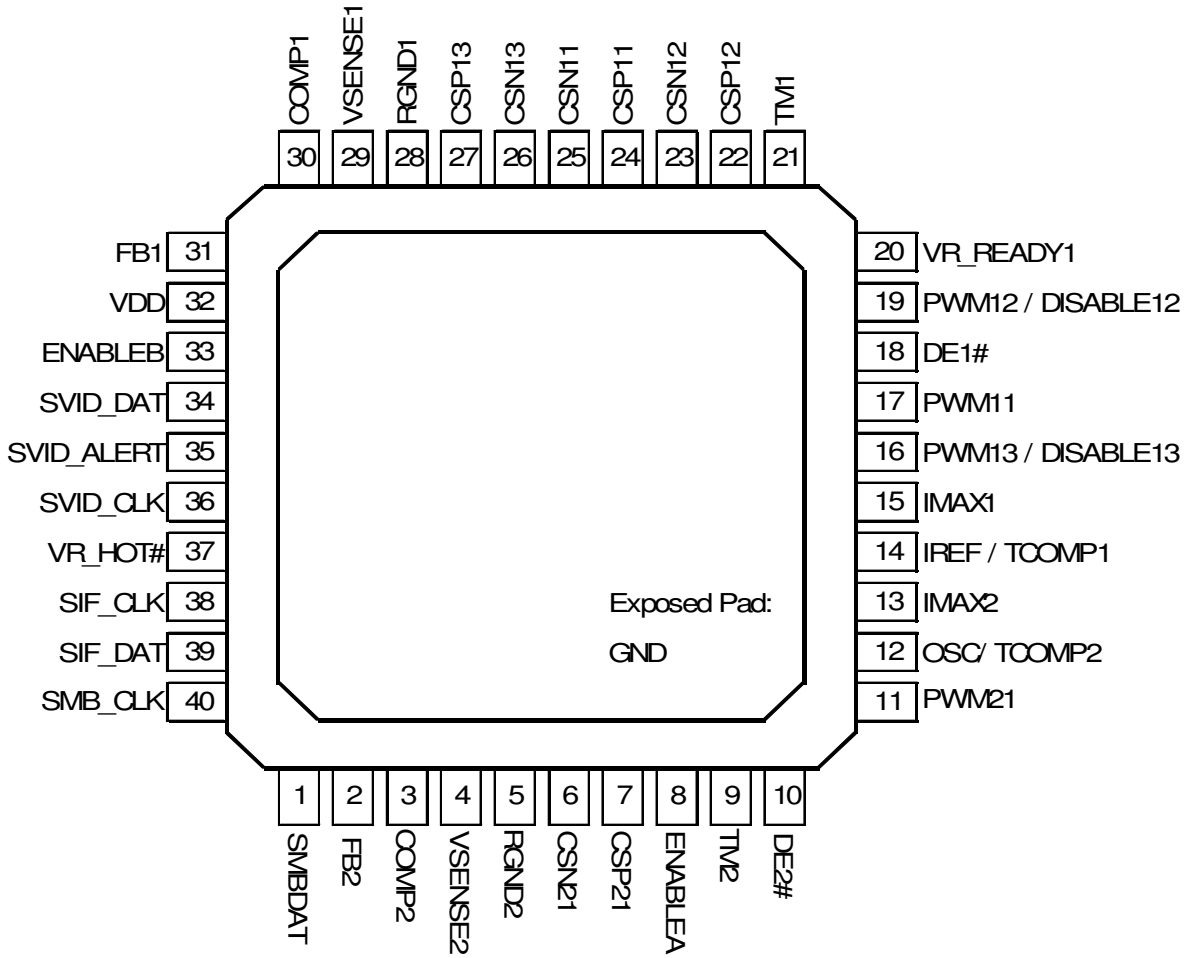
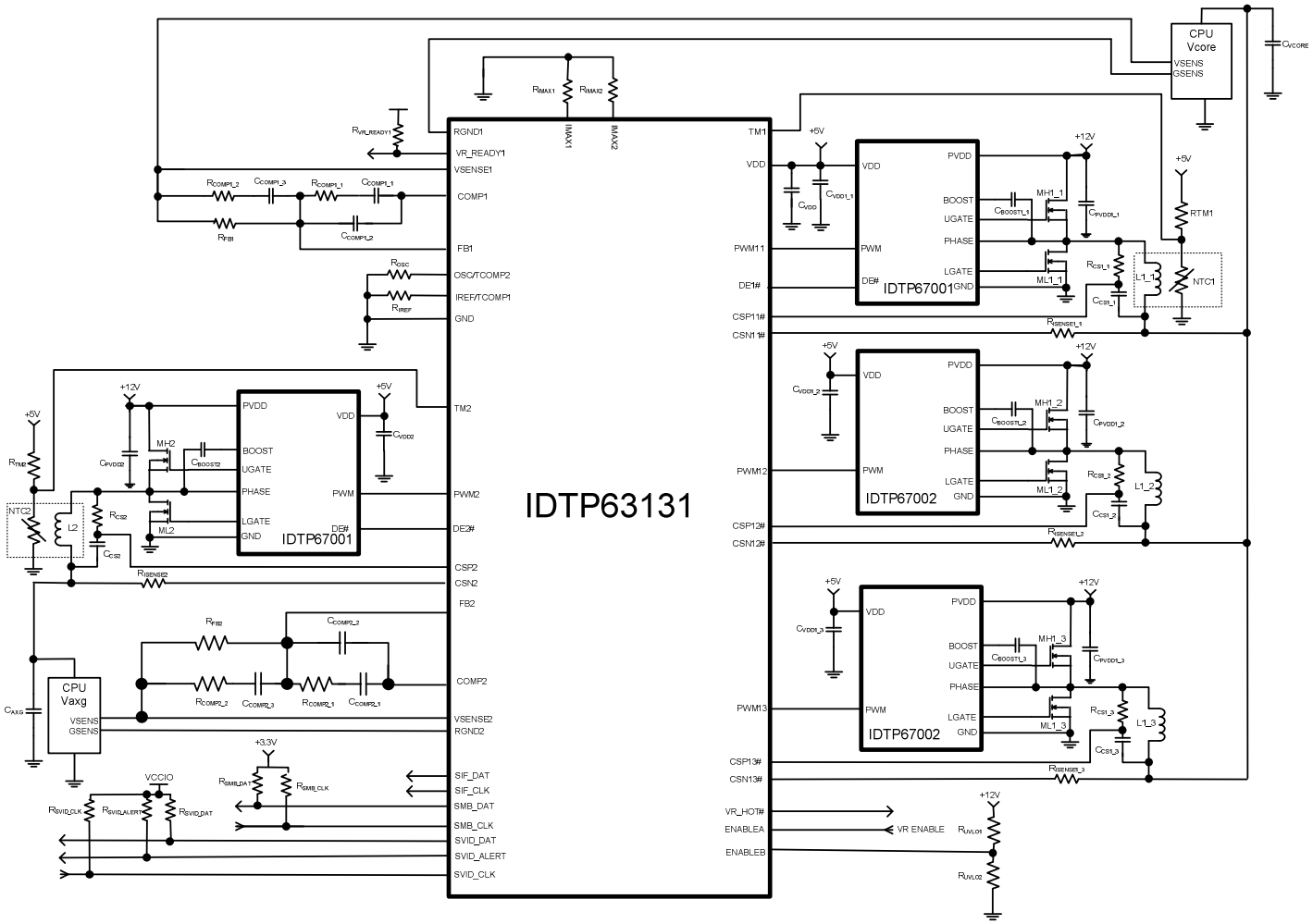
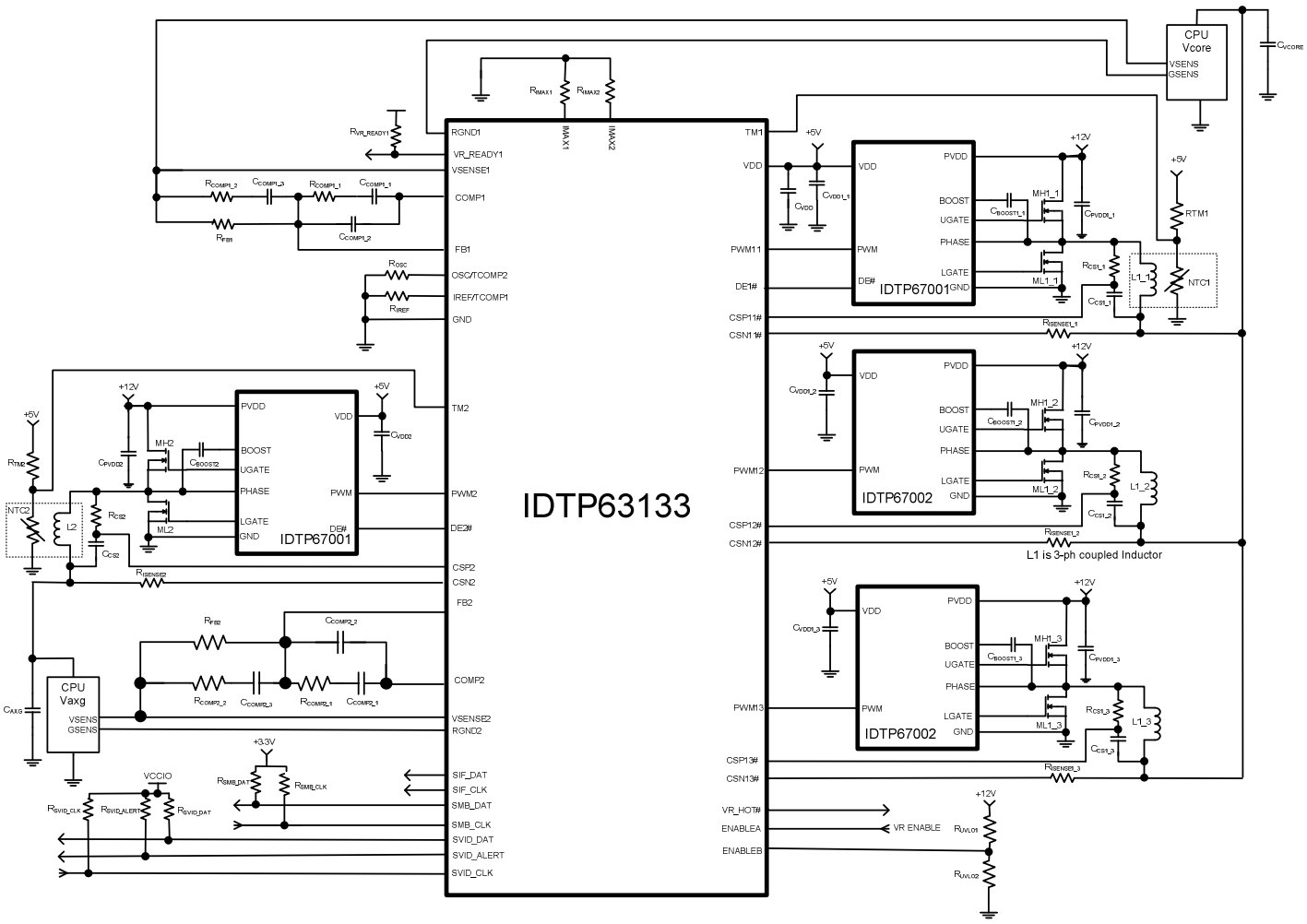
PIN ASSIGNMENT



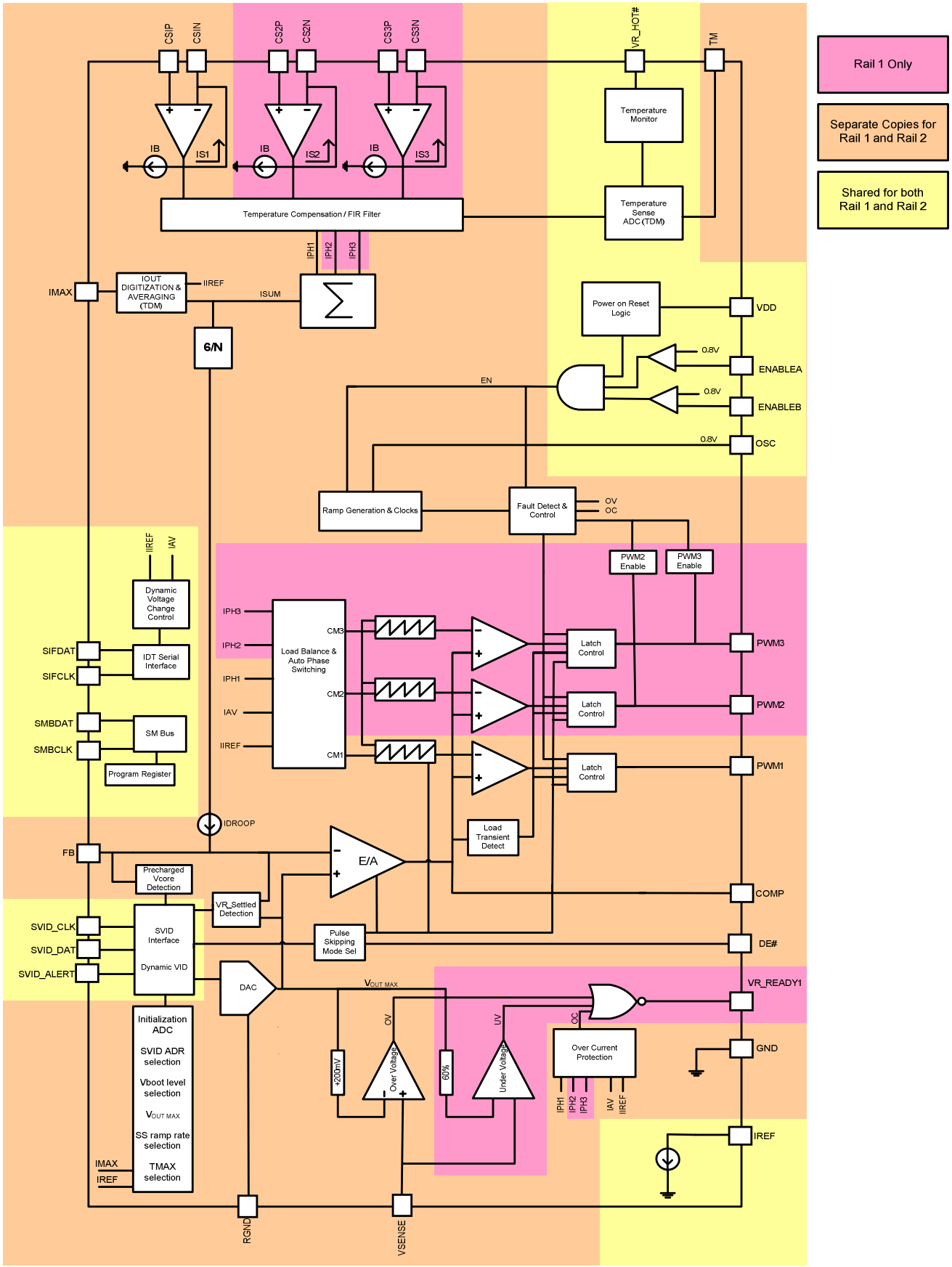
APPLICATION CIRCUIT (Discrete Inductor)



APPLICATION CIRCUIT (Coupled Inductor)



BLOCK DIAGRAM



PIN TYPES

I/O TYPE	DESCRIPTION
A-I, A-O	**Analog Levels**: Input, Output
D-I, D-O , D-IO	**Digital Levels**: Input, Output, Input/Output
GND	**Ground**: Any connection to Ground
P-I	**Power Supply**: Input
NC	**No Internal Connection**

PIN DESCRIPTIONS

Pin #	Pin Name	Pin Type	Description
1	SMB_DAT	D-IO	Data input and output for SMBus serial interface.
2	FB2	A-I	Inverting input to the Rail 2 error amplifier.
3	COMP2	A-O	Output of the Rail 2 error amplifier.
4	VSENSE2	A-I	Rail 2 output voltage remote sense positive input.
5	RGND2	A-I	Rail 2 output voltage remote sense negative input.
6	CSN2	A-I	Rail 2 current sense amplifier inverting input.
7	CSP2	A-I	Rail 2 current sense amplifier non-inverting input.
8	ENABLEA	A-I	1 of 2 enable inputs. Connect to VR input voltage (12V) with resistor divider for UVLO or VR enable input.Keep this pin voltage below 4V for normal operation.Connect this pin to VDD (5V) prior to power-on to program 1.1V Boot Voltage on both Rail 1 and 2. Advanced diagnostic and one time programming capabilites can be activated by this pin. Contact IDT technical support for more info.
9	TM2	A-I	Rail 2 thermal monitor input. Connect to a negative thermal coefficient (NTC) thermistor network to generate a voltage inversely proportional to temperature.
10	DE2#	D-O	Active low signal enables diode emulation mode for Rail2 phase #1 driver IC.
11	PWM2	D-O	Rail 2 PWM output signal.
12	OSC/TCOMP2	A-I	External resistor connected to GND or VDD programs the oscillator frequency, which is common for both PWM rails. Also determines whether temperature compensation for Rail2 is enabled. Connecting the resistor to GND enables compensation while connecting it to VDD disables compensation.
13	IMAX2	A-I	Programs the total OCP trip levels and scales the DVC & DEC thresholds for Rail 2.
14	IREF/TCOMP1	A-I	External resistor connected to GND or VDD creates an accurate internal current reference. Also determines whether temperature compensation for Rail1 is enabled. Connecting the resistor to GND enables compensation while connecting it to VDD disables compensation.
15	IMAX1	A-I	Programs the total OCP trip levels and scales the DVC & DEC thresholds for Rail 1.
16	PWM13/DISABLE13	D-IO	Rail 1 Phase 3 PWM output signal. Also programs the number of Rail 1 active phases at power-up.
17	PWM11	D-O	Rail 1 Phase 1 PWM output signal.
18	DE1#	D-O	Active low signal enables diode emulation mode for Rail1 phase #1 driver IC.
19	PWM12/DISABLE12	D-O	Rail 1 Phase 2 PWM output signal. Also programs the number of Rail 1 active phases at power-up.
20	VR_READY1	D-O	Open-drain active drives low if Rail 1 output voltage is not in regulation or if any fault condition exists.
21	TM1	A-I	Rail 1 thermal monitor input. Connect to a negative thermal coefficient (NTC) thermistor network to generate a voltage inversely proportional to temperature.
22	CSP12	A-I	Rail 1 Phase 2 current sense amplifier non-inverting input.
23	CSN12	A-I	Rail 1 Phase 2 current sense amplifier inverting input.
24	CSP11	A-I	Rail 1 Phase 1 current sense amplifier non-inverting input.
25	CSN11	A-I	Rail 1 Phase 1 current sense amplifier inverting input.
26	CSN13	A-I	Rail 1 Phase 3 current sense amplifier inverting input.
27	CSP13	A-I	Rail 1 Phase 3 current sense amplifier non-inverting input.
28	RGND1	A-I	Rail 1 output voltage remote sense negative input.
29	VSENSE1	A-I	Rail 1 output voltage remote sense positive input.
30	COMP1	A-O	Output of the Rail 1 error amplifier.
31	FB1	A-I	Inverting input to the Rail 1 error amplifier.
32	VDD	P-I	IC Bias. Connect to 5V supply.
33	ENABLEB	A-I	1 of 2 enable inputs. Connect to VR input voltage (12V) with resistor divider for UVLO or VR enable input.
34	SVID_DAT	D-IO	SVID bus data signal.
35	SVID_ALERT	D-O	SVID bus alert signal.
36	SVID_CLK	D-I	SVID bus clock signal.
37	VR_HOT#	D-O	Open drain active low signal indicates either Rail 1 or 2 is close to its maximum thermal limit.
38	SIF_CLK	D-O	Clock output pin for the SIF interface.
39	SIF_DAT	D-O	Data output pin for the serial interface.
40	SMB_CLK	D-I	Clock input for SMBus serial interface.
41	GND	GND	IC bias and substrate. Connect package tab to ground.

ABSOLUTE MAXIMUM RATINGS

Stresses above the ratings listed below can cause permanent damage to the IDTP63131/IDTP63133. These ratings, which are standard values for IDT consumer rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating	Units
Supply Voltage, VDD	-0.3 to 6	V
All Inputs and Outputs	GND -0.3 to VDD +0.3	V
ESD (HBM)	2000	V
Junction Temperature	-40 to +150	℃
Operating Temperature	-40 to 85	℃
Storage Temperature	-65 to +150	℃
Soldering Temperature	260	℃

Electrical Characteristics

Unless stated otherwise, 4.75V ≤ VDD ≤ 5.25V, -40°C ≤ Junction Temperature ≤ 100°C. Typical values are at T_J = 25°C.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Bias Current						
Quiescent Current	I_{VDD}	PWM1112,13,21 Open ,RT=63.4K		22	25.5	mA
RGNDx Bias Current	I_{RGND}	VAC=2.2V			450	µA
Power-On Reset						
POR Threshold	VDD_{RTH}	Rising	4.0	4.2	4.4	V
	VDD_{HYS}	Hysteresis	0.3	0.5	0.7	V
ENABLEA/B Threshold	EN_{RTH}	Rising	0.75	0.8	0.85	V
	EN_{HYS}	Hysteresis		40		mV
Bias Current	EN_{BIAS}	V(ENx) = 1V	-1		5	µA
Master Oscillator						
Frequency Accuracy	F_{SW}	Rosc = 63.4 kΩ (+/-1%)	368	395	432	kHz
Adjustment Range of Switching Frequency	F_{SWAR}	Minimum setting			200	kHz
		Maximum setting	1000			kHz
Ramp Generator						
Ramp Amplitude	V_{RA}			2.4		V
Max PWM Duty Cycle	DC_{PWM}		90			%
Reference and DAC						
System Accuracy (1.0V – 2.16V)		Includes Error Amp input offset measred at 1V,0.8V,0.5V	-0.5		+0.5	%
System Accuracy (0.8V – 0.995V)			-5		+5	mV
System Accuracy (0.25V - 0.795)			-8		+8	mV
DVID Slow Slew Rate	DVIDS		2.5	3.33		mV / µs
DVID Fast Slew Rate	DVIDF		10	13.33		mV / µs
Over Current Protection						
Over current Threshold	I_{OC_TOT}	Sum of configured phases sense current for a given rail		1.25x I_{MAX}		µA
Current Sensing						
Rail1 Droop Current Accuracy at 20A/phase	I_{FB1_60A}	ISENS11=ISEN12=ISENS13=20µA ,RISENSX=499Ω	114	120	126	µA
Rail1 Droop Current Accuracy at 30A/phase	I_{FB1_90A}	ISENS11=ISEN12=ISENS13=30µA, RISENSX=499Ω	171	180	189	µA
Rail2 Droop Current Accuracy at 20A/phase	I_{FB1_20A}	ISENS21=20µA, RISENSX=750Ω	113 (109)	120	127 (129)	µA
Rail2 Droop Current Accuracy at 30A/phase	I_{FB1_90A}	ISENS21=30µA, RISENSX=750Ω	169.5 (167.5)	180	190.5	µA
Rail1 Digital Report	I_{DIG1}	IFB1=169.8µA, IMAX=112A, RISENSX=499Ω	B5h	C1h	CDh	(%IMAX*256)-1
Rail2 Digital Report	I_{DIG2}	IFB2=163.8µA, IMAX=36A, RISENSX=750Ω	B7h	C1h	CBh	(%IMAX*256)-1
Common Mode Range	V_{CM_SENS}		0.5		2.2	V
PWM Outputs						
PWM Output Voltage Low	V_{OL_PWM}	Load = +1 mA			0.4	V
PWM Output Voltage High	V_{OH_PWM}	Load = -1 mA	4.0			V

Electrical Characteristics (Continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
PWM12 & PWM13 Inputs						
Input Low	V_{ILPWM}				0.25 x VDD	
Output OV and UV Protection						
UV & OV Threshold	V_{UVR}	VSENSE Rising	65	70	75	%VID
	V_{UVF}	VSENS Falling	55	60	65	%VID
	V_{OVR}	VSENSE Rising	-8%	V_{OUT_MAX} + offsets + 200mV	+8%	V
Error Amp						
DC Gain	A_{EA}	R_L = 10 kΩ to ground		80		dB
Gain-Bandwidth Product	GBW_{EA}	C_L = 30 pF		15		MHz
Slew Rate		C_L = 30 pF, R_L = 6k		15		V/µs
Maximum Output Voltage	V_{OH_EA}	Load = -1000 µA	4.2			V
Minimum Output Voltage	V_{OL_EA}	Load = 1000 µA(Clamped Internally)			0.7	V
SVID Input/Output						
CPU I/O Voltage	V_{TT} (VDDIO)		0.95	1.05 to 1.0	1.08	V
Input Low	V_{IL_SVID}				0.45	V
Input High	V_{IH_SVID}	Input High Voltage	0.65			V
Hysteresis	V_{HYS_SVID}	Hysteresis	0.05			V
Buffer On Resistance	R_{ON_SVID}	V_{DRAIN}=0.31* V_{TT}	4		13	ohm
Output High Voltage	V_{OH_SVID}	Open Drain,R pull up to V_{TT}		V_{TT}		V
VR_READY Outputs						
Output Voltage	V_{VRDY}	Load = 4mA			300	mV
Leakage Current	I_{VRRDY}	V(VR_READYx) = 5.0V	-1		1	µA
VR_HOT# Output						
CPU I/O Voltage	V_{TT} (VDDIO)		0.95	1.05 to 1.0	1.08	ohm
Thermal Monitor						
VR_HOT# Trip point	T_{MAX}	VR_HOT# assertion set by TMAX	-4	T_{MAX}	4	°C
VR_HOT# Hysteresis	T_{VRH_HYS}	VR_HOT# de-assertion Hysteresis		3		%
SVID Thermal Alert	T_{ALRT}	SVID Thermal Alert assertion set by 0.97 * TMAX	-4	0.97*T_{MAX}	4	°C
SVID Thermal Alert Hysteresis	T_{ALRT_HYS}	SVID Thermal Alert de-assertion Hysteresis		3		%
Thermal reporting SMBUS / SVID register	$T_{SENSE20}$	0 °C to 20 °C thermistor temperature range	-5 (-7)		5 (7)	°C
Thermal reporting SMBUS / SVID register	$T_{SENSE70}$	20 °C to 70 °C thermistor temperature range	-5		5	°C
Thermal reporting SMBUS / SVID register	$T_{SENSE110}$	70 °C to 110 °C thermistor temperature range	-3		3	°C
Current sense Compensation	T_{COMP}	Sense current error from VTM=20 °C to VTM=100 °C Tcomp enabled for Cu DCR	-4		4	µA
SMBus						
Input Low Threshold	V_{IL_SMB}				0.8	V
Input High Threshold	V_{IH_SMB}		2.0			V
Input Hysteresis	V_{HYS_SMB}		150			mV
Output Voltage	V_{OL_SMB}	Open drain sinking 8mA			400	mV
SIF_CLK & SIF_DAT Output						
LOW level output voltage	V_{OLSIF}	1 mA load			0.25XVDD	V
HIGH level output voltage	V_{OHSIF}	1 mA load	0.75XVDD			V

Note: Limits in parenthesis are applicable when Industrial temp range is used.

INTRODUCTION

The IDTP63131/IDTP63133 is a dual output PWM control IC that is complaint with Intel VR12/IMVP7 power specifications. The primary output (Rail 1) can be configured for 1 to 3 phase operation. The secondary output (Rail 2) provides single phase operation. An advanced control loop algorithm is included that overrides the fixed frequency PWM timing and allows all available phases to fire simultaneously in response to load steps.

Programmable Dynamic Voltage Control (DVC) and Dynamic Frequency Control (DFC) allow CPU performance and power consumption to be optimized as a function of load current. Dynamic Efficiency Control (DEC) enables all configured phases to operate when full current output is required and dynamically reduces the number of active phases at reduced current levels.

An SMBus interface allows programming of IC configuration parameters and provides diagnostic and operational telemetry data to the host system.

The IDTP63131/IDTP63133 can operate in stand-alone mode or it can be one part of a two chip solution to implement a high performance, energy saving, computing system. The IDTP63131/IDTP63133 PWM controller and ICS9CPS4592 clock generator coordinate adjustments to the output voltage with changes in the clock frequency to optimize system performance. Figure 1 provides a simplified block diagram of this system.

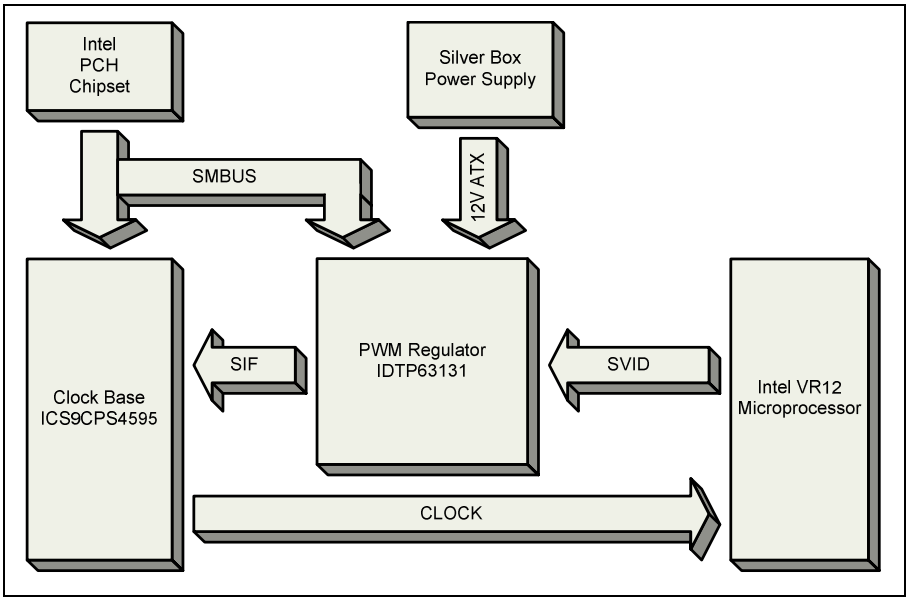


Figure 1 – Two Part System using the IDTP63131 and the ICS9CPS4595

FEATURE SUMMARY

The IDTP63131/IDTP63133 provides a rich feature set in addition to what is required by VR12/IMVP7 as described in the following table.

Feature	Rail 1	Rail 2	Description
Programmable Soft Start	Y	Y	SMBus programmable for each rail
Programmable Switching Frequency	Y	Y	Both Rails have the same per phase switching frequency during PS0 and PS1 operation
SMBus Interface	Y	Y	Extensive Programmability and Telemetry Capabilities. All VR12 SVID registers available through SMBus.
Dynamic Voltage Control	Y	Y	Programmable output offset voltage based upon Rail 1 load current
SIF Interface	Y	N	Serial communication interface to IDT Clock IC
Dynamic Frequency Control	Y	Y	Load current info communicated to IDT Clock IC for CPU clock frequency scaling
Programmable Output Voltage	Y	Y	SMBus can offset or overide SVID
Output Voltage up to 2.6V	Y	Y	SMBus programmable for DVC/DFC and standard overclocking
Dynamic Efficiency Control	Y	Y	Programmable automatic phase shedding and diode emulation based upon load current
PS2 frequency	Y	Y	SMBus enabled option
Temperature Reporting	Y	Y	Read through SVID or SMBus. 1 degree C resolution.
Temperature Offset	Y	Y	Calibrate for environmental factors. SVID and SMBus programmable.
Programmable SVID address	Y	Y	SVID address is SMBus progammable
Programmable OC, UV, OV	Y	Y	SMBus programmable trip thresholds
SMBus diagnostics	Y	Y	OC, OV, UV , and OT warning and fault events reported to host system
Phase disable through SMBus	Y	Y	Useful during debug
Low frequency SVID operation	Y	Y	10us link state timeout option allows system testing using standard test/ATE equipment. SMBus enabled.
Test Mode	Y	Y	Connecting the TEST pin to VDD (5V) prior to power-on provides 1.1V Vboot voltage on both Rail 1 and 2. Useful for VR debug without CPU or Vtt tool installation.

PIN PROGRAMMABLE INITIALIZATION

There are six IDTP63131/IDTP63133 functions that are pin programmed through detection of a pin voltage or current. These functions are;

1. Number of Configured and Populated Rail 1 Phases
2. Precision Bias Current Generator
3. Load Line Temperature Compensation Enables
4. VR maximum load current (IMAX)
5. Switching Frequency

Number of Active Rail 1 Phases

Phase 1 is always active and should always be configured with an appropriate power stage (driver IC, FETs, and inductor). Phase 2 and phase 3 are optional and its power stage does not need to be populated. The number of active Rail 1 phases is determined by evaluating the state of the PWM13 and PWM12 pins upon IC power-up. The most straightforward approach to achieve the desired configuration is as follows;

- To select a 2 phase configuration connect both PWM13 to ground.
- To select a 1 phase configuration connect PWM13 and PWM12 to ground

Table 1 – Rail 1 Active Phase Number Configuration Options

PWM13 Level	PWM12 Level	Rail 1 Active Phases
L	L or H	1 phase
L	Connect to PWM12	2 phase
Connect to PWM13	Connect to PWM12	3 phase

The PWM12 and PWM13 input pins are sampled 800us after the later of VDD under voltage lockout or ENABLEA/B input pins exceeding their thresholds. The high or low levels must be continually held in their respective states for 150us. A compatible external Driver IC that includes internal bias resistors such as IDTP67001 will automatically bias the PWM pins to the ~1/2 VDD voltage. Power the Driver IC from the same 5V supply as the IDTP63131/IDTP63133.

SMBus Control and Reporting of Rail 1 Active Phase Number

The number of configured and active rail 1 phases can be read through the SMBus. If a SVID PS1, 2, or 3 or DEC event has deactivated one or more phases only the number of active phases is reported. All phases except phase 1 can also be disabled through SMBus to assist in VR debug. Disabling phases through SMBus does not affect phase timing.

Reference Current (IREF) and Rail 1 Load Line Temperature Compensation Enable

Many of the IDTP63131/IDTP63133 functions are pin programmed by a current created by regulating a voltage across an external resistor. In some cases the resulting current is used directly by internal analog circuitry. In other cases the current is fed to an ADC(analog to digital converter) for further processing by internal digital circuitry. In order to accurately process this current information an accurate reference current is created by placing a 51.1kΩ (± 1% accurate) resistor between IREF and either GND or VDD. Connecting the resistor to GND enables Rail 1 load line temperature compensation while connecting it to VDD disables it. The voltage across the IREF resistor is regulated to 0.8V creating a nominal 16µA reference current.

Pin Current Programming ADCs

A number of IDTP63131/IDTP63133 functions are digitally pin programmed by placing an external resistor between a pin and either GND or VDD. The voltage across the external resistor is regulated to 0.8V. The resulting current is fed to an ADC where it is compared to the IREF current and converted to digital form. The block diagram of this circuit is shown in figure 2.

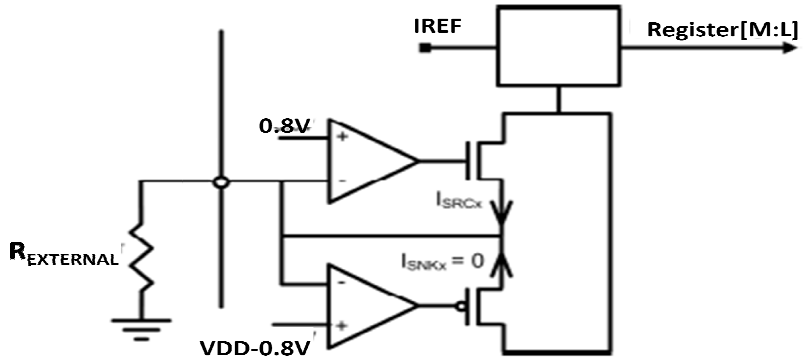


Figure 2 – Pin Programming ADC

Maximum VR Load Current (IMAX)

The IMAX1 and IMAX2 pins program the maximum load current for both Rail 1 and Rail 2 respectively. Unlike some of the other initialization pins, these pins remain active during VR operation since OCP detection relies upon the derived current. A 3-bit ADC converts the IMAX pin current to a digital word to program the digital IMAX registers. Connecting a resistor from the IMAX pin to either ground or VDD effectively provides 4-bit resolution. As phase count increases, it is reasonable to expect that a higher IMAX threshold is desirable. Therefore, a fixed base IMAX level is set depending on the number of active phases. The base IMAX level starts at 0A for one phase configurations and 64A for two or three phase configurations. The base IMAX level increases in 4A increments up to 60A for one phase and 124A for two or three phases. Select the appropriate resistor from the following table.

Table 2 – IMAX Configuration Options

# of Config Phases	RIMAX Connection	RIMAX (kohm)	IMAX
1	GND	200	0
1	GND	66.5	4
1	GND	40.2	8
1	GND	28.7	12
1	GND	22.1	16
1	GND	18.2	20
1	GND	15.4	24
1	GND	13.0	28
1	VDD	200	32
1	VDD	66.5	36
1	VDD	40.2	40
1	VDD	28.7	44
1	VDD	22.1	48
1	VDD	18.2	52
1	VDD	15.4	56
1	VDD	13.0	60
2 or 3	GND	200	64
2 or 3	GND	66.5	68
2 or 3	GND	40.2	72
2 or 3	GND	28.7	76
2 or 3	GND	22.1	80
2 or 3	GND	18.2	84
2 or 3	GND	15.4	88
2 or 3	GND	13.0	92
2 or 3	VDD	200	96
2 or 3	VDD	66.5	100
2 or 3	VDD	40.2	104
2 or 3	VDD	28.7	108
2 or 3	VDD	22.1	112
2 or 3	VDD	18.2	116
2 or 3	VDD	15.4	120
2 or 3	VDD	13.0	124

Oscillator and Rail 2 Thermal Compensation Enable

An external resistor connected to the ROSC pin to GND programs the switching frequency according to equation 1. Connecting the resistor to GND enables Rail 2 thermal compensation (discussed later). Connecting the resistor to VDD disables Rail 2 thermal compensation.

$$R_{OSC} = 1 / F_{SW} \times 40pF \text{ (equation 1)}$$

$$F_{SW} = 1 / R_{OSC} \times 40pF$$

Boot Voltage (Test Pin)

VR12/IMVP7 specifications require an initial boot (start) voltage of zero volts (off) for desktop and notebook client platforms. However this can be inconvenient during initial VR power-on, debug, and characterization as it requires a CPU, Vtt tool, or other means to send SVID or SMBus commands to the controller to initiate VR start-up. To address this issue the IDTP63131/IDTP63133 includes a test function. If the ENABLEA pin (Pin 8) is connected to VDD (5V) prior to the application of input power both Rail 1 and 2 will power-up with VBOOT = 1.1V without the need for SVID or SMBus commands. For normal operation this pin should be connected to platform enable signal.

In addition to enabling a 1.1V boot voltage, operation in test mode (ENABLEA pin = VDD) also provides advanced diagnostic and one time programmability (OTP) functionality. Please contatct IDT technical support for more information on extended test mode capabilities.

THEORY OF OPERATION

Phase Current Sensing

Inductor DCR current sensing is implemented by connecting a series resistor and a capacitor network in parallel with the inductor and measuring the voltage across the capacitor as shown in Figure 3. Usually the resistor R_{CS} and capacitor C_{CS} are chosen so that the time constant of R_{CS} x C_{CS} equals the time constant of the inductor, which is the inductance L divided by the inductor R_{DCR}. If the two time constants match, the voltage across C_{CS} is proportional to the current through the inductor and the sense circuit can be treated as if it was a sense resistor in series with the inductor. Any mismatch of the time constants does not affect the measurement of inductor DC current, but affects the AC component of the inductor current.

As depicted in figure 3, the IDTP63131/IDTP63133 includes current sense amplifiers in each phase that use feedback to inject a current out of each CSNn input pin such that its voltage is the same as the corresponding CSPn pin. Thus, the voltage across the C_{CS} capacitor, which represents the inductor current, appears across the R_{ISENSE} resistor. The resulting I_{SENSE} current is used to control load balancing, load line, and other functions that require accurate inductor current information. A fixed I_{BIAS} current that is derived from the IREF current reference is added to prevent a “dead zone” when inductor current is zero or negative. This bias current is subtracted prior to subsequent processing by internal circuits. If a noise filter cap is applied from the CSN pin to ground its value should be 47pF or less to ensure stability of the current sense amplifier.

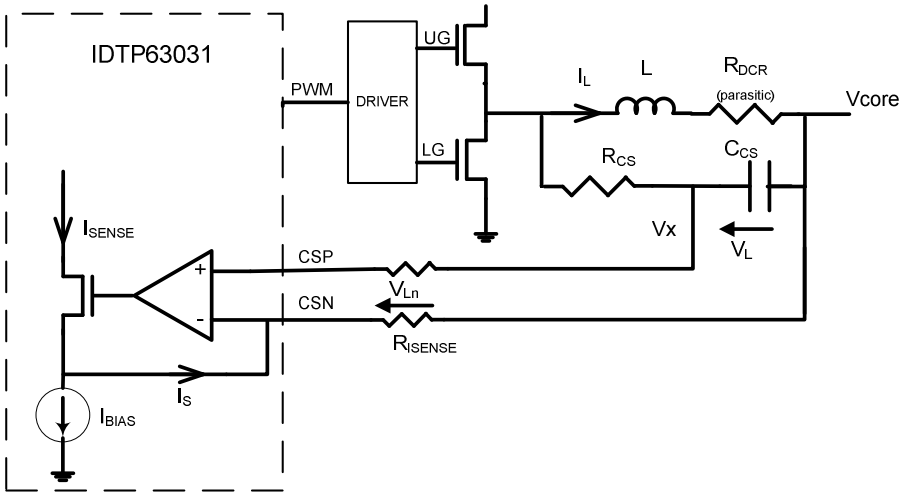


Figure 3 – Inductor Current Sensing

R_{ISENSE} resistor selection

To ensure output current is correctly reported via the SVID or SMBus the R_{ISENSE} resistors should be selected so that 1µA is generated for every Amp of inductor current. Use equation 2 to select the R_{ISENSE} resistor values for both Rail 1 and Rail 2.

$$R_{ISENSE} = DCR \times 1{,}000{,}000 \quad \text{(equation 2)}$$

For an inductor with a 0.5 mohm DCR; R_{ISENSE} = .0005 ohm x 1,000,000 = 500 ohms (499 ohms nearest 1% standard value).

Load Line and R_{FB} Selection

The I_{SENSE} currents from the configured phases are processed and the average value is multipled by six and outputed at the FBx pins. To maintain a constant load line impedance the droop current is derived from all the configured phases regardless of whether any are disabled due to operation in a power savings mode. The current sourced out of the FBx pins develops a voltage across the FB resistors to implement a load line. Use Equation 3 to select the FB resistor value. The FBx pin current source in either rail can be turned off to disable the load line through use of the SMBus DEV_CTRL3 register.

$$R_{FB} = R_{load\ line} \times R_{ISENSE} \times \#\ \text{of configured phases} / (DCR \times 6) \quad \text{(equation 3)}$$

For a three phase converter with DCR = 0.5 mohm, R_{ISENSE} = 499 ohms, and load line impedance of 1.7 mohms;

$$R_{FB} = 1.7\ \text{mohm} \times 499\ \text{ohm} \times 3 / (0.5\ \text{mohm} \times 6) = 848.3\ \text{ohm (845 ohm nearest 1\% standard value)}$$

Digital Load Current Reporting

The averaged sensed phase current in each rail is digitally filtered and converted to an 8 bit digital word by a dedicated 7-bit ADC. The ADC uses the pin programmed IMAX reference current as the full scale reference for the IOUT register (FFh). The 7 data bits are left justified and the LSB (bit 0) is always set high (logic 1). Each effective LSB increment (bit 1) is therefore equivalent to IMAX / 128. The ADC output is digitally averaged over a 1 ms period and is updated every 64µs. Output current is interpreted by converting the hexidecimal or binary number to decimal, dividing by 255, and multipling by the programmed IMAX value. For example if IMAX is programmed to 112A a readout of 93 hex = 10010011 binary = 147 decimal. Output current report is 147 / 255 x 112A = 64.6 Amps. Figure 4 provides a block diagram of the current sense circuit elements.

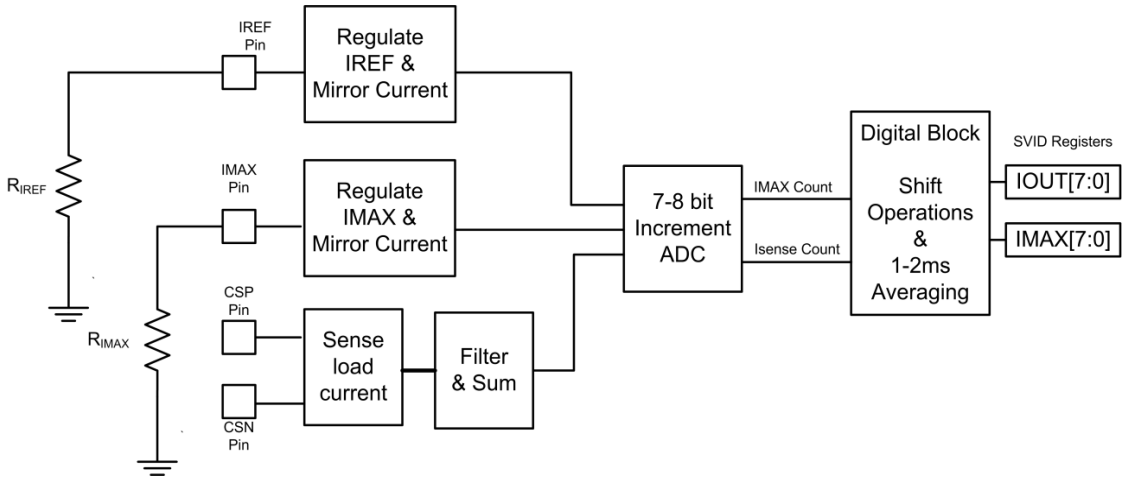


Figure 4 – Digital Load Current Report Block Diagram

PWM Modulation

The IDTP63131/IDTP63133 implements voltage mode control with trailing edge modulation. The voltage mode ramp amplitude is typically 2.4V over the full switching period (24mV / % duty cycle) with duty cycle limited to 93% to ensure proper driver bootstrap operation. After a PWM pulse is terminated the voltage mode ramp is driven to 0.8V volts by the ramp clamp. Upon receiving the next clock pulse the voltage mode ramp is created by a current source charging an internal capacitor. Current sharing among active phases is achieved by controlling the duty cycle of each phase through a current mode feedback loop. In Rail 1 Phase 1 is the master and the other phases adjust their ramps to match the Phase 1 output current. Figure 5 provides a block diagram of the PWM modulator for a 2 phase VR.

The error amp provides high gain, bandwidth, and slew rate using type 3 external compensation. A DAC (Digital to Analog Converter) sets the error amp reference voltage and is biased to the converter remote sense ground to eliminate the need for a differential remote sense amplifier and error factors associated with it. Converter output voltage offset and load line are implemented through bias currents flowing into the feeback resistor. Figure 6 depicts the error amplifier configuration.

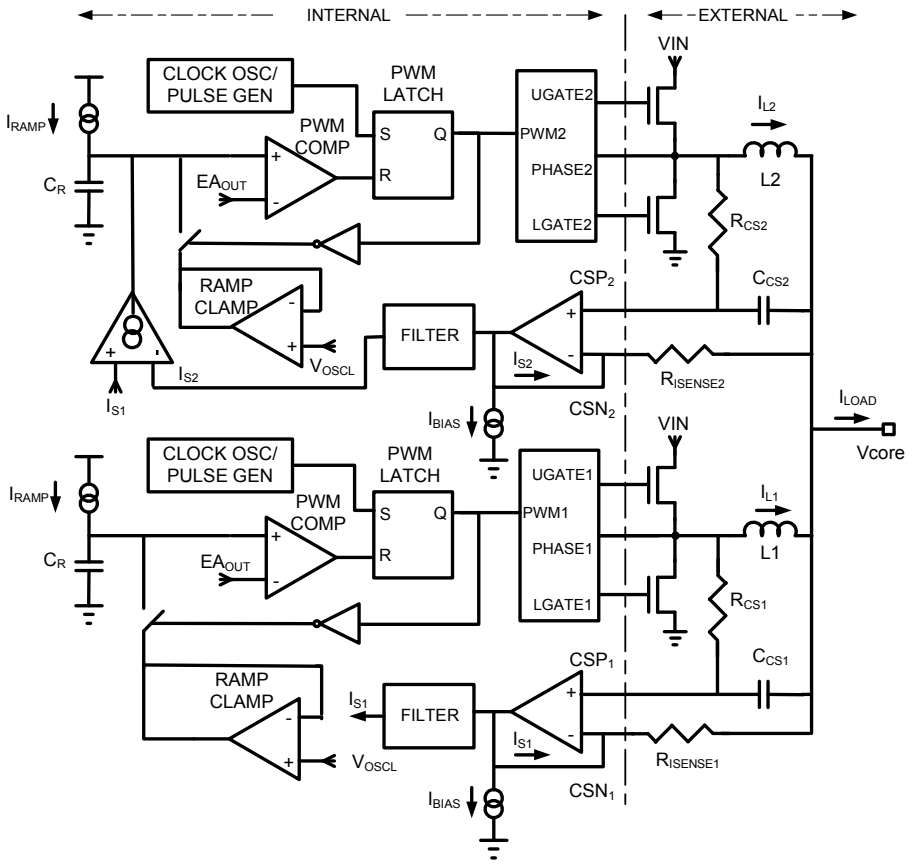


Figure 5 - PWM modulator block diagram

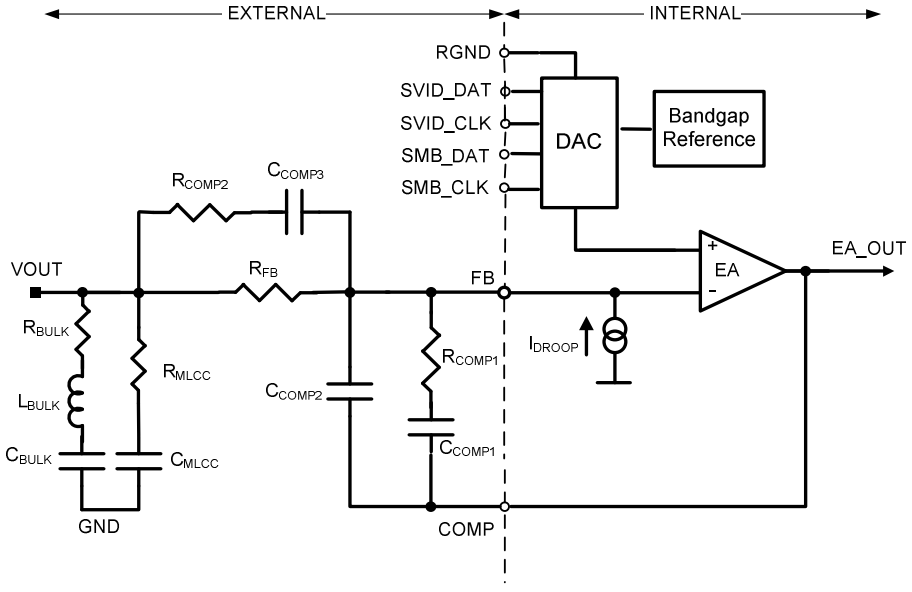


Figure 6 – Error Amp Configuration

Output Voltage Programming

IDTP63131/IDTP63133 supports the entire Intel VR12/IMVP-7 VID table and offsets for both Rail 1 and 2. Refer to the Intel specifications for more information. If an SVID offset command + SetVID command causes rollover of VID table, i.e. a voltage above 1.52V, the transaction will be rejected.

The maximum output voltage of either rail can be programmed up to 2.16V. Output voltage can also be programmed or read and additional DVC offsets can be applied through the SMBus. Offsets from SVID, SMBus, DVC can all be applied

simultaneously. The maximum output voltage is VID (1.52V) + DVC offset (programmable in 5mV increments up to 0.64V) = 2.16V. Output voltages beyond the Intel VID table are useful for high performance over clocking applications and will not trigger over or under voltage conditions. SVID register Vout Max applies only to the SVID VID code and offset; SMBus or DVC offsets are not limited by this register.

Start-up Sequence

The IDTP63131/IDTP63133 has an internal undervoltage lockout function on its 5V input. In mosty cases,the VR input voltage is 12V and provided by a different supply than the 5V controller bias. Two enable pins (ENABLEA/B) with identical functionality are provided for system enable and undervoltage lockout of the VR input voltage. Connect a resistor divider from the VR input voltage to one of the enable pins to program an appropriate threshold. The second enable pin should be connected to the platform specific signal that provides the VR enable signal. If either an internal 5V or ENABLEA/B undervoltage occurs all data registers are reset to their default or pin programmed settings. Upon clearing the 5V undervoltage threshold the IC begins it's initialization process by reading in OTP (one time programmed) trim bits and enabling SVID and SMBus communication. The initialization process can take up to 1.34ms.

The controller will begin the start-up sequence for both rails once both the enable pins have exceeded their 0.8V threshold voltages and the internal 5V undervoltage lockout has cleared. There are no special sequencing requirements for the internal 5V undervoltage lockout or the two enable inputs. If the enable inputs are asserted more than 1.34ms after the internal 5V undervoltage clears the controller will go through an additonal configuration period of up to 1ms while it reads and configures its pin programmable data registers.

After initialization the IDTP63131/IDTP63133 will power-up per Intel VR12/IMVP-7 specifications with VBOOT = 0V. The SMBus interface can also program the boot voltage to any valid VID value. If Vboot is zero volts (off) the IDTP63131/IDTP63133 does not begin PWM until an SVID/SMBus command sets a new non-zero target VID. If Vboot is programmed to anything other than zero volts the SVID ALERT line will be asserted low once soft start is complete.

Figure 7 provides a timeline for the initialization process. To ensure a smooth start-up the maximum duty cycle of the first four PWM pulses are limited to 12.5%.

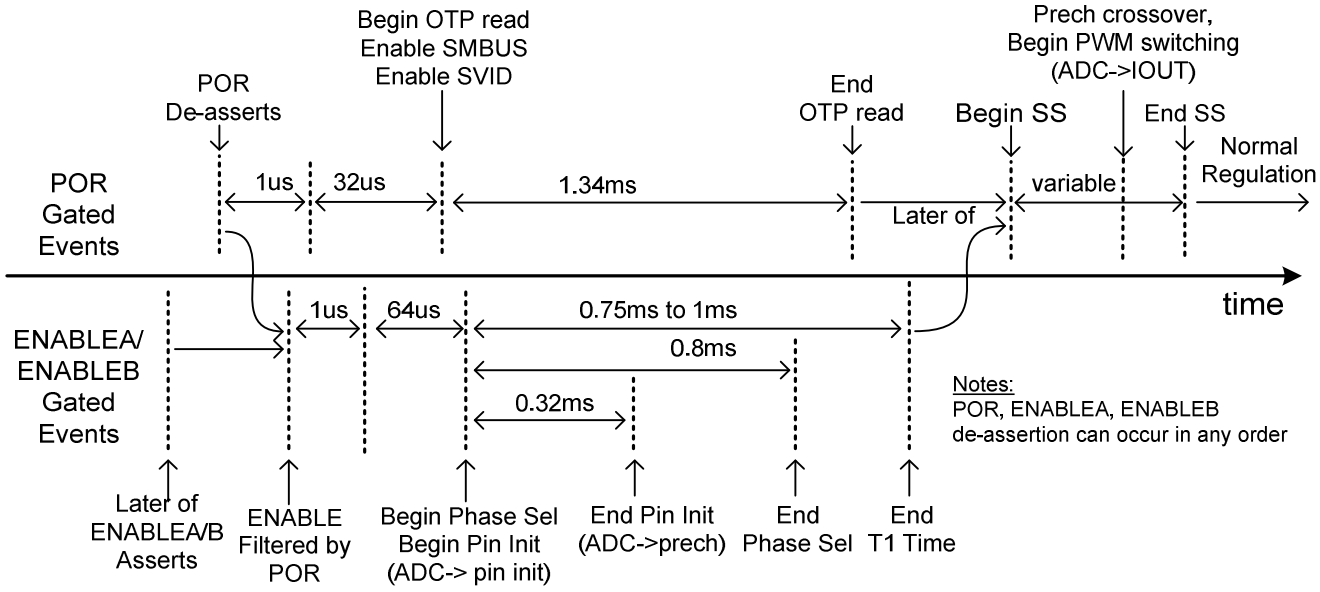


Figure 7 – Chip Initialization Sequence

Thermal Sense Voltage Generation

The IDTP63131/IDTP63133 continuously senses the VR temperature by monitoring the voltage on the TM pins (1 for each rail). The voltage-temperature dependence is determined by a thermistor typically located close to the inductors. The IDTP63131/IDTP63133 has been optimized for an NTC thermistor with a 25°C resistance of 6.8KΩ and a beta (B) of 3477 such as the Vishay NTHS0805N02N6801 and provides good accuracy over a temperature range of 0 to 110 Deg C. Connect a 1kohm resistor from VDD (5V) to each TMx pin and a thermistor from each TMx pin to ground. Contact IDT technical support if you wish to use a thermistor with different characteristics.

Temperature Trip Level (TMAX)

TMAX is the maximum temperatures the VR will support without issuing a thermal alert or VR_HOT# pin assertion. Default IDTP63131/IDTP63133 TMAX setting is 110 degrees C. However, this can programmed with SMBus to any value up to 127 degrees C in one degree C increments. IDTP63131/IDTP63133 provides independent temperature sensing for both Rail 1 and Rail 2 but they share a common TMAX value. TMAX is represented in 8 bit binary format in deg C, IE 100C = 64h.

Digital Temperature Conversion and Reporting

The voltage applied to the two TM pins is detected and converted by a single 7 bit ADC into an 8-bit digital register that provides the temperature measured at each thermistor. The ADC updates every 32µs in one bit increments or decrements so each rail is updated every 64us. Data is right justified so bits 0:6 represent VR temperature and bit 7 is always zero. Temperature readout through either SMBus or SVID is a decimal conversion of the hexidecimal/binary data from 0°C to 127°C with 1°C LSB. For example 65 degrees C would read as 41h. The output of the temperature sense ADCs can be offset up to +/-31 degress C in 1 degree increments to compensate for thermistor location, airflow, or calibration during platform manufacture using SVID or SMBus.

Temperature Compensation of Sensed Load Current

The 7 bit digital word representing temperature will thermally compensate the analog current current sense amplifiers if enabled by the IREF (Rail 1) and ROSC (Rail 2) pin programming. Current sense temperature compensation is useful for typical inductor current sense applications. Disable current sense temperature compensation if inductors with zero TC DCR are used. Every 1 deg C change in temperature causes a 0.385% change in the DCR of inductors with copper conductors and the current sense amplifier output current is adjusted accordingly. This arrangement is shown in figure 8 and results in very low thermal drift of load line and current reporting.

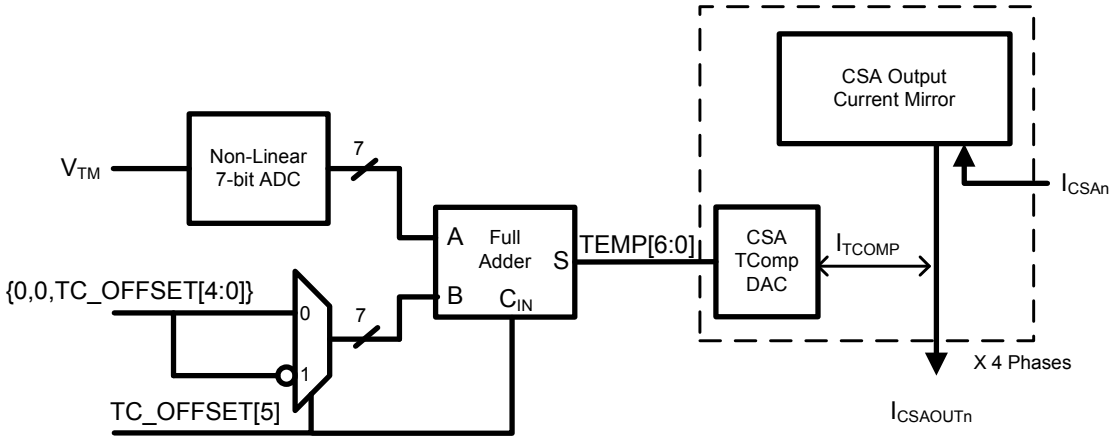


Figure 8 – Temperature Sense and Compensation Block Diagram

VR_HOT#, Thermal Alert Bit, Temperature Zones

The IDTP63131/IDTP63133 complies with all the required functionality of these temperature related features based upon the digital temperature data. Refer to Intel specifications for detailed operating descriptions.

Over Current Protection

IDTP63131/IDTP63133 provides three independent over current protection mechanisms.

1. Cycle-by-cycle over current protection terminates a PWM pulse in a phase whose current exceeds a programmable percentage above IMAX divided by the number of configured phases but does not cause VR shutdown.
2. Hiccup over current protection occurs if the average VR current continuously exceeds a programmable percentage above IMAX for a period longer than 12µs. The timeout period prevents false triggering of OCP events. To ensure that ripple and noise do not prevent OC detection the timeout period is not reset unless the average VR current drops below the over current threshold for more than 400ns.
3. Rail 1 will exit a VR12 power state or DEC mode if the current in an active phase exceeds 80% of the normal cycle-by-cycle phase over current threshold. A PS/DEC Exit event causes immediate activation of all configured phases.

Rail 1 and 2 share common OC thresholds relative to their independently programmed IMAX levels. Over current thresholds are outlined in the following table and non-default values can be programmed using the SMBus interface.

Table 3 – SMBus Programmable OC Thresholds

TRP_OCP[3:2]	Phase OC Threshold	Average OC Threshold	Rail 1 PS/DEC Exit OC Threshold
00 (default)	IMAX x 1.50 / # Configured Phases	IMAX x 1.25	IMAX x 1.2 / # Active Phases
01	IMAX x 1.80 / # Configured Phases	IMAX x 1.50	IMAX x 1.44 / # Active Phases
10	IMAX x 2.10 / # Configured Phases	IMAX x 1.75	IMAX x 1.68 / # Active Phases
11	IMAX x 2.40 / # Configured Phases	IMAX x 2.00	IMAX x 1.92 / # Active Phases

If an average OC event is detected the PWM outputs are tri-stated (MOSFET gates driven low), VR_READY1 is driven low for a Rail1 OC event, and an OC warning is asserted in the SMBus register for the corresponding rail. The controller stays in this state for 12ms and then attempts to restart. If another average OC condition occurs before soft start is completed the controller will repeat this cycle. That is, it will wait another 12ms and attempt to restart again. If an average OC fault is encountered during this second attempt an OC alert is asserted in the SMBus register for the corresponding rail. After 2 failed attempts to restart due to an average OC condition the rail is latched off and can only be cleared by cycling the VDD power input or a soft reset through the SMBus interface. The sequence of detecting an OCP event, attempting a soft start, and checking for another OCP event is called a hiccup. Figure 9 depicts an average OC event occuring during normal operation and continuing during two attempts to restart resulting in a latch off condition.

If at any point during this hiccup process the part is able to recover to normal operation for 4ms, the over-current event counter is reset to 0, and an additional three OCP events will be required to induce OCP latch off and shutdown. The VR has returned to normal operation.

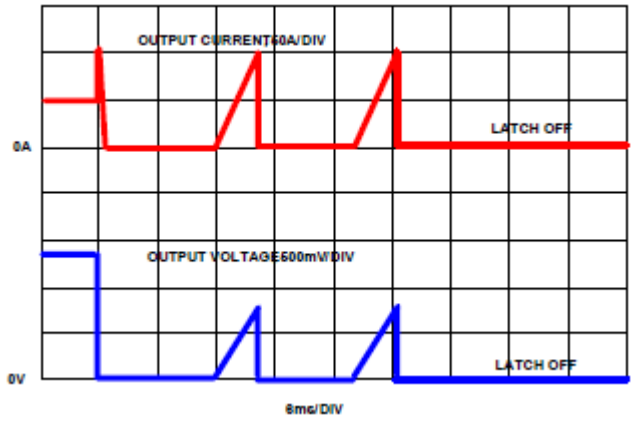


Figure 9 – OCP Hiccup and Latch Off

DVID or DVC events can cause an output voltage increase when the VR is already providing a high output current. During these events, meeting the slew rate specifications may require output currents above the nominal OCP level to charge the output capacitors. To prevent false over-current events average OCP detection is blanked during DVID and DVC increase from the first DAC code change through 128us after the final DAC code change.

VR Ready

The VR_READY1 pin is an open drain active high output that requires an external pull-up resistor. It indicates whether or not the controller is regulating output voltage, and whether any fault condition exist on the Rail1 output. During start-up and shutdown the VR_READY1 output drive low and will transition to a high impedance state after the rail start-up sequence completes and the output voltage is between the over-voltage and under-voltage limits. If an under-voltage, over-voltage, or over-current condition occurs on Rail1 its VR_READY1 pin will drive low to indicate a fault condition has occurred. If either ENABLE pin is pulled low the VR_READY1 pin will drive low to indicate that both Rail1 and Rail2 outputs have been disabled.

During an over-voltage or over-current event, VR_READY1 is latched low and will not go high again until after a successful soft-start. If an undervoltage event occurs the only action taken is that VR_READY1 is pulled low and will revert back to a high impedance state when the output voltage returns to within the under-voltage threshold.

The undervoltage threshold for increasing output voltage is measured at the VSENSE1 pins and can be programmed to 50%, 60%, 70%, or 80% of the programmed output voltage through SMBus. Hysteresis of 10% is provided for all four thresholds. A filter with a deglitch-time of one switching cycle is included to remove the possibility of false undervoltage trips.

VR_READY1 status can also be read with SMBus. To avoid confusion the SMBus register does not indicate an undervoltage condition until after successful completion of soft start.

Output Over Voltage Protection (OVP)

An over voltage event is detected if the VSENSEx pins rise above their trip thresholds for more than 250ns. The over voltage threshold is based on the value of V_{OUTMAX} plus any VID or DVC offsets. An SMBus programmable OVP offset (register 0Bh) is added to V_{OUTMAX} and any VID or DVC offsets to allow control of how much the VSENSE pins must exceed the OVP reference voltage before an OVP event is triggered. The default OVP offset is +200mV. SMBus can also communicate overvoltage faults and warnings to the host system.

The IDTP63131/IDTP63133 implements a dedicated 5 bit OVP DAC for each output to generate appropriate reference voltages for the overvoltage comparators. The OVP DAC allows OVP functionality at all times unlike other techniques such as blanking. The OVP DACs are 5 bits with 40mV as the base level and 80mV per LSB so the maximum OVP threshold is 40mV plus 31 (11111 binary) x 80mV = 2.52V plus the SMBus programmable OVP offset (+200mV default). The 5 bit OVP DAC output voltage closest to the target OVP threshold will automatically be selected as the OVP reference voltage.

Figure 10 shows the relationship between the over-voltage threshold, output voltage, the VID voltage, and V_{OUTMAX} during various DVID and DVC events. If an over-voltage condition is detected the controller will signal the driver ICs to switch on all low-side power MOSFETs and switch off all the high-side MOSFETs in order to protect the load.

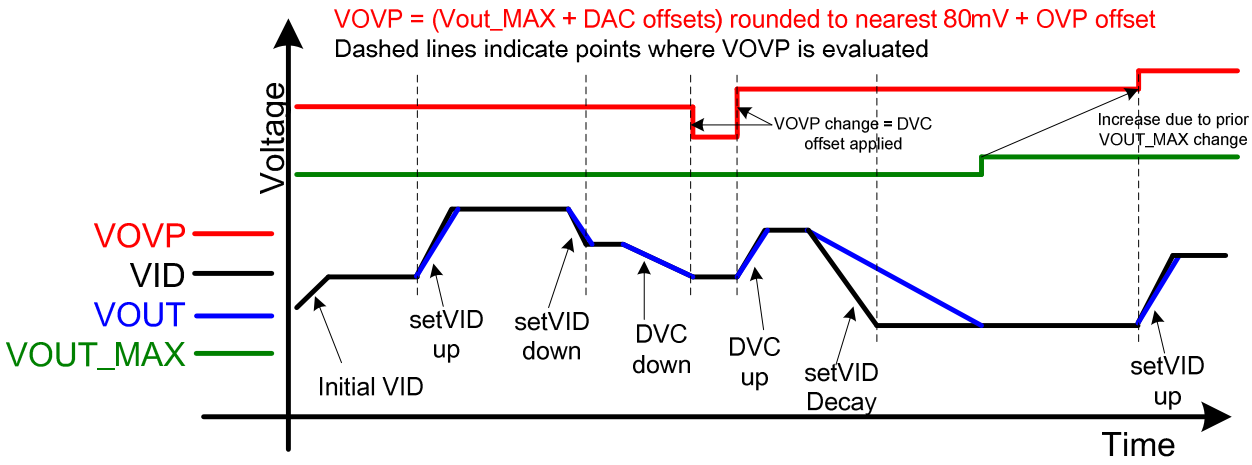


Figure 10 – OVP Threshold Interaction with DVID/DVC

If the OVP event occurs during normal operation (that is, when VR_READY is asserted), executing a power cycle or performing a SMBus reset is required to restart the controller. If the OVP event occurs during soft start, the OVP event will not be latched. Instead, the controller will bias the power MOSFETs as described above until the OVP condition disappears, and then will begin the soft start sequence. The SMBus OVP_ALERT register will not be set, but the OVP_WARN register will be set high.

Power State Operating Modes

IDTP63131/IDTP63133 provides multiple operating modes to reduce power loss when VR output current is less than the maximum. Power saving modes can be initiated through SVID or SMBus power state commands or can occur autonomously in Rail 1 if DEC is enabled. Default mode is all configured phases active with continous inductor current forced by the synchronous rectifier MOSFETs (VR12 PS0 state). Lower power state commands override DEC operation. DEC automatically resumes once an SVID or SMBus command causes PS0 to resume.

A power state 1 (PS1) command does not modify the single phase Rail 2 operation but can deactivate Rail 1 phases depending upon configuration. A power state 2 (PS2) or SetVID_Decay command initiates single phase pulse skipping operation in either rail. In PS2 the DEx pin asserts low to communicate to the compatible driver IC that it should transition

from forced continuous conduction mode to diode emulation mode. PS2 can be disabled and its operating characteristics can be adjusted using SMBus. A power state 3 (PS3) command is acknowledged, but the functionality is the same as for PS2 mode.

A Set_VID fast or slow command, all phase event, or an exit PS per phase OCP event while in PS1, 2, or 3 will cause a transistion to the PS0 state. The SVID/SMBus master must then re-issue a power state command to re-enter a lower power state. Exit from PS2 or PS1 to a higher power state is immediate to support potential increases in load current.

Rail 1 Power State Configuration and Operation

The minimum number of active phases for Rail 1 PS modes are programmable through the SMBUS. One, two, or three Rail 1 active phases can be selected but the default is one. If more than one Rail 1 active phases are programmed a PS2, PS3, or Set VID Decay command will be acknowledged but Rail 1 will remain in PS1 mode.

Upon receiving a PS1, 2, or 3 command when operating in the default PS0 state phases are gradually shed one at time by decreasing their duty cycle and contribution to load current. When the inductor current in a phase being dropped falls below approximately 3 Amps, the PWM output signal for that phase is tri-stated. The timing of remaining active phases in Rail 1 are also gradually changed to their new positions. For example a three phase VR transitioning to one phase will first gradually drop Phase 3 while Phase 2 timing gradually changes from 360 / 3 = 120 degrees to 180 degrees. When this is complete Phase 2 will gradually be dropped. This methodolgy minimizes output voltage pertubation when entering a PS mode.

Upon receiving an SVID PS2 or Set VID Decay command while in PS0 with only one phase programmed to be active Rail 1 first transitions to one phase PS1 configuration and then the remaining active phase enters discontinuous mode.

Rail 1 Dynamic Efficiency Control Mode (DEC)

DEC provides automatic variation in the number of Rail 1 active phases as a function of load current in order to optimize efficiency. DEC operation is enabled and programmed through the SMBus interface. The number of active phases is determined by comparing the sum of all active phase currents against programmable thresholds. There are two Rail 1 thresholds to deactivate phases 3, and 2. The minimum number of active phases is also SMBus programmable. If the minimum active number of Rail 1 phases is set to more than one then the thresholds for phases below the minimum are not used. The methodology used to drop and add phases is the same as for VR12 power states.

Figure 11 illustrates how the DEC levels divide up the total Rail 1 measured current into three regions. Each threshold has one value for rising currents (called “H” for high) and another for falling currents (called “L” for low) to provide hysteresis in DEC level changes. All DEC thresholds are defined as a percentage of the maximum system load current (IMAX 1 or 2) and are programmed with a 7 bit word to align with the128 levels generated by the 7 bit digital current reporting ADC.

If Rail 1 is configured for 2 phases then only DEC_LEVEL1 can be implemented to divide up the measured current into two regions.

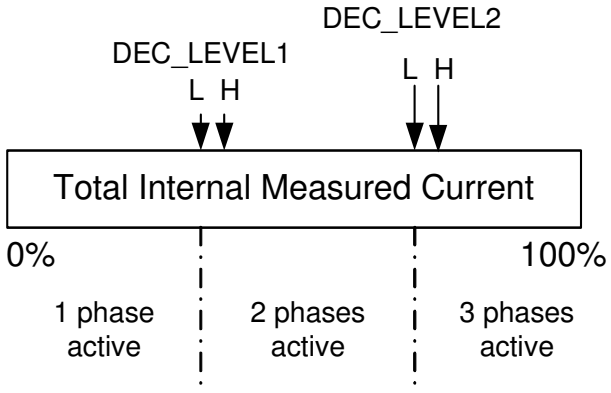


Figure 11 – Rail 1 DEC Thresholds

To prevent undesirable rapid toggling of the number of active phases, transitions are delayed by a programmable window filter. The load current must cross a DEC threshold for at least 50% of the period to initiate a change in the active phase count.

Two methods are provided to prevent increases in load current that are faster than the DEC window period from creating a phase overcurrent condition. In addition to Exit PS over current protection an All Phase event due to a fast load increase

causes DEC mode to be exited and all phases are immediately reactivated. Normal DEC operation resumes following the Exit PS OCP or All Phase event.

VR12 low power states (PS1/2/3) and DEC can both be enabled through SMBus programming. For joint DEC/PS operation, the minimum number of programmed DEC phases is used and the minimum number of PS phases is ignored. In this same joint operation, when PS0 is re-entered, all available phases are activated and then normal DEC operation resumes. There is also an SMBus programming option to automatically enter PS2 after the number of active phases has been reduced to one.

Dynamic Voltage Control (DVC) and Dynamic Frequency Control (DFC)

DVC enables output voltage to be offset as a function of load current. This feature along with controlling the CPU clock frequency (DFC) enables development of customized algorithms to increase system performance, reduce system power consumption, or both. The IDTP63131/IDTP63133 SMBus interface is required to enable DVC/DVC and configure all associated modes of operation. The IDTP63131/IDTP63133 SIF interface communicates the DVC/DFC states and other operational information to the ICS9CPS4592 clock generator IC.

There are four DVC/DFC states in the IDTP63131/IDTP63133 and companion ICS9CPS4592. The four states are supported by three IDTP63131/IDTP63133 DVC/DFC load current thresholds. As shown in figure 12, each threshold has one value for rising currents (called “H” for high) and another for falling currents (called “L” for low) to provide hysteresis in DVC level changes. DVC thresholds are defined as a percentage of the maximum system load current (IMAX1) and are programmed with a 7 bit word to align with the128 levels generated by the 7 bit digital current reporting ADC.

Each DVC level has an associated programmable positive or negative VID offset value. VR output voltage can be changed in 5mv increments up to +/- 640mV. The DVC00 offsets can also be programmed and applied to modify the VR output voltages even when DVC mode is not enabled.

The sensed Rail 1 current is used for all DVC transitions of both rails and there is only one shared set of thresholds for Rail 1 and Rail 2. This means that any Rail 1 change in DVC levels results in a change in Rail 2 DVC level. However, there are separate DVC VID offset registers for each rail, so entering DVC levels can have a different effect on the two rails. For example, Rail1 could have a +50mV offset while Rail 2 has a -10mV offset.

A programmable delay period prevents rapid changes in DVC/DFC levels. The load current must remain at the new level for at least 50% of the period or it will not result in a DVC/DFC change. Once a new threshold has been validated by the delay period the output voltage is ramped to the new VID offset at the Set VID Slow slew rate if it is a voltage decrease and at the Set VID Fast slew rate if it is a voltage increase. It is not necessary that changes in DVC levels occur incrementally. For example, it is possible to go directly from DVC00 to DVC 10.

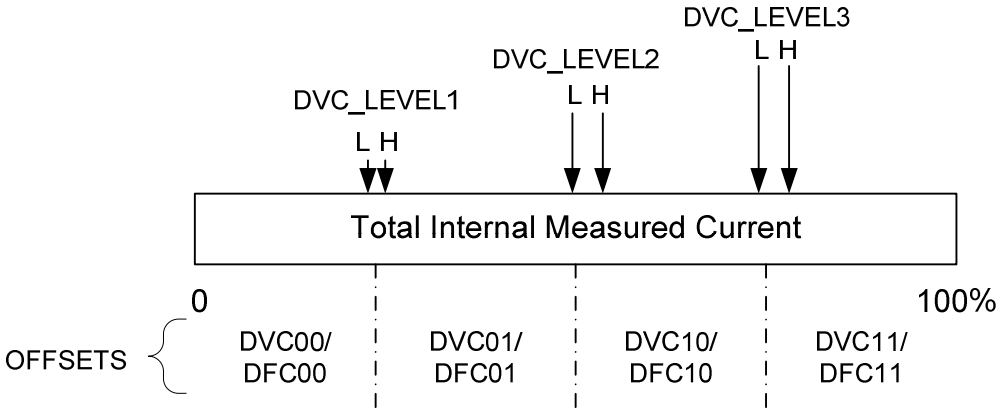


Figure 12 - DVC Threshold Levels and Offsets

To avoid “blue screen” system shutdowns output voltage must always increase prior to clock frequency increases and clock frequency decreases must precede output voltage decreases. An SMBus programmable delay ensures that output voltage decreases are delayed until they are communicated to the ICS9CPS4592 and it has completed the related decrease in clock frequency. The ICS9CPS4592 includes a delay period to ensure clock frequency is not increased until output voltage has reached a higher level. Figure 13 depicts the timing relationship between changes in output voltage and clock frequency.

The SVID VID code plus any VID offset is always the default setting for initial power-up. If DVC is enabled through SMBus the DVC commands will begin offseting the SVID VID after an SMBus programmable delay period from VR READY assertion.

There are two SMBus programming options for DVC and SVID VID control. The first option is to read and lock in the initial SVID VID code that was programmed. This option results in subsequent SVID VID commands, and changes to the SVID offset being disabled during DVC operation. The second option is to allow SVID commands to alter the VID code and offset while DVC is enabled.

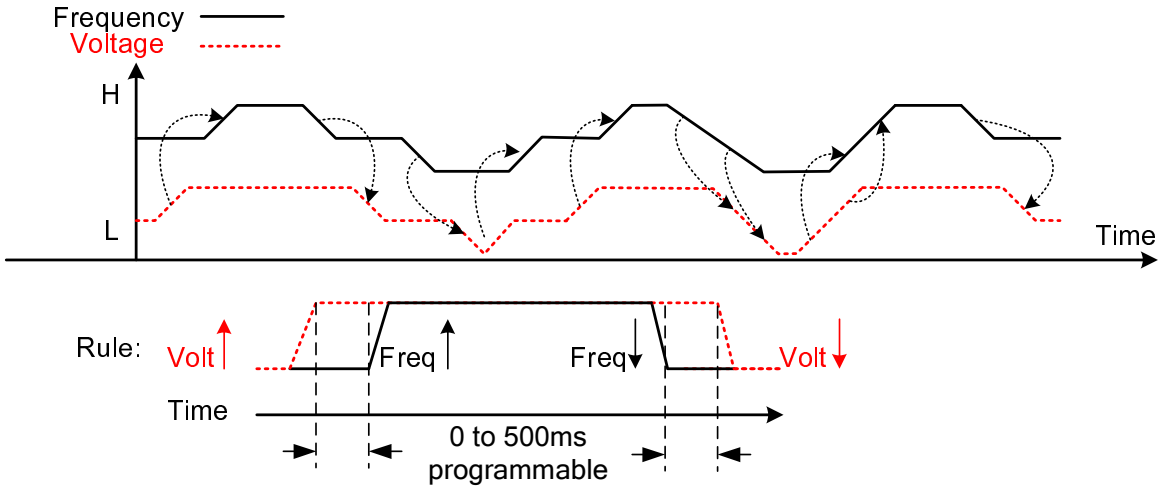


Figure 13 – Output Voltage and Clock Frequency Change Timing

If selected, VID lock will occur when the VR READY delay period ends if SMBus DVC programming ocurred prior to VR powerup. If SMBus DVC is programmed after VR powerup and the default 60ms VR_READY delay then VID lock will occur upon the enable of DVC mode. To ensure consistent VID lock behavior it is recommended to use SMBus to lock out the SVID VID and program a suitable VID prior to enabling DVC mode.

An additional SMBus programmable option is to exit DVC mode if a PS1, 2, 3 or Set VID Decay command is received. In this case DVC operation resumes 250us after returning to the PS0 power state. If VR_READY1 or VR_HOT# are de-asserted for any reason DVC control will return to the DVC00 level. Upon re-assertion DVC operation resumes.

To ensure proper operation, if SMBus DVC programming occurs after VR power up all other DVC registers should be programmed prior to enabling DVC mode.

Serial Communication Interfaces

IDTP63131/IDTP63133 includes three serial interfaces for communication with other system components;

1. VR12/IMVP-7 SVID Intel proprietary interface. Refer to Intel documentation for more information. Some optional SVID registers that are unsupported in IDTP63131, IDT63133 will return 00h.

2. SMBUs Interface: SMBus (System Management Bus) version 2.0, August 3, 2000 compatible interface that allows most IDTP63131/IDTP63133 features to be software programmable. IDTP63131/IDTP63133 acts in slave mode only. The SMBus version 2.0 specification can be accessed from http://smbus.org/specs/. The IDTP63131/IDTP63133 SMBus address is 3C hexidecimal or 0011 1100 in binary format. The SMBus maximum operating frequency is 400kHz.

3. SIF Interface: IDT proprietary interface whose protocol matches that of SMBus but with a 666.7khz clock frequency and with 750Ω pull-up resistors integrated into the IDTP63131/IDTP63133. This interface is used to communicate the VR status to the ICS9CPS4592 clock generator IC. IDTP63131/IDTP63133 acts in master mode and ICS9CPS4592 acknowleges commands only so SIF traffic is essentially one way.

SMBUS and SVID Register Overview

All registers including SVID are accesible through the SMBUS interface. SVID registers are mapped so that a read/write through the SVID bus will access the appropriate register using the supplied SVID address and offset.The following codes are used below to describe register types:

Type	Description
ReadWrite	Read/Write: Register bit may be written and read by the user
ReadClear	Read Clear: Register bit may not be written by user (writes are ignored), but are set by the IDTP63131/IDTP63133. When read by the user, the bit will be cleared.
ReadOnly	Read Only: Register bit may not be written by user (writes are ignored), but are set by the IDTP63131/IDTP63133. When read by the user, the bit retains its value.
WriteOnly	Write Only: Writing the register initiates some sort of one-time action. Reading the register always returns 00h
R/W or RO	Read/Write or Read Only: Depending on the value of a controlling bit, this register may or may not be written. It may always be read.

The following tables provide detailed descriptions of the IDTP63131/IDTP63133 SMBus and SVID registers. The SMBus register offset is provided in hexidecimal format in the top left corner of each table.

SMBus Control Registers

Six control registers change the mode of operation

00h	DEVICE CONTRL 1			
Bit	**Name**	**Control Function**	**Type**	**Default**
7	SOFT RESET	Write 1 to reset all status registers to defaults and begin soft start for both Rails (identical to resetting via either enable pin). Writing a 1 is not stored so subsequent soft reset only requires writing another 1 to this bit.	WriteOnly	0b
6:5	Reserved			
4:2	SVID ADDRESS	Specifies the SVID addresses of rail 1 & rail 2 • 000b = Rail1 Address = 00h, Rail 2 address = 01h • 001b = Rail1 Address = 02h, Rail 2 address = 03h • 010b = Rail1 Address = 04h, Rail 2 address = 05h • 011b = Rail1 Address = 06h, Rail 2 address = 07h • 100b = Rail1 Address = 08h, Rail 2 address = 09h • 101b = Rail1 Address = 0Ah, Rail 2 address = 0Bh • 110b = Rail1 Address = 0Ch, Rail 2 address = 0Dh • 111b = Rail1 Address = 0Eh, Rail 2 address = 0Hh	ReadWrite	000b
1	Reserved			
0	SVID TEST MODE	• 0b = normal mode, SVID returns to rest state if clock is inactive for 625ns (typical) • 1b = test mode, SVID returns to rest state if clock is inactive for 10us (typical)	ReadWrite	0b

01h	DEVICE CONTROL 2			
Bit	**Name**	**Control Function**	**Type**	**Default**
7	RAIL2 VID WRITE ENABLE	Controls how the R2_VID register is written. • 0: RAIL2_VID and RAIL2_SVID_OFFSET are modified only by SVID commands, and become read only through SMBUS. • 1: RAIL2_VID and R2_SVID_OFFSET ignore SVID commands and may only be modified thru SMBUS	ReadWrite	0b
6	RAIL1 VID WRITE ENABLE	Controls how the R1_VID register is written. • 0: R1_VID and R1_SVID_OFFSET are modified only by SVID commands, and become read only through SMBUS. • 1: R1_VID and R1_SVID_OFFSET ignore SVID commands and may only be modified thru SMBUS	ReadWrite	0b
5	SIF ENABLE	SIF Interface Select • 0b = Disable • 1b = Enable	ReadWrite	0b
4	GPO ENABLE	GPO Interface Select • 0b = Disable • 1b = Enable If SIF_EN=1b then this bit is ignored.	ReadWrite	0b
3:0	SIF COMMAND ENABLE	If SIF_CMD_EN[N] = 0, SIF command N is disabled. • 3: OCP • 2: OVP • 1: VR_HOT • 0: Rail 1 PS transition (new level in data)	ReadWrite	1111b

02h	DEVICE CONTROL 3			
Bit	**Name**	**Control Function**	**Type**	**Default**
7	Reserved			
6	RAIL1 PHASE3 ENABLE	Rail 1 Phase #3 enable/disable for VR debug. Phase timing not modified. • 0b = Disable • 1b = Enable	ReadWrite	1b
5	RAIL1 PHASE2 ENABLE	Rail 1 Phase #2 enable/disable for VR debug. Phase timing not modified. • 0b = Disable • 1b = Enable	ReadWrite	1b
4	RAIL1 PHASE1 ENABLE	Rail 1 Phase #1 enable/disable. This phase is always enabled if Rail 1 is enabled • 0b = Disable • 1b = Enable	ReadOnly	1b
3	Reserved			
2	RAIL2 ENABLE	Rail 2 enable/disable • 0b = Disable • 1b = Enable	ReadOnly	1b
1	RAIL2 DROOP ENABLE	Enables DROOP current generation for Rail 2. When disabled, current from the DROOP circuitry is forced to 0. • 0b = Disable • 1b = Enable	ReadWrite	1b
0	RAIL1 DROOP ENABLE	Enables DROOP current generation for Rail 1. When disabled, current from the DROOP circuitry is forced to 0. • 0b = Disable • 1b = Enable	ReadWrite	1b

03h	DEVICE CONTROL 4			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:6	RAIL2 SOFT START SLEW RATE	Rail 2 soft start ramp rate control • 00b = 0.625 mV/us • 01b = 1.250 mV/us • 10b = 2.500 mV/us • 11b = 3.750 mV/us	ReadWrite	10b
5:4	RAIL1 SOFT START SLEW RATE	Rail 1 soft start ramp rate control • 00b = 0.625 mV/us • 01b = 1.250 mV/us • 10b = 2.500 mV/us • 11b = 3.750 mV/us	ReadWrite	10b
3:2	OVER CURRENT THRESHOLD	Over current detection trip point selection. Common control for both Rails, but the ocp trip point is set for Rail 1 by IMAX1 and for Rail 2 by IMAX2 • 00b: I_{OCAVG} = 1.25 x I_{MAX}, I_{OCPH} = 1.50 x I_{MAX} / #ph, $I_{OCEXITPS}$ = 1.2 x I_{MAX} / #ph • 01b: I_{OCAVG} = 1.50 * I_{MAX}, I_{OCPH} = 1.80 * I_{MAX} / #ph, $I_{OCEXITPS}$ = 1.44 x I_{MAX} / #ph • 10b: I_{OCAVG} = 1.75 * I_{MAX}, I_{OCPH} = 2.10 * I_{MAX} / #ph, $I_{OCEXITPS}$ = 1.68 x I_{MAX} / #phase • 11b: I_{OCAVG} = 2.00 * I_{MAX}, I_{OCPH} = 2.30 * I_{MAX} / #ph, $I_{OCEXITPS}$ = 1.92 x I_{MAX} / #ph	ReadWrite	00b
1:0	Reserved			

04h	DEVICE CONTR0L 5			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:6	R2_ PS2_OFS	Trim for Rail 2 pulse skipping thresholds(Coarse adj): Higher threshold gives more skipping • 00b: Default • 01b: Shift pulse skip thresholds down by 0.125V • 10b: Shift pulse skip thresholds up by 0.125V • 11b: Shift pulse skip thresholds up by 0.25V	ReadWrite	00b
5:4	R2_ PS2_RBOT	Trim for Rail 2 pulse skipping thresholds(fine adj) Larger ramp bottom shift gives more skipping: • 00b: 90mV Default • 01b: 120mV • 10b: 60mV • 11b: 30mV	ReadWrite	00b
3:2	R1_ PS2_OFS	Trim for Rail 1 pulse skipping thresholds(Coarse adj): Higher threshold gives more skipping • 00b: Default • 01b: Shift pulse skip thresholds down by 0.125V • 10b: Shift pulse skip thresholds up by 0.125V • 11b: Shift pulse skip thresholds up by 0.25V	ReadWrite	00b
1:0	R1_ PS2_RBOT	Trim for Rail 1 pulse skipping thresholds(fine adj) Larger ramp bottom shift gives more skipping: • 00b: 90mV Default • 01b: 120mV • 10b: 60mV • 11b: 30mV	ReadWrite	00b

Device Status Registers

Three registers provide information on VR status

05h	RAIL1 STATUS			
Bit	**Name**	**Control Function**	**Type**	**Default**
7	RAIL1 OVER VOLTAGE PROTECTION ALERT	Asserted when an OVP shutdown has occurred. • 0b = Normal • 1b = Warning	ReadClear	0b
6	RAIL1 OVER CURRENT PROTECTION ALERT	Asserted when an OCP shutdown has occurred. • 0b = Normal • 1b = Warning	ReadClear	0b
5	RAIL1 UNDER VOLTAGE PROTECTION ALERT	• 0b = Normal • 1b = Warning	ReadClear	0b
4	RAIL1 VRHOT ALERT	• 0b = Normal • 1b = Warning Always 0 if THERM_EN (register 0Ch bit 4) is low	ReadClear	0b
3	RAIL1 ENABLED	Indicates whether or not Rail 1 is enabled • 0b = Disable • 1b = Enable	ReadOnly	1b
2	RAIL1 OVER CURRENT PROTECTION WARNING	Asserted when an over-current condition has been detected and hiccup mode has been entered. • 0b = Normal, 1b = Warning	ReadClear	0b
1	RAIL1 OVER VOLTAGE PROTECTION WARNING	Asserted when an over-voltage condition has been detected, even if that event does not lead to shutdown (as with some soft start situations).. • 0b = Normal • 1b = Warning	ReadClear	0b
0	Reserved			

06h	RAIL2 STATUS			
Bit	**Name**	**Control Function**	**Type**	**Default**
7	RAIL2 OVER VOLTAGE PROTECTION ALERT	Asserted when an OVP shutdown has occurred. • 0b = Normal • 1b = Warning	ReadClear	0b
6	RAIL2 OVER CURRENT PROTECTION ALERT	Asserted when an OCP shutdown has occurred. • 0b = Normal • 1b = Warning	ReadClear	0b
5	RAIL2 UNDER VOLTAGE PROTECTION ALERT	• 0b = Normal • 1b = Warning	ReadClear	0b
4	RAIL2 VRHOT ALERT	• 0b = Normal • 1b = Warning Always 0 if THERM_EN (register OCh bit 5) is low.	ReadClear	0b
3	RAIL2 ENABLED	Indicates whether or not Rail 2 is enabled • 0b = Disable • 1b = Enable	ReadOnly	1b
2	RAIL2 OVER CURRENT PROTECTION WARNING	Rail 2 Over-Current Protection Warning Asserted when an over-current condition has been detected and hiccup mode has been entered • 0b = Normal • 1b = Warning	ReadClear	0b
1	RAIL2 OVER VOLTAGE PROTECTION WARNING	Asserted when an over-voltage condition has been detected, even if that event does not lead to shutdown (as with some soft start situations). • 0b = Normal • 1b = Warning	ReadClear	0b
0	Reserved			

07h	PHASE STATUS			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:6	RAIL1 ACTIVE PHASE NUMBER	Number of Rail 1 phases currently active. This will always be equal to the sum of 1's in register DEVICE CONTROL 3 (02h) bits 7:4 unless Rail 1 is in DEC, PS1, or PS2 mode. • 00b = 1 phase • 01b = 2 phases • 10b = 3 phases • 11b = 4 phases	ReadOnly	N/A
5:0	Reserved			

VID Code Registers

Three registers control and program output voltage settings

08h	VID CONTROL			
Bit	**Name**	**Control Function**	**Type**	**Default**
7	Reserved			
6	RAIL2 SVID ENABLE	Determines whether SVID commands control the Rail2 output voltage or not . • If high, changes to the Rail 2 VID register (SMBus DDh) are copied to the Rail 2 DAC VID register (SMBus 09h). • If low, changes to the Rail 2 VID register (SMBus DDh) are copied to the Rail 2 DAC VID register (SMBus 09h).	ReadWrite	1b
5	RAIL1 SVID ENABLE	Determines whether SVID commands control the Rail1 output voltage or not . • If high, changes to the Rail 1 VID register (SMBus DDh) are copied to the Rail 1 DAC VID register (SMBus 0Ah). • If low, changes to the Rail 1 VID register (SMBus DCh) are copied to the Rail 1 DAC VID register (SMBus 0Ah).	ReadWrite	1b
4	RAIL2 VID FIXED DVC00 OFFSET ENABLE	Allows the offset stored in DVC00 RAIL2 VID OFFSET (SMBus register 38h) to be applied as a fixed VID offset if the Rail 2 DVC function is not enabled (SMBus register 30h bit 6 =0b). • 0b = Disable • 1b = Enable	ReadWrite	0b
3	RAIL1 VID OFFSET ENABLE	Allows the offset stored in DVC00 RAIL1 VID OFFSET (SMBus register 34h) to be applied as a fixed VID offset if the Rail 1 DVC function is not enabled (SMBus register 30h bit 7 =0b). • 0b = Disable • 1b = Enable	ReadWrite	0b
2:0	Reserved			

09h	RAIL2 VID DAC STATUS			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL2 DAC VID	Current VID input setting of DAC for Rail 2	ReadOnly	00b

0Ah	RAIL1 VID DAC STATUS			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL1 DAC VID	Current VID input setting of DAC for Rail 1	ReadOnly	00b

UVP and OVP Register

Adjust the output under and overvoltage thresholds

0Bh	UVP AND OVP THRESHOLD ADJUST			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:6	RAIL2 OVER VOLTAGE PROTECTION OFFSET	Rail 2 Over-Voltage Protection Threshold VID Offset • 00b = 150mV • 01b = 200mV • 10b = 250mV • 11b = 300mV	ReadWrite	01b
5:4	RAIL2 UNDER VOLTAGE PROTECTION LEVEL	Rail 2 Under Voltage Protection Level: • 00 = 80% • 01 = 70% • 10 = 60% • 11 = 50% Hysteresis is 10% for all options. UV is cleared when the voltage rises to UV trip+10% of the VID setting	ReadWrite	10b
3:2	RAIL1 OVER VOLTAGE PROTECTION OFFSET	Rail 1 Over-Voltage Protection Threshold VID Offset • 00b = 150mV • 01b = 200mV • 10b = 250mV • 11b = 300mV	ReadWrite	01b
1:0	RAIL1 UNDER VOLTAGE PROTECTION LEVEL	Rail 1 Under Voltage Protection Level: • 00 = 80% • 01 = 70% • 10 = 60% • 11 = 50% Hysteresis is 10% for all options. UV is cleared when the voltage rises to UV trip+10% of the VID setting	ReadWrite	10b

Thermal Monitor and Temperature Compensation Register

Enable thermal compensation and VR_HOT operation

0Ch	THERMAL CONTROL			
Bit	**Name**	**Control Function**	**Type**	**Default**
7	RAIL2 THERMAL COMPENSATION ENABLE	Enable Rail 2 Internal Temperature Compensation. Set at startup by the OSC resistor connection • 0b = Disable (OSC resistor to VDD) • 1b = Enable (OSC resistor to GND)	ReadWrite	0b
6	RAIL1 THERMAL COMPENSATION ENABLE	Enable Rail 1 Internal Temperature Compensation Set at startup by the IREF resistor connection • 0b = Disable (IREF resistor to VDD) • 1b = Enable (IREF resistor to GND)	ReadWrite	0b
5	RAIL2 VRHOT ENABLE	Enables Rail 2 thermal overstress detection when high. When low, VR_HOT# stay high. • 0b = Disable • 1b = Enable	ReadWrite	1b
4	RAIL1 VRHOT ENABLE	Enables Rail 1 thermal overstress detection when high. When low, VR_HOT# stay high. • 0b = Disable • 1b = Enable	ReadWrite	1b
3:0	Reserved			

DEC Registers

Thirteen registers enable and configure Dynamic Efficiency Control (DEC) operation

20h	DEC CONTROL			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:6	Reserved			
5	RAIL1 DEC ENABLE	Rail 1 DEC Control • 0b = Disable • 1b = Enable	ReadWrite	0b
4	RAIL1 DEC PS2	Rail 1 DEC PS2 Control. Automatically enter pulse skipping mode when the lowest DEC threshold is reached for Rail 2 (1 phase operation) • 0b = Disable • 1b = Enable If R1_DEC1_EN = 0, R1_DEC_PS2 has no effect.	ReadWrite	1b
3:2	RAIL1 PS1 PHASE NUMBER	Control for minimum number of phases to be used in PS1 mode for Rail 1. If a PS2/3 command is received, the minimum phase number is over-ridden and the controller drops to 1 phase operation to allow pulse skipping and diode emulation modes. • 00b/01b = 1 phase • 10b = 2 phases • 11b = 3 phases	ReadWrite	01b
1:0	RAIL1 DEC PHASE NUMBER	Control for minimum number of phases to be used in DEC mode for Rail 1. If a PS2/3 command is received, the minimum phase number is over-ridden, and the controller drops to 1 phase operation to allow pulse skipping and diode emulation modes. • 00b/01b = 1 phase • 10b = 2 phases • 11b = 3 phases	ReadWrite	01b

21h	RAIL1 DEC SOFT START DELAY			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL1 DEC SOFT START DELAY	Delay after soft start after which DEC operations can occur for Rail 1, 4ms/per LSB.	ReadWrite	0Fh

22h	RAIL1 DEC WINDOW			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL1 DEC WINDOW	Rail 1 DEC detection window, 4ms/per LSB.	ReadWrite	0Fh

23h	RAIL1 DEC LEVEL 1H			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL1 DEC LEVEL 1 HIGH	Transition current level is given by I_{MAX_R1} * (LEVEL[7:0] + 1)/256	ReadWrite	00h

24h	RAIL1 DEC LEVEL 1L			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL1 DEC LEVEL 1 LOW	Transition current level is given by I_{MAX_R1} * (LEVEL[7:0] + 1)/256	ReadWrite	00h

25h	RAIL1 DEC LEVEL 2H			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL1 DEC LEVEL 2 HIGH	Transition current level is given by I_{MAX_R1} * (LEVEL[7:0] + 1)/256	ReadWrite	00h

26h	RAIL1 DEC LEVEL 2L			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL1 DEC LEVEL 2 LOW	Transition current level is given by I_{MAX_R1} * (LEVEL[7:0] + 1)/256	ReadWrite	00h

DVC Registers

Eighteen registors enable and configure Dynamic Voltage Control (DVC) operation

30h	DVC CONTROL			
Bit	**Name**	**Control Function**	**Type**	**Default**
7	RAIL1 DVC ENABLE	Enable Rail 1 DVC operation • 0b =Disable • 1b=Enable If R1_DVC_EN=1 and DVID_EN=0 (reg 08h) PS1, 2, and 3 commands do not effect VR operation	ReadWrite	0b
6	RAIL2 DVC ENABLE	Enable Rail 2 DVC operation • 0b =Disable • 1b=Enable If R2_DVC_EN=1 and DVID_EN=0 (reg 08h) PS1, 2, and 3 commands do not effect VR operation	ReadWrite	0b
5	RAIL2 DVC ALERT ENABLE	By default when R2_DVC_EN=1 then alerts from Rail2 will cause the system to return to DVC/DFC00. This operation can be disabled by setting field to “0”	ReadWrite	1b
4	DVC DVID ENABLE	• 0b = DVID commands and SVID offset commands are ignored while in DVC mode • 1b = DVID commands and SVID offset commands are allowed while in DVC mode	ReadWrite	1b
3	DVC PS ENABLE	• 0b = changing to PS1,2, or 3 will exit DVC mode until the part returns to PS0 • 1b = Power State changes allowed in DVC mode	ReadWrite	0b
4:0	Reserved			

31h	DVC WINDOW			
Bit	**Name**	**Control Function**	**Type**	**Default**
7	Reserved			
6:0	DVC WINDOW	DVC detection window, 1ms/per LSB. Window filter is activated on when a threshold level is crossed.	ReadWrite	0Fh

32h	DVC DFC DELAY			
Bit	**Name**	**Control Function**	**Type**	**Default**
7	Reserved			
6:0	DVC DFC DELAY	DVC/DFC delay time control register. When DVC indicates that Rail1 voltage needs to be lowered, the DVC information is sent to the clock IC and the timer is started (4ms/bit). On timer completion, the output voltage is lowered.	ReadWrite	0Fh

33h	DVC SOFT START DELAY			
Bit	**Name**	**Control Function**	**Type**	**Default**
7	Reserved			
6:0	DVC SOFT START DELAY	Delay after soft start after which DVC operations can occur, 4ms/per LSB.	ReadWrite	0Fh

34h	DVC00 RAIL1 VID OFFSET			
Bit	**Name**	**Control Function**	**Type**	**Default**
7	DVC00 RAIL1 VID OFFSET	• 0b = positive offset • 1b = negative offset	ReadWrite	0b
6:0	DVC00 RAIL1 VID OFFSET	Magnitude of the offset (1 LSB = 5 mV)	ReadWrite	00h

35h	DVC01 RAIL1 VID OFFSET			
Bit	**Name**	**Control Function**	**Type**	**Default**
7	DVC01 RAIL1 VID OFFSET POLARITY	• 0b = positive offset • 1b = negative offset	ReadWrite	0b
6:0	DVC01 RAIL1 VID OFFSET	Magnitude of the offset (1 LSB = 5 mV)	ReadWrite	00h

36h	DVC10 RAIL1 VID OFFSET			
Bit	**Name**	**Control Function**	**Type**	**Default**
7	DVC10 RAIL1 VID OFFSET POLARITY	• 0b = positive offset • 1b = negative offset	ReadWrite	0b
6:0	DVC10 RAIL1 VID OFFSET	Magnitude of the offset (1 LSB = 5 mV)	ReadWrite	00h

37h	DVC11 RAIL1 VID OFFSET			
Bit	**Name**	**Control Function**	**Type**	**Default**
7	DVC11 RAIL1 VID OFFSET POLARITY	• 0b = positive offset • 1b = negative offset	ReadWrite	0b
6:0	DVC11 RAIL1 VID OFFSET	Magnitude of the offset (1 LSB = 5 mV)	ReadWrite	00h

38h	DVC00 RAIL2 VID OFFSET			
Bit	**Name**	**Control Function**	**Type**	**Default**
7	DVC00 RAIL2 VID OFFSET POLARITY	• 0b = positive offset • 1b = negative offset	ReadWrite	0b
6:0	DVC00 RAIL2 VID OFFSET	Magnitude of the offset (1 LSB = 5 mV)	ReadWrite	00h

39h	DVC01 RAIL2 VID OFFSET			
Bit	**Name**	**Control Function**	**Type**	**Default**
7	DVC01 RAIL2 VID OFFSET POLARITY	• 0b = positive offset • 1b = negative offset	ReadWrite	0b
6:0	DVC01 RAIL2 VID OFFSET	Magnitude of the offset (1 LSB = 5 mV)	ReadWrite	00h

3Ah	DVC10 RAIL2 VID OFFSET			
Bit	**Name**	**Control Function**	**Type**	**Default**
7	DVC10 RAIL2 VID OFFSET POLARITY	• 0b = positive offset • 1b = negative offset	ReadWrite	0b
6:0	DVC10 RAIL2 VID OFFSET	Magnitude of the offset (1 LSB = 5 mV)	ReadWrite	00h

3Bh	DVC11 RAIL2 VID OFFSET			
Bit	**Name**	**Control Function**	**Type**	**Default**
7	DVC11 RAIL2 VID OFFSET POLARITY	• 0b = positive offset • 1b = negative offset	ReadWrite	0b
6:0	DVC11 RAIL2 VID OFFSET	Magnitude of the offset (1 LSB = 5 mV)	ReadWrite	00h

3Ch	DVC LEVEL 1H			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	DVC LEVEL 1 HIGH	Transition current level is given by I_{MAX_R1} * (LEVEL[7:0] + 1)/256	ReadWrite	00h

3Dh	DVC LEVEL 1L			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	DVC LEVEL 1 LOW	Transition current level is given by I_{MAX_R1} * (LEVEL[7:0] + 1)/256	ReadWrite	00h

3Eh	DVC LEVEL 2H			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	DVC LEVEL 2 HIGH	Transition current level is given by I_{MAX_R1} * (LEVEL[7:0] + 1)/256	ReadWrite	00h

3Fh	DVC LEVEL 2L			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	DVC LEVEL 2 LOW	Transition current level is given by I_{MAX_R1} * (LEVEL[7:0] + 1)/256	ReadWrite	00h

40h	DVC LEVEL 3H			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	DVC LEVEL 3 HIGH	Transition current level is given by I_{MAX_R1} * (LEVEL[7:0] + 1)/256	ReadWrite	00h

41h	DVC LEVEL 3L			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	DVC LEVEL 3 LOW	Transition current level is given by I_{MAX_R1} * (LEVEL[7:0] + 1)/256	ReadWrite	00h

SVID Registers (see Intel documents for SVID command index)

A0h	VENDOR IDENTIFICATION			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	VENDOR IDENTIFICATION	Intel assigned VR vendor ID for IDT	ReadOnly	28h

A1h	PRODUCT IDENTIFICATION			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	PRODUCT IDENTIFICATION	IDT assigned product ID for IDTP63131	ReadOnly	01h

95h	PRODUCT REVISION NUMBER			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	PRODUCT REVISION	IDT assigned product revision number	ReadOnly	0Ah

A3h	PRODUCT DATE			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	PRODUCT DATE	Indentifies the manufacturing date code. This is an optional SVID register and is hard coded to 00h.	ReadOnly	00h

A4h	LOT CODE			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	LOT CODE	Indentifies part lot code. This is an optional SVID register and is hard coded to 00h.	ReadOnly	00h

A5h	PROTOCOL VERSION			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	PROTOCOL IDENTIFICATION	Identifies supported version of SVID protocol	ReadOnly	01h

A6h	RAIL1 CAPABILITY			
Bit	**Name**	**Control Function**	**Type**	**Default**
7	RAIL1 OUTPUT CURRENT ADC TYPE	Digitized output current FFh is equivalent to IMAX	ReadOnly	1b
6	RAIL1 TEMPERATURE	Digitized temperature register is supported	ReadOnly	1b
5	RAIL1 INPUT POWER	Digitized input power register is not supported	ReadOnly	0b
4	RAIL1 INPUT VOLTAGE	Digitized input voltage register is not supported	ReadOnly	0b
3	RAIL1 INPUT CURRENT	Digitized input current register is not supported	ReadOnly	0b
2	RAIL1 OUTPUT POWER	Digitized output power register is not supported	ReadOnly	0b
1	RAIL 1 OUTPUT VOLTAGE	Digitized output voltage register is not supported	ReadOnly	0b
0	RAIL1 OUTPUT CURRENT	Digitized output current register is supported	ReadOnly	1b

A7h	RAIL2 CAPABILITY			
Bit	**Name**	**Control Function**	**Type**	**Default**
7	RAIL2 OUTPUT CURRENT ADC TYPE	Digitized output current FFh is equivalent to IMAX	ReadOnly	1b
6	RAIL2 TEMPERATURE	Digitized temperature register is supported	ReadOnly	1b
5	RAIL2 INPUT POWER	Digitized input power register is not supported	ReadOnly	0b
4	RAIL2 INPULT VOLTAGE	Digitized input voltage register is not supported	ReadOnly	0b
3	RAIL2 INPUT CURRENT	Digitized input current register is not supported	ReadOnly	0b
2	RAIL2 OUTPUT POWER	Digitized output power register is not supported	ReadOnly	0b
1	RAIL2 OUTPUT VOLTAGE	Digitized output voltage register is not supported	ReadOnly	0b
0	RAIL2 OUTPUT CURRENT	Digitized output current register is supported	ReadOnly	1b

B0h	RAIL1 STATUS 1			
Bit	**Name**	**Control Function**	**Type**	**Default**
7	RAIL1 READ STATUS 2	A value of 1b indicates that the R1_STATUS_2 register should be read (there has been an error on the SVID bus). This register is cleared after a GetReg(R1_STATUS_2)	ReadOnly	0b
6:3	Reserved			
2	RAIL1 ICC_ MAX ALERT	Indicates ICC Max Alert Status: 0b = IOUT < ICC_MAX 1b = IOUT > = ICC_MAX	ReadOnly	0b
1	RAIL1 THERMAL ALERT	Indicates Thermal Alert Status. The thermal alert asserts when the Rail 1 temp sensor shows 97% of TEMP_MAX and de-assert at 94% of TEMP_MAX. 0b = Temp <= TEMP_MAX * 0.94 1b = Temp >= TEMP_MAX * 0.97	ReadOnly	0b
0	RAIL1 VR_SETTLED ALERT	Indicates VR Settled Status: 0b = VR is ramping 1b = VR is at target voltage	ReadOnly	0b

B1h	RAIL2 STATUS 1			
Bit	**Name**	**Control Function**	**Type**	**Default**
7	RAIL2 READ STATUS 2	A value of 1b indicates that the R2_STATUS_2 register should be read (there has been an error on the SVID bus). This register is cleared after a GetReg(R2_STATUS_2)	ReadOnly	0b
6:3	Reserved			
2	RAIL2 ICC_MAX ALERT	Indicates ICC Max Alert Status: 0b = IOUT < ICC_MAX 1b = IOUT > = ICC_MAX	ReadOnly	0b
1	RAIL2 THERMAL ALERT	Indicates Thermal Alert Status. The thermal alert asserts when the Rail 2 temp sensor shows 97% of TEMP_MAX and de-assert at 94% of TEMP_MAX. 0b = Temp <= TEMP_MAX * 0.94 1b = Temp >= TEMP_MAX * 0.97	ReadOnly	0b
0	RAIL2 VR_SETTLED ALERT	Indicates VR Settled Status: 0b = VR is ramping 1b = VR is at target voltage	ReadOnly	0b

B2h	RAIL1 STATUS 2			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:2	Reserved			
1	RAIL1 SVID DATA ERROR	0b = No error 1b = SVID data frame error	ReadClear	0b
0	RAIL1 SVID PARITY ERROR	0b = No error 1b = SVID parity error	ReadClear	0b

B3h	RAIL2 STATUS 2			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:2	Reserved			
1	RAIL2 SVID DATA ERROR	0b = No error 1b = SVID data frame error	ReadClear	0b
0	RAIL2 SVID PARITY ERROR	0b = No error 1b = SVID parity error	ReadClear	0b

B4h	RAIL1 TEMPERATURE ZONE			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL1 TEMPERATURE ZONE	Provides the current temp zone for Rail1	ReadOnly	00h

B5h	RAIL2 TEMPERATURE ZONE			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL2 TEMPERATURE ZONE	Provides the current temp zone for Rail2	ReadOnly	00h

B6h	RAIL1 CURRENT ZONE			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL1 CURRENT ZONE	00h indicates not supported	ReadOnly	00h

B7h	RAIL2 CURRENT ZONE			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL2 CURRENT ZONE	00h indicates not supported	ReadOnly	00h

B8h	RAIL1 OUTPUT CURRENT			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL1 OUTPUT CURRENT	Digitized total output current, binary encoded as load current as a % of IMAX for Rail 1	ReadOnly	01h

B9h	RAIL2 OUTPUT CURRENT			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL2 OUTPUT CURRENT	Digitized total output current, binary encoded as load current as a % of IMAX for Rail 2	ReadOnly	01h

BAh	RAIL1 OUTPUT VOLTAGE			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL1 OUTPUT VOLTAGE	00h indicates not supported	ReadOnly	00h

BBh	RAIL2 OUTPUT VOLTAGE			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL2 OUTPUT VOLTAGE	00h indicates not supported	ReadOnly	00h

BCh	RAIL1 TEMPERATURE			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL1 TEMPERATURE	8 bit binary word ADC of VR temperature measured at sensor 1, binary format in deg C, IE 65C=41h.	ReadOnly	41h

BDh	RAIL2 TEMPERATURE			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL2 TEMPERATURE	8 bit binary word ADC of VR temperature measured at sensor 2, binary format in deg C, IE 65C=41h.	ReadOnly	41h

BEh	RAIL1 OUTPUT POWER			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL1 OUTPUT POWER	00h indicates not supported	ReadOnly	00h

BFh	RAIL2 OUTPUT POWER			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL2 OUTPUT POWER	00h indicates not supported	ReadOnly	00h

C0h	RAIL1 INPUT CURRENT			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL1 INPUT CURRENT	00h indicates not supported	ReadOnly	00h

C2h	RAIL1 INPUT VOLTAGE			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL1 INPUT VOLTAGE	00h indicates not supported	ReadOnly	00h

C3h	RAIL2 INPUT VOLTAGE			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL2 INPUT VOLTAGE	00h indicates not supported	ReadOnly	00h

C4h	RAIL1 INPUT POWER			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL1 INPUT POWER	00h indicates not supported	ReadOnly	00h

C5h	RAIL2 INPUT POWER			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL2 INPUT POWER	00h indicates not supported	ReadOnly	00h

C6h	RAIL1 STATUS 2 PREVIOUS			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL1 STATUS 2 PREVIOUS	This register contains a copy of the status2 data that was last read with the GetReg(status2) command.	ReadOnly	00h

C7h	RAIL2 STATUS 2 PREVIOUS			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL2 STATUS 2 PREVIOUS	This register contains a copy of the status2 data that was last read with the GetReg(status2) command.	ReadOnly	00h

C8h	RAIL1 MAXIMUM CURRENT			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL1 ICC_MAX	Data register containing the Icc max the platform supports. The platform designer programs this value by setting the IMAX resistor value. Binary format in amps. IE 100A=64h.	ReadOnly	N/A

C9h	RAIL2 MAXIMUM CURRENT			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL2 ICC_MAX	Data register containing the Icc max the platform supports. The platform designer programs this value by setting the IMAX resistor value. Binary format in amps. IE 100A=64h	ReadOnly	N/A

CAh	RAIL1 MAXIMUM TEMPERATURE			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL1 TEMP_MAX	Data register containing the temperature max the platform supports and the level VR_hot asserts. The platform design engineer programs this value by setting the TMAX resistor value, accepting the default, or over-riding through SMBUS. Binary format in deg C. IE 100C=64h. This data is used with the temperature zone register.	ReadWrite	6Eh

CBh	RAIL2 MAXIMUM TEMPERATURE			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL2 TEMP_MAX	Data register containing the temperature max the platform supports and the level VR_hot asserts. The platform design engineer programs this value by setting the TMAX resistor value, accepting the default, or over-riding through SMBUS. Binary format in deg C. IE 100C=64h. this data is used with the temperature zone register.	ReadWrite	6Eh

CCh	RAIL1 DC_LL			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL1 DC_LL	00h indicates not supported	ReadOnly	00h

CDh	RAIL2 DC_LL			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL2 DC_LL	00h indicates not supported	ReadOnly	00h

CEh	RAIL1 SLEW RATE FAST			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL1 SR_FAST	Fast slew rate capability. Binary format in mV/us IE 0D=13 mv/us.	ReadOnly	0Dh

CFh	RAIL2 SLEW RATE FAST			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL2 SR_FAST	Fast slew rate capability. Binary format in mV/us IE 0D=13 mv/us.	ReadOnly	0Dh

D0h	RAIL1 SLEW RATE SLOW			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL1 SR_SLOW	Slow slew rate capability. Binary format in mv/us, IE 03h=3mV/us	ReadOnly	03h

D1h	RAIL2 SLEW RATE SLOW			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL2 SR_SLOW	Slow slew rate capability. Binary format in mv/us, IE 03h=3mV/us	ReadOnly	03h

D2h	RAIL1 BOOT VOLTAGE			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL1 VBOOT	Default Vboot voltage is 0V but can over-ride through SMBUS. Coding matches VID table, IE 97h=1.0V.	ReadWrite (SMBus) Read Only (SVID)	00h

D3h	RAIL2 BOOT VOLTAGE			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL2 VBOOT	Default Vboot voltage is 0V but can over-ride through SMBUS. Coding matches VID table, IE 97h=1.0V.	ReadWrite (SMBus) Read Only (SVID)	00h

D4h	RAIL1 VR_TOL			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL VR_TOL	00h indicates not supported	ReadOnly	00h

D5h	RAIL2 VR_TOL			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL2 VR_TOL	00h indicates not supported	ReadOnly	00h

D6h	RAIL1 I_OFFSET			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL1 I_OFFSET	00h indicates not supported	ReadOnly	00h

D7h	RAIL2 I_OFFSET			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL2 I_OFFSET	00h indicates not supported	ReadOnly	00h

D8h	RAIL1 TEMPERATURE OFFSET			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:6	Reserved		ReadWrite	00b
5:0	RAIL1 TEMPERATURE OFFSET	LSB = 1°C offset 1xxxxxb = Negative offset 0xxxxxb = Positive offset Note: 100000b = 000000b= No offset	ReadWrite	000000b

D9h	RAIL2 TEMPERATURE OFFSET			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:6	Reserved		ReadWrite	00b
5:0	RAIL2 TEMPERATURE OFFSET	LSB = 1°C offset 1xxxxxb = Negative offset 0xxxxxb = Positive offset Note: 100000b = 000000b= No offset	ReadWrite	000000b

DAh	RAIL1 VOUT_MAX			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL1 VOUT_MAX	This register is programmable by the master and sets the maximum VID the VR will support. VID Offset does not effect Vout Max. IE VID+SVID_offset can be > Vout max.	ReadWrite	FBh (1.5V)

DBh	RAIL2 VOUT_MAX			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL2 VOUT_MAX	This register is programmable by the master and sets the maximum VID the VR will support. VID Offset does not affect Vout max. IE VID+SVID_offset can be > Vout max.	ReadWrite	FBh (1.5V)

DCh	RAIL1 VID			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL1 VID	Data register containing current programmed VID voltage, VID data format. Default is 00h, zero volts output, VR off. Device control register 2 (01h) determines whether this register is written by SVID or SMBus.	ReadWrite	00h

DDh	RAIL2 VID			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL2 VID	Data register containing current programmed VID voltage, VID data format. Default is 00h, zero volts output, VR off. Device control register 2 (01h) determines whether this register is written by SVID or SMBus.	ReadWrite	00h

DEh	Rail1 POWER STATE			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL1 POWER STATE	Register containing the current programmed power state. Default is 00h, normal power mode.	ReadWrite	00h

DFh	RAIL2 POWER STATE			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL2 POWER STATE	Register containing the current programmed power state. Default is 00h, normal power mode.	ReadWrite	00h

E0h	RAIL1 SVID OFFSET			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL1 SVID OFFSET	Binary format, 2's complement magnitude of the VID code offset (1 LSB = 5 mV), SVID_OFFSET + VID can exceed VOUT_MAX, but cannot exceed 1.52V	ReadWrite	00h

E1h	RAIL2 SVID OFFSET			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL2 SVID OFFSET	Binary format, 2's complement magnitude of the VID code offset (1 LSB = 5 mV), SVID_OFFSET + VID can exceed VOUT_MAX, but cannot exceed 1.52V	ReadWrite	00h

E2h	RAIL1 MULTI VR			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:2	Reserved			
1	RAIL1 LOCK VID AND POWER STATE	0b = Normal mode, not locked 1b = Slave address is locked in the current VID setting and power state setting. It will reject all setVID commands including SetVID(AllCall) and SetPS(AllCall) until such time that the VR is issued a SetPS(00h) returning to normal mode to unlock that VR. Cycling POR, ENABLEA or ENABLEB will also reset to normal mode	ReadWrite	0b
0	RAIL1 VR_READY 0V	0b = VR_READY asserts low if an off code is received. 1b = VR_READ does not assert if an off code is received (0.0V is considered a valid voltage).	ReadWrite	0b

E3h	RAIL2 MULTI VR			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:2	Reserved			
1	RAIL2 LOCK VID AND POWER STATE	0b = Normal mode, not locked 1b = Slave address is locked in the current VID setting and power state setting. It will reject all setVID commands including SetVID(AllCall) and SetPS(AllCall) until such time that the VR is issued a SetPS(00h) returning to normal mode to unlock that VR. Cycling POR, ENABLEA or ENABLEB will also reset to normal mode	ReadWrite	0b
0	RAIL2 VR_READY 0V	0b = VR_READY asserts low if an off code is received. 1b = VR_READ does not assert if an off code is received (0.0V is considered a valid voltage).	ReadWrite	0b

0xe4	R1_SET_REG_ADR			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL1 SET_REG_ADR	Scratch pad register for temporary storage of the SetRegADR pointer register	ReadWrite	00h

0xe5	R2_SET_REG_ADR			
Bit	**Name**	**Control Function**	**Type**	**Default**
7:0	RAIL2 SET_REG_ADR	Scratch pad register for temporary storage of the SetRegADR pointer register	ReadWrite	00h

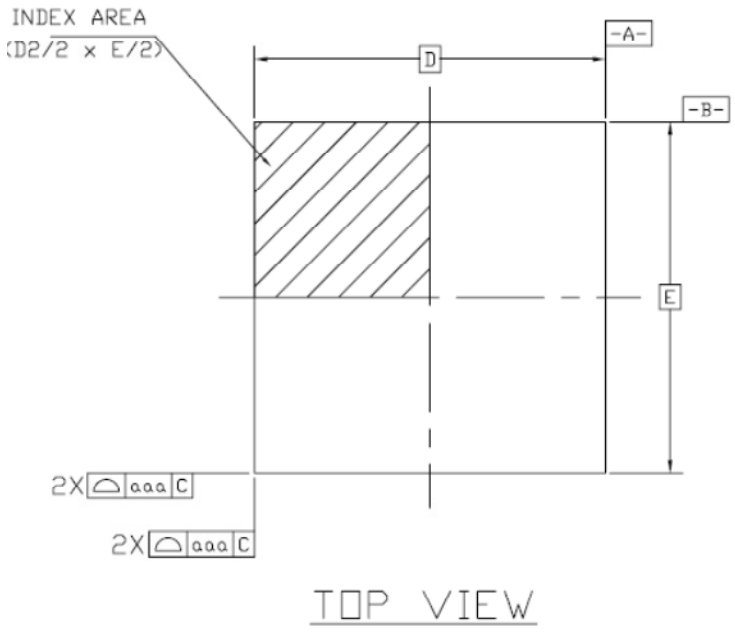
Ordering Information

Part / Order Number	Shipping Packaging	Inductor DCR	Package
IDTP63131-00NDGI	Tray	DCR ≤ 0.7mΩ	Industrial Temp QFN-40
IDTP63131-00NDGI8	Tape and Reel	DCR ≤ 0.7mΩ	Industrial Temp QFN-40
IDTP63133-00NDGI	Tray	DCR ≤ 0.7mΩ	Industrial Temp QFN-40
IDTP63133-00NDGI8	Tape and Reel	DCR ≤ 0.7mΩ	Industrial Temp QFN-40

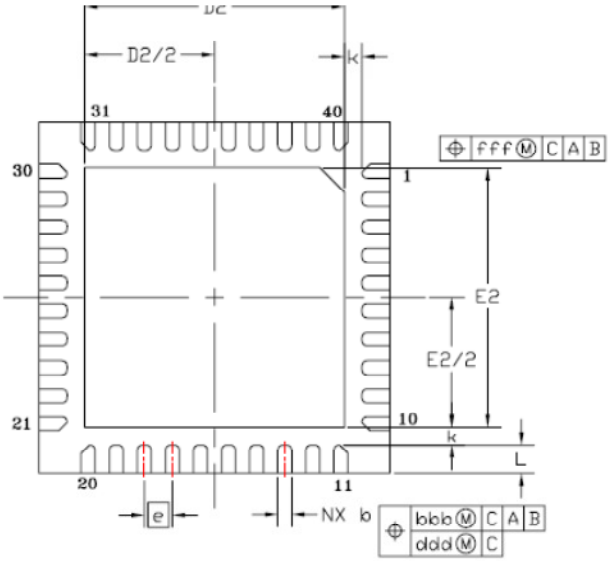
-00 may be replaced with alternate part number for custom configurations, contact IDT.

Package Outline and Package Dimensions (40 Pin QFN)

Package dimensions are consistent with JEDEC Publication No. 95



TOP VIEW



BOTTOM VIEW

SIDE VIEW

SYMBOL	DIMENSION		
	MIN	NOM	MAX
b	0.15	0.20	0.25
D		5.00 BSC	
E		5.00 BSC	
D2	3.55		3.80
E2	3.55		3.80
L	0.30	0.40	0.50
e		0.40 BSC	
N		40	
ND		10 (note 3)	
NE		10 (note 3)	
A	0.80		1.00
A1	0.00	0.02	0.05
A3		0.2 REF	
k		0.25	
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

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