

UHF linear push-pull power transistor

BLV58

FEATURES

- High power gain
- Double stage internal input matching for high input impedance
- Diffused emitter-ballasting resistors enhances ruggedness
- Gold metallization for high reliability.

DESCRIPTION

The BLV58 is a common emitter epitaxial npn silicon planar transistor designed for high linearity class-A operation in UHF (bands 4 and 5) TV transmitters and transposers.

The device is incorporated in a push-pull SOT289 flange envelope with a ceramic cap, which is utilized with the emitters connected to the flange.

PINNING - SOT289

PIN	DESCRIPTION
1	collector 1
2	collector 2
3	base 1
4	base 2
5	emitter

QUICK REFERENCE DATA

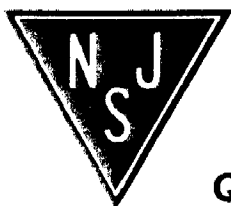
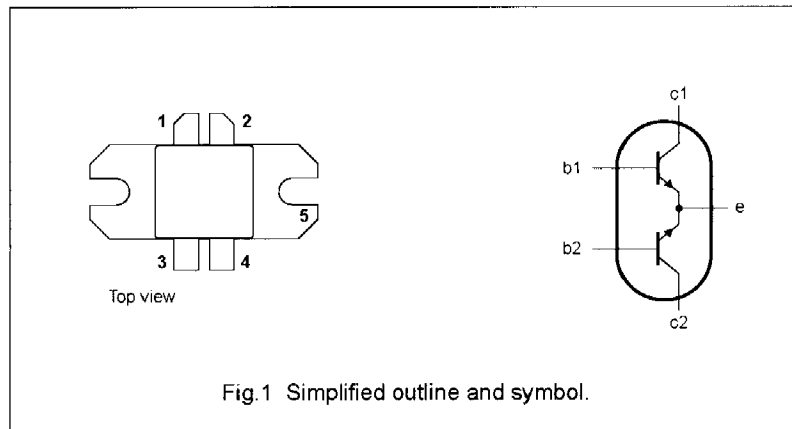
RF performance at $T_h = 25^\circ\text{C}$ in a common emitter test circuit.

MODE OF OPERATION	f_{vision} (MHz)	V_{CE} (V)	I_{CQ} (A)	$P_{\text{o sync}}$ (W)	G_p (dB)	d_{im} (dB) (note 1)
c.w. class-A	860	25	2×1.6	25	>10	<-45

Note

1. Three-tone test method (vision carrier -8 dB, sound carrier -7 dB, sideband signal -16 dB); zero dB corresponds to peak sync level.

PIN CONFIGURATION



NJ Semi-Conductors reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by NJ Semi-Conductors is believed to be both accurate and reliable at the time of going to press. However, NJ Semi-Conductors assumes no responsibility for any errors or omissions discovered in its use. NJ Semi-Conductors encourages customers to verify that datasheets are current before placing orders.

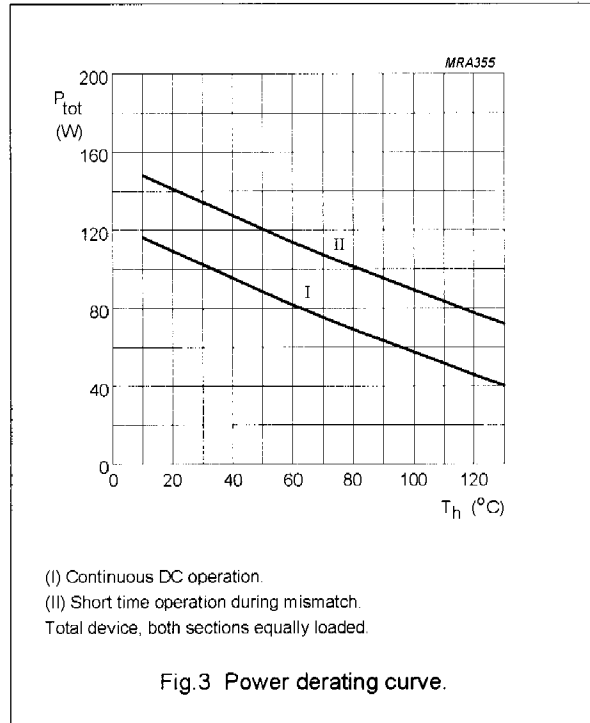
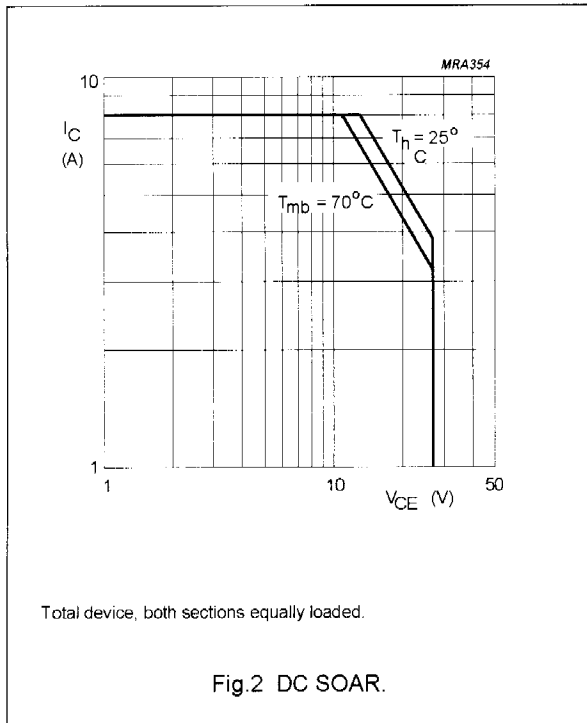
LIMITING VALUES (per transistor section unless otherwise specified)

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	-	50	V
V_{CEO}	collector-emitter voltage	open base	-	27	V
V_{EBO}	emitter-base voltage	open collector	-	3.5	V
$I_C, I_{C(AV)}$	collector current	DC or average value	-	4	A
I_{CM}	collector current	peak value; $f > 1$ MHz	-	8	A
P_{tot}	total power dissipation	DC operation; $T_{mb} = 70^\circ\text{C}$ (note 1)	-	87	W
T_{stg}	storage temperature range		-65	150	$^\circ\text{C}$
T_j	junction operating temperature		-	200	$^\circ\text{C}$

Note

1. Total device, both sections equally loaded.



THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j-mb(DC)}$	from junction to mounting base	$P_{dis} = 87\ W;$ $T_{mb} = 70\ ^\circ C$ (note 1)	1.5	K/W
$R_{th\ mb-h}$	from mounting base to heatsink	note 1	0.2	K/W

Note

1. Total device, both sections equally loaded.

CHARACTERISTICS

Values apply to either transistor section; $T_j = 25\ ^\circ C$.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	open emitter; $I_C = 20\ mA$	50	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; $I_C = 50\ mA$	27	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; $I_E = 10\ mA$	3.5	–	–	V
I_{CES}	collector-emitter leakage current	$V_{BE} = 0;$ $V_{CE} = 27\ V$	–	–	10	mA
h_{FE}	DC current gain	$V_{CE} = 25\ V;$ $I_C = 1.6\ A$	30	–	–	
C_c	collector capacitance	$V_{CB} = 25\ V;$ $I_E = I_e = 0;$ $f = 1\ MHz$	–	36	45	pF

PACKAGE OUTLINE

Flanged ceramic package; 2 mounting holes; 4 leads

SOT289A

