

PRELIMINARY DATA SHEET

SKY13277-355LF: GaAs SP3T Absorptive Switch 500 MHz–2.5 GHz

Features

- Positive voltage control (0/3 V typ.)
- High isolation 62 dB at 1 GHz
- Integrated silicon CMOS driver
- Isolated ports are absorptive
- Available lead (Pb)-free and RoHS-compliant MSL-1 @ 260°C per JEDEC J-STD-020

Description

The SKY13277-355LF is a pHEMT GaAs FET IC high isolation absorptive single-pole 3-throw switch packaged in a 20-lead exposed-pad plastic package for low-cost commercial applications. This switch controls signals from 500 MHz to 2.5 GHz. The switch is ideal for cellular base station switch matrices and other applications that require good RF impedance match independent of switch state.

The SKY13277-355LF comprises a pHEMT switch die and a Si CMOS controller die. The switch die contains integral terminating resistors that present an absorptive load to the external circuit when the switch path is in its isolation state. The controller die has three inputs: supply voltage (V_{DD}) and two logic control bits that select the state of the pHEMT switch die. External DC block capacitors are required on all RF ports.

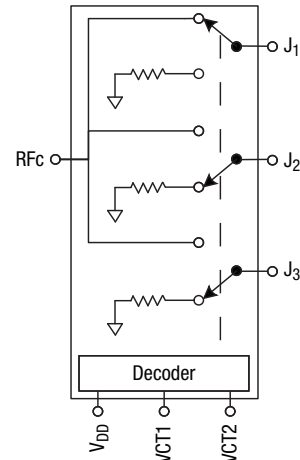
The SKY13277-355LF operates from -40 °C to 85 °C.

A populated evaluation board is available.

NEW Skyworks offers lead (Pb)-free, RoHS (Restriction of Hazardous Substances)-compliant packaging.



Functional Diagram



Electrical Specifications at 25 °C

V_{DD} = 5 V, V_{CTL} = 0/5 V, T = 25 C, P_{INPUT} = 0 dBm, Z₀ = 50 Ω, unless otherwise noted

Parameter	Frequency	Min.	Typ.	Max.	Unit
Insertion loss	0.5–1.0 GHz		0.9	1.1	dB
	1.0–2.0 GHz		1.1	1.3	dB
	2.0–2.5 GHz		1.3	1.5	dB
Isolation	0.5–1.0 GHz	60	62		dB
	1.0–2.0 GHz	53	57		dB
	2.0–2.5 GHz	49	55		dB
Return loss insertion loss state	0.5–1.0 GHz	11	15		dB
	1.0–2.0 GHz	9	12		dB
	2.0–2.5 GHz	8	11		dB
Return loss isolation state	0.5–1.0 GHz	11	15		dB
	1.0–2.0 GHz	10	14		dB
	2.0–2.5 GHz	8	13		dB

Operating Characteristics at 25 °C

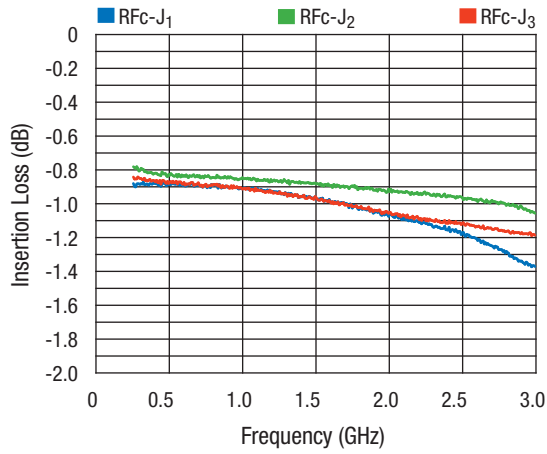
V_{DD} = 5 V, V_{CTL} = 0/5 V, T = 25 C, P_{INPUT} = 0 dBm, Z₀ = 50 Ω, unless otherwise noted

Parameter	Condition	Frequency	Min.	Typ.	Max.	Unit
Switching characteristics						
Rise/fall time	10/90% or 90/10% RF			5		ns
On/off time	50% V _{CTL} to 90/10% RF			15		ns
Input power for 1 dB compression	V _{DD} = 5 V	0.5–2.5 GHz		30		dBm
Intermodulation Intercept Point (IP3)	For two tone input power 13 dBm/tone 1 MHz spacing, V _{DD} = 5 V	0.5–2.5 GHz		43		dBm
Control voltages	V _{CTLLOW}		0		0.5	V
	V _{CTHIGH}		2.4		V _{DD}	V
Supply voltage (V _{DD})			2.75		5.5	V
Supply currents	V _{DD} = 3 V			5		uA
	V _{CTLLOW} , V _{CTHIGH}			5		uA

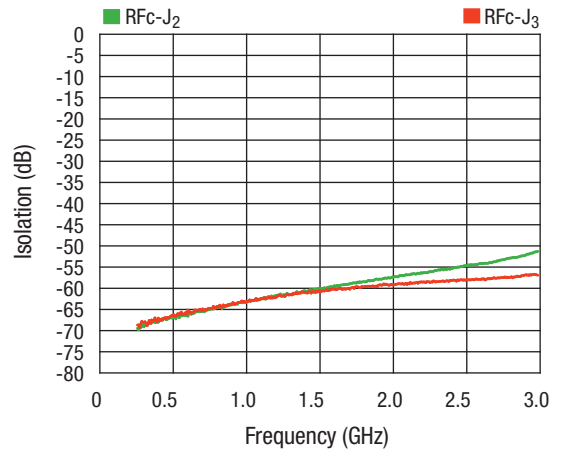
1. V_{DD} must be powered on prior to a V_{CTL} high signal. A latch up condition may occur if a logic high signal is applied prior to the V_{DD} voltage.
2. Control voltages switch the V_{DD} voltage to the GaAs switch.

Typical Performance Data

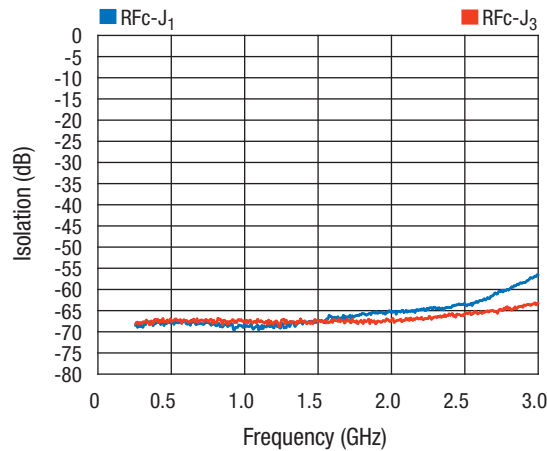
$V_{DD} = 5\text{ V}$, $V_{CTL} = 0/5\text{ V}$, $T = 25\text{ C}$, $P_{INPUT} = 0\text{ dBm}$, $C_{BLOCK} = 47\text{ pF}$, $Z_0 = 50\ \Omega$, unless otherwise noted



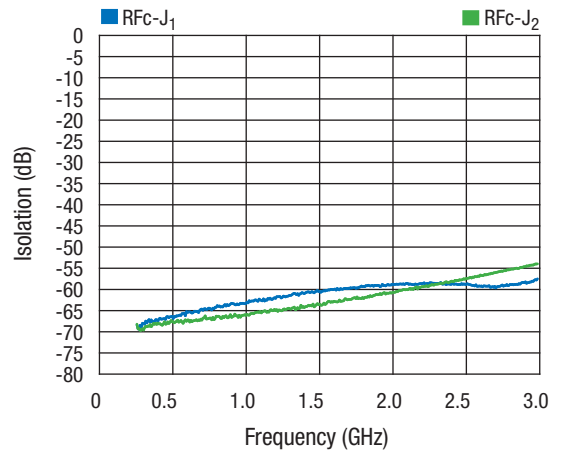
Typical Insertion Loss



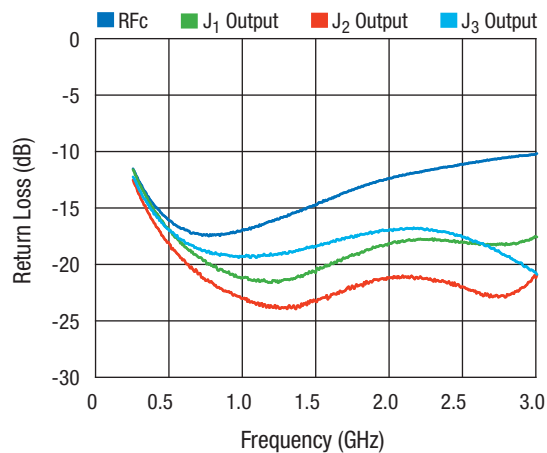
Typical Isolation RfC-J1 Ins. state



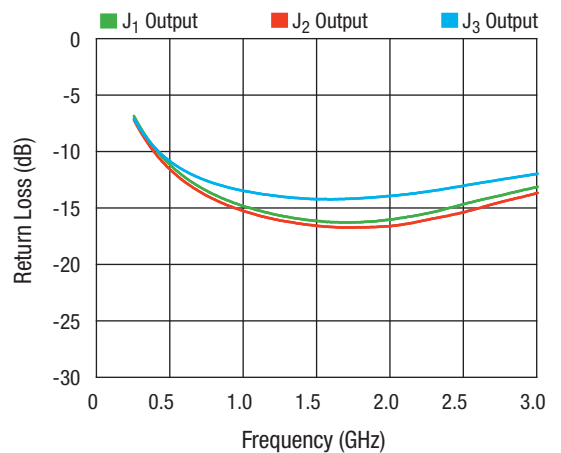
Typical Isolation RfC-J2 Ins. state



Typical Isolation RfC-J3 Ins. state



Typical Return Loss Ins. State



Typical Return Loss Isolation States

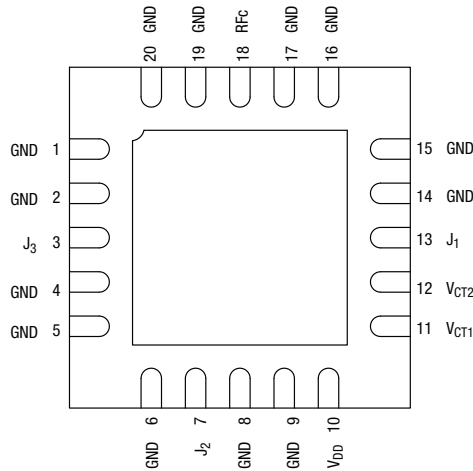
Absolute Maximum Ratings

Characteristic	Value
RF input power @ 5.5 V	32 dBm, f > 500 MHz
V _{DD} voltage range	2.75 ≤ V _{DD} ≤ 5.5 V
Operating temperature	-40 °C to +85 °C
Storage temperature	-65 °C to +150 °C

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum ratings. Exceeding any of the absolute maximum/minimum ratings may result in permanent damage to the device and will void the warranty.

CAUTION: Although this device is designed to be as robust as possible, ESD (Electrostatic Discharge) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

Pin Out (Top View)



DC blocks are required on RFC, J₁, J₂, J₃.

Truth Table

VCT1	VCT2	RFC to J ₁	RFC to J ₂	RFC to J ₃
0	0	Insertion loss	Isolation	Isolation
1	0	Isolation	Insertion loss	Isolation
0	1	Isolation	Isolation	Insertion loss
1	1	Undefined	Undefined	Undefined

"0" = 0 to 0.5 V.
 "1" = 2.4 to V_{DD}.
 V_{DD} = 2.75 to 5.5 V.

Recommended Solder Reflow Profiles

Refer to the ["Recommended Solder Reflow Profile"](#) Application Note.

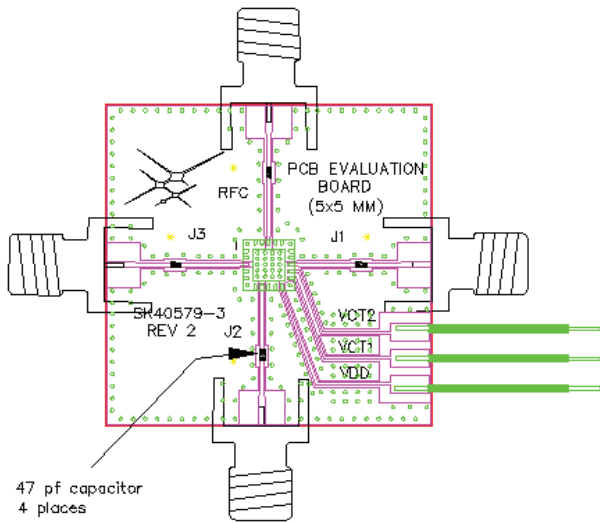
Tape and Reel Information

Refer to the ["Discrete Devices and IC Switch/Attenuators Tape and Reel Package Orientation"](#) Application Note.

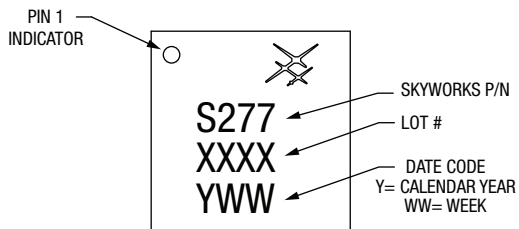
Pin Descriptions

Pin Number	Pin Name	Description
1, 2, 4, 5, 6, 8, 9, 14-17, 19, 20	Gnd	Ground
3	J ₃	RF port, must be DC blocked
7	J ₂	RF port, must be DC blocked
10	V _{DD}	DC bias for decoder
11	V _{CT1}	DC logic pin
12	V _{CT2}	DC logic pin
13	J ₁	RF port, must be DC blocked
18	RFC	RF common port, must be DC blocked
Exposed Paddle	Paddle	Ground

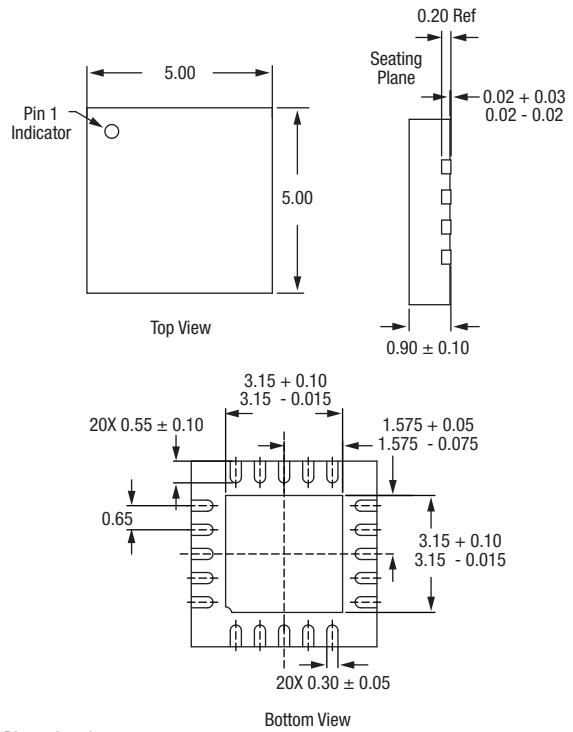
Evaluation Board



Part Marking



QFN-20 (5 x 5 mm)



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