

# NTD25P03L, STD25P03L

## MOSFET – Power, P-Channel, Logic Level, DPAK

**-25 A, -30 V**

Designed for low voltage, high speed switching applications and to withstand high energy in the avalanche and commutation modes. The source-to-drain diode recovery time is comparable to a discrete fast recovery diode.

### Features

- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### Typical Applications

- PWM Motor Controls
- Power Supplies
- Converters
- Bridge Circuits

### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	-30	V
Gate-to-Source Voltage – Continuous – Non-Repetitive (t <sub>p</sub> ≤ 10 ms)	V <sub>GS</sub> V <sub>GSM</sub>	±15 ±20	V V <sub>pk</sub>
Drain Current – Continuous @ T <sub>A</sub> = 25°C – Single Pulse (t <sub>p</sub> ≤ 10 μs)	I <sub>D</sub> I <sub>DM</sub>	-25 -75	A A <sub>pk</sub>
Total Power Dissipation @ T <sub>A</sub> = 25°C	P <sub>D</sub>	75	W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Single Pulse Drain-to-Source Avalanche Energy – Starting T <sub>J</sub> = 25°C (V <sub>DD</sub> = 25 Vdc, V <sub>GS</sub> = 5.0 Vdc, Peak I <sub>L</sub> = 20 Apk, L = 1.0 mH, R <sub>G</sub> = 25 Ω)	E <sub>AS</sub>	200	mJ
Thermal Resistance – Junction-to-Case – Junction-to-Ambient (Note 1) – Junction-to-Ambient (Note 2)	R <sub>θJC</sub> R <sub>θJA</sub> R <sub>θJA</sub>	1.65 67 120	°C/W
Maximum Lead Temperature for Soldering Purposes, (1/8 in from case for 10 seconds)	T <sub>L</sub>	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

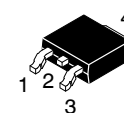
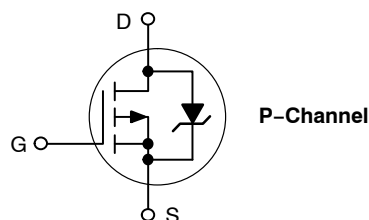
1. When surface mounted to an FR4 board using 0.5 sq in pad size.
2. When surface mounted to an FR4 board using the minimum recommended pad size.



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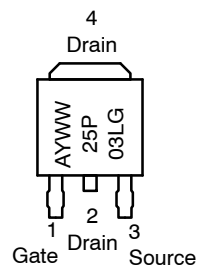
<http://onsemi.com>

V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> TYP	I <sub>D</sub> Max
-30 V	51 mΩ @ 5.0 V	-25 A



DPAK  
CASE 369C  
STYLE 2

### MARKING DIAGRAM & PIN ASSIGNMENT



- A = Assembly Location\*
- Y = Year
- WW = Work Week
- 25P03L = Device Code
- G = Pb-Free Package

\* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

# NTD25P03L, STD25P03L

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = -250 μA) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	-30	-24		V mV/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = -30 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 25°C) (V <sub>DS</sub> = -30 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	I <sub>DSS</sub>			-1.0 -100	μA
Gate-Body Leakage Current (V <sub>GS</sub> = ±15 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>			-100	nA

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μAdc) Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	-1.0	-1.6 4.0	-2.0	V mV/°C
Static Drain-to-Source On-State Resistance (V <sub>GS</sub> = -5.0 Vdc, I <sub>D</sub> = -12.5 Adc) (V <sub>GS</sub> = -5.0 Vdc, I <sub>D</sub> = -25 Adc) (V <sub>GS</sub> = -4.0 Vdc, I <sub>D</sub> = -10 Adc)	R <sub>DS(on)</sub>		0.051 0.056 0.065	0.072 0.080 0.090	Ω
Forward Transconductance (V <sub>DS</sub> = -8.0 Vdc, I <sub>D</sub> = -12.5 Adc)	g <sub>FS</sub>		13		Mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = -25 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>iss</sub>	900	1260	pF
Output Capacitance		C <sub>oss</sub>	290	410	
Reverse Transfer Capacitance		C <sub>rss</sub>	105	210	

### SWITCHING CHARACTERISTICS (Notes 3 & 4)

Turn-On Delay Time	(V <sub>DD</sub> = -15 Vdc, I <sub>D</sub> = -25 A, V <sub>GS</sub> = -5.0 V, R <sub>G</sub> = 1.3 Ω)	t <sub>d(on)</sub>	9.0	20	ns
Rise Time		t <sub>r</sub>	37	75	
Turn-Off Delay Time		t <sub>d(off)</sub>	15	30	
Fall Time		t <sub>f</sub>	16	55	
Gate Charge	(V <sub>DS</sub> = -24 Vdc, V <sub>GS</sub> = -5.0 Vdc, I <sub>D</sub> = -25 A)	Q <sub>T</sub>	15	20	nC
		Q <sub>1</sub>	3.0		
		Q <sub>2</sub>	9.0		
		Q <sub>3</sub>	7.0		

### BODY-DRAIN DIODE RATINGS (Note 3)

Diode Forward On-Voltage	(I <sub>S</sub> = -25 Adc, V <sub>GS</sub> = 0 V) (I <sub>S</sub> = -25 Adc, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125°C)	V <sub>SD</sub>	-1.0 -0.9	-1.5	V
Reverse Recovery Time	(I <sub>S</sub> = -25 A, V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs)	t <sub>rr</sub>	35		ns
		t <sub>a</sub>	20		
		t <sub>b</sub>	14		
Reverse Recovery Stored Charge		Q <sub>RR</sub>	0.035		μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperature.

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## TYPICAL MOSFET ELECTRICAL CHARACTERISTICS

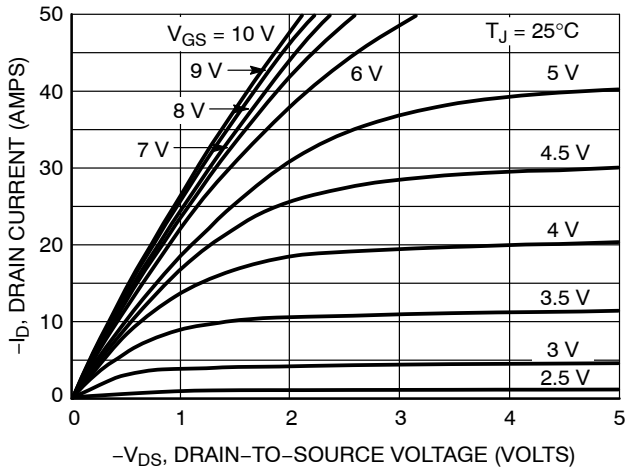


Figure 1. On-Region Characteristics

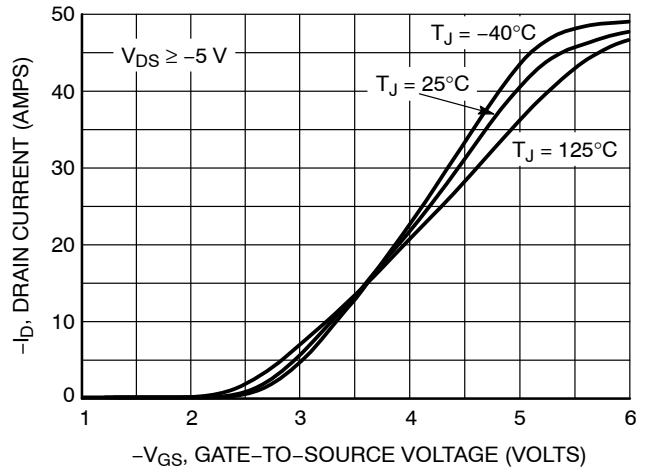


Figure 2. Transfer Characteristics

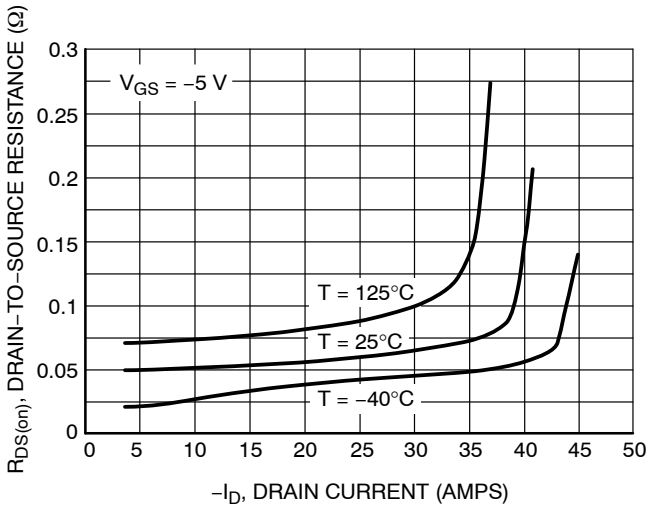


Figure 3. On-Resistance versus Drain Current and Temperature

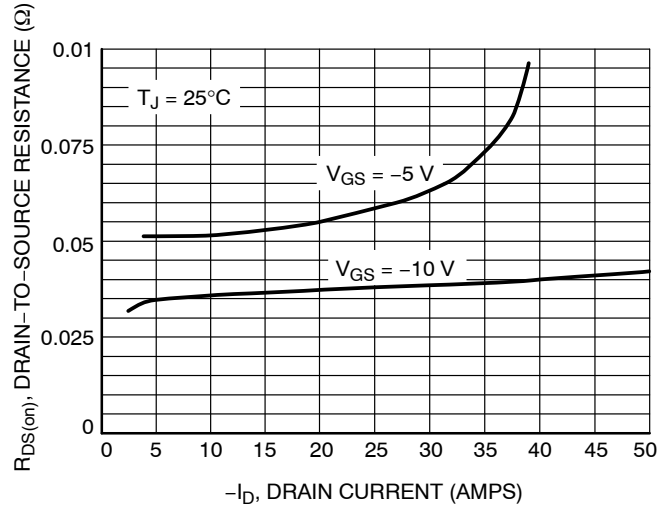


Figure 4. On-Resistance versus Drain Current and Gate Voltage

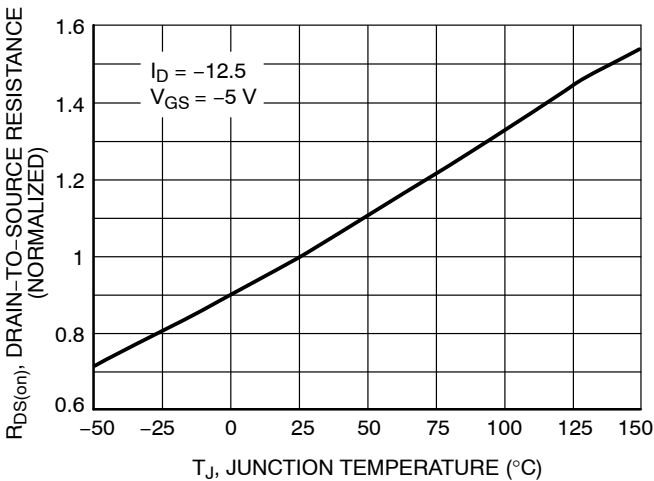


Figure 5. On-Resistance Variation with Temperature

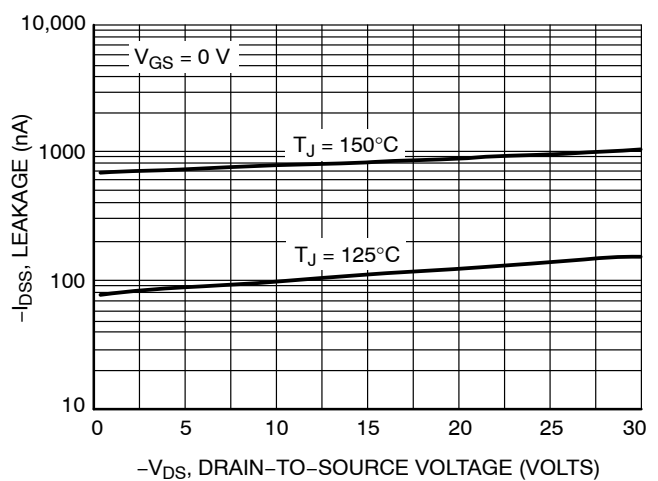


Figure 6. Drain-to-Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ( $\Delta t$ ) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain-gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ( $I_{G(AV)}$ ) can be made from a rudimentary analysis of the drive circuit so that

$$t = Q/I_{G(AV)}$$

During the rise and fall time interval when switching a resistive load,  $V_{GS}$  remains virtually constant at a level known as the plateau voltage,  $V_{GSP}$ . Therefore, rise and fall times may be approximated by the following:

$$t_r = Q_2 \times R_G / (V_{GG} - V_{GSP})$$

$$t_f = Q_2 \times R_G / V_{GSP}$$

where

$V_{GG}$  = the gate drive voltage, which varies from zero to  $V_{GG}$

$R_G$  = the gate drive resistance

and  $Q_2$  and  $V_{GSP}$  are read from the gate charge curve.

During the turn-on and turn-off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$$

$$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$$

The capacitance ( $C_{iss}$ ) is read from the capacitance curve at a voltage corresponding to the off-state condition when calculating  $t_{d(on)}$  and is read at a voltage corresponding to the on-state when calculating  $t_{d(off)}$ .

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by  $L di/dt$ , but since  $di/dt$  is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

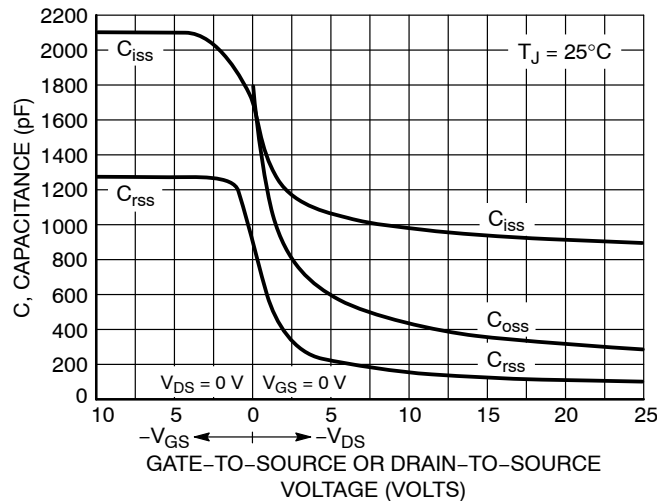
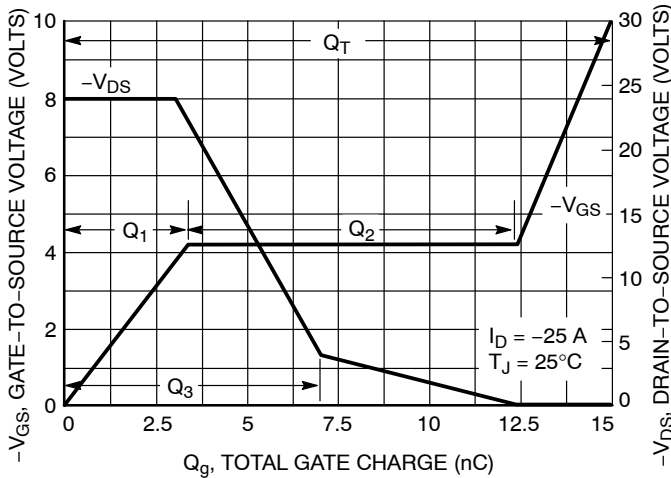
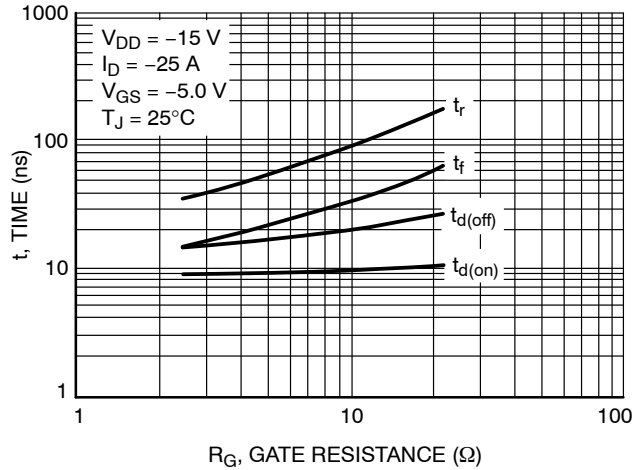


Figure 7. Capacitance Variation

## NTD25P03L, STD25P03L



**Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge**



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

### DRAIN-TO-SOURCE DIODE CHARACTERISTICS

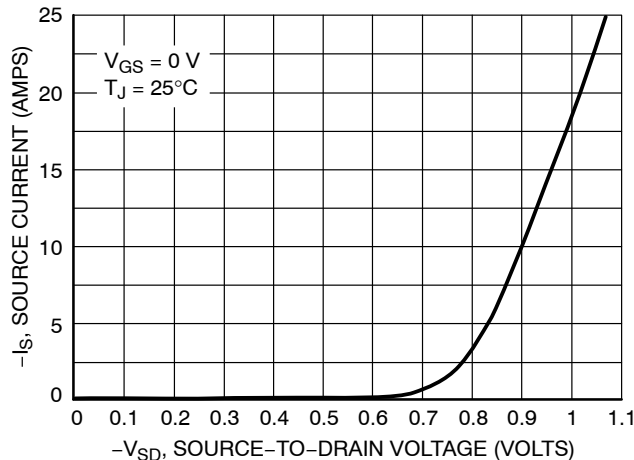
The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time,  $t_{rr}$ , due to the storage of minority carrier charge,  $Q_{RR}$ , as shown in the typical reverse recovery wave form of Figure 14. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short  $t_{rr}$  and low  $Q_{RR}$  specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by

high  $di/dt$ s. The diode's negative  $di/dt$  during  $t_a$  is directly controlled by the device clearing the stored charge. However, the positive  $di/dt$  during  $t_b$  is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of  $t_b/t_a$  serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter  $t_{rr}$ ), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher  $di/dt$  than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.



**Figure 10. Diode Forward Voltage versus Current**

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## SAFE OPERATING AREA

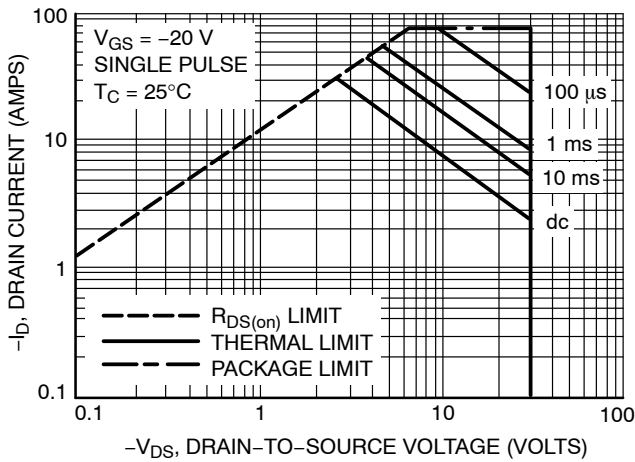
The Forward Biased Safe Operating Area curves define the maximum simultaneous drain-to-source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ( $T_C$ ) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off-state and the on-state may traverse any load line provided neither rated peak current ( $I_{DM}$ ) nor rated voltage ( $V_{DSS}$ ) is exceeded, and that the transition time ( $t_r$ ,  $t_f$ ) does not exceed 10  $\mu$ s. In addition the total power averaged over a complete switching cycle must not exceed  $(T_{J(MAX)} - T_C)/(R_{\theta JC})$ .

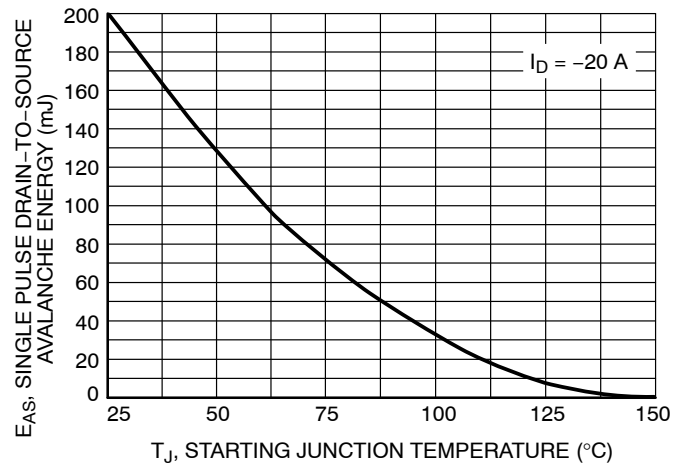
A power MOSFET designated E-FET can be safely used in switching circuits with unclamped inductive loads. For

reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non-linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E-FETs can withstand the stress of drain-to-source avalanche at currents up to rated pulsed current ( $I_{DM}$ ), the energy rating is specified at rated continuous current ( $I_D$ ), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous  $I_D$  can safely be assumed to equal the values indicated.



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

# NTD25P03L, STD25P03L

## TYPICAL ELECTRICAL CHARACTERISTICS

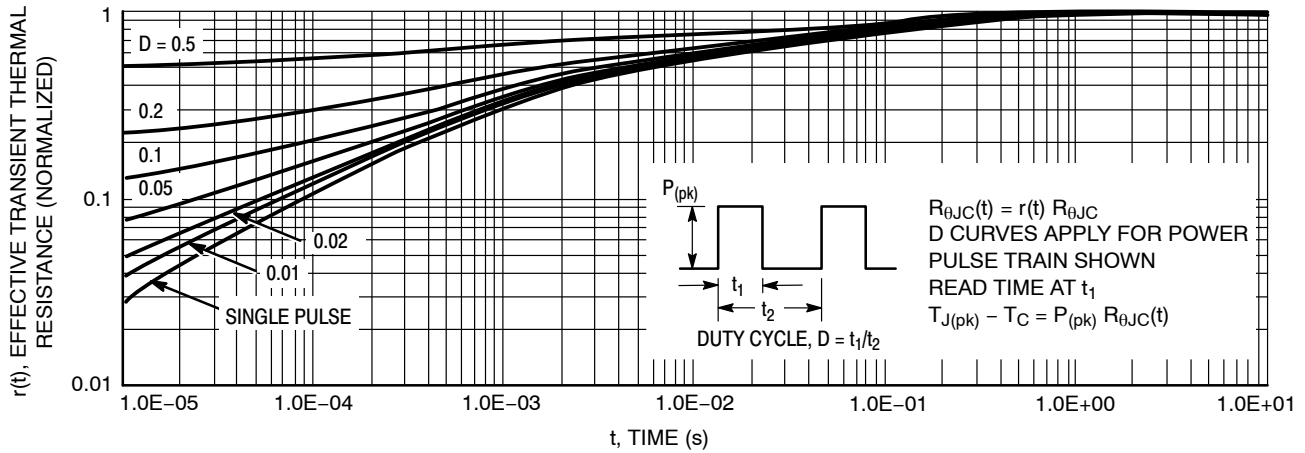


Figure 13. Thermal Response

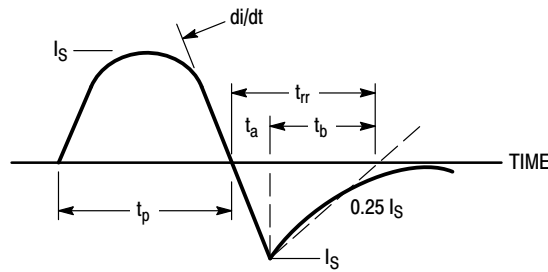


Figure 14. Diode Reverse Recovery Waveform

### ORDERING INFORMATION

Device	Package	Shipping†
NTD25P03LT4G	DPAK (Pb-Free)	2500 / Tape & Reel
STD25P03LT4G*	DPAK (Pb-Free)	2500 / Tape & Reel

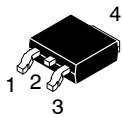
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



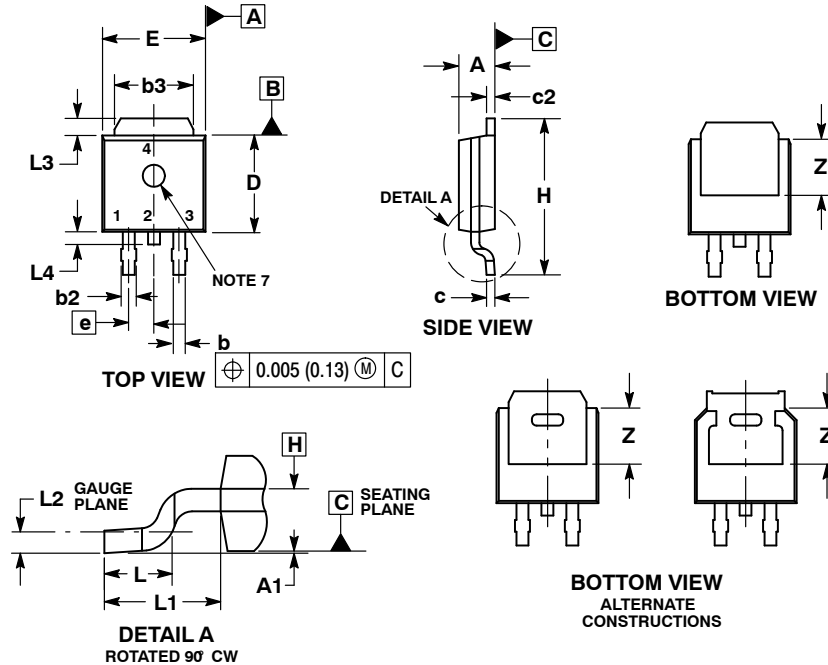
SCALE 1:1

### DPAK (SINGLE GAUGE)

#### CASE 369C

#### ISSUE F

DATE 21 JUL 2015

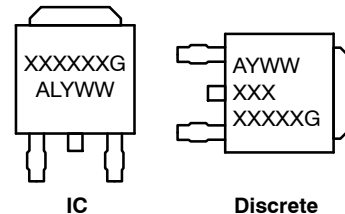


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

### GENERIC MARKING DIAGRAM\*

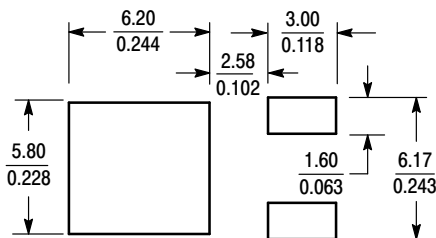


- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.

- |  |  |   |   |  |
|--|--|---|---|--|
| <p>STYLE 1:<br/>PIN 1. BASE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p>STYLE 2:<br/>PIN 1. GATE<br/>2. DRAIN<br/>3. SOURCE<br/>4. DRAIN</p>          | <p>STYLE 3:<br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p> | <p>STYLE 4:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. GATE<br/>4. ANODE</p>              | <p>STYLE 5:<br/>PIN 1. GATE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p>     |
| <p>STYLE 6:<br/>PIN 1. MT1<br/>2. MT2<br/>3. GATE<br/>4. MT2</p>                 | <p>STYLE 7:<br/>PIN 1. GATE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p>STYLE 8:<br/>PIN 1. N/C<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p>   | <p>STYLE 9:<br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. RESISTOR ADJUST<br/>4. CATHODE</p> | <p>STYLE 10:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p> |

### SOLDERING FOOTPRINT\*



SCALE 3:1 (mm / inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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<b>DESCRIPTION:</b>	<b>DPAK (SINGLE GAUGE)</b>	<b>PAGE 1 OF 1</b>

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