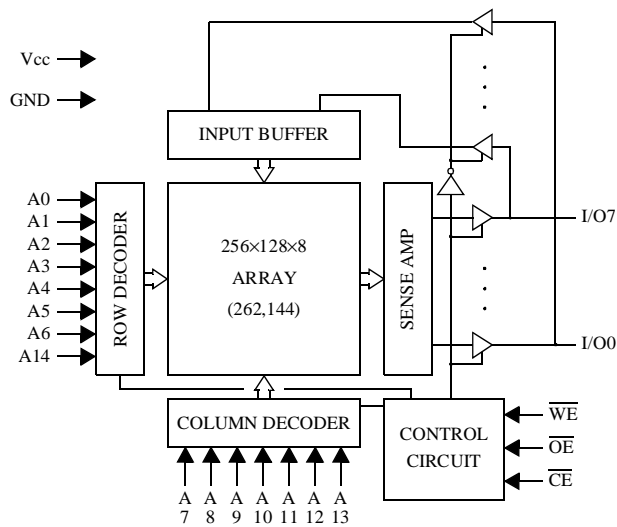


32K×8 CMOS SRAM (Common I/O)

**FEATURES**

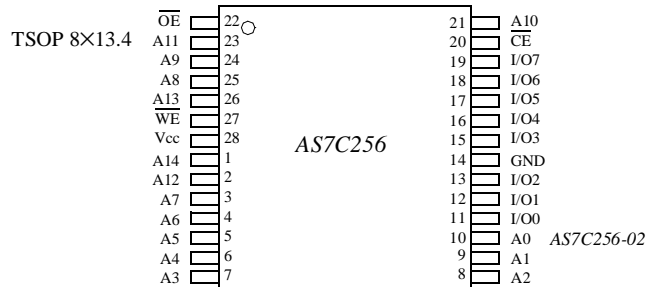
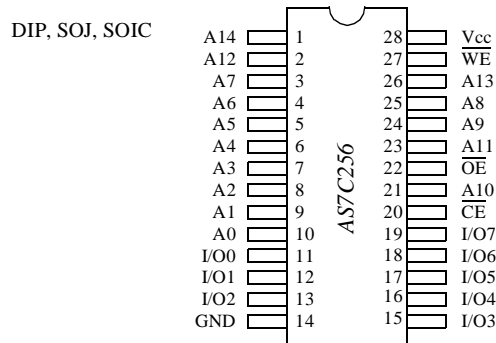
- Organization: 32,768 words × 8 bits
- High speed
  - 10/12/15/20/25/35 ns address access time
  - 3/3/4/5/6/8 ns output enable access time
- Low power consumption
  - Active: 660 mW max (10 ns cycle)
  - Standby: 11 mW max, CMOS I/O  
2.75 mW max, CMOS I/O, L version
  - Very low DC component in active power
- 2.0V data retention (L version)
- Equal access and cycle times
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  inputs
- TTL-compatible, three-state I/O
- 28-pin JEDEC standard packages
  - 300 mil PDIP and SOJ  
Socket compatible with 7C512 and 7C1024
  - 330 mil SOIC
  - 8×13.4 TSOP
- ESD protection > 2000 volts
- Latch-up current > 200 mA

**LOGIC BLOCK DIAGRAM**



AS7C256-01

**PIN ARRANGEMENT**



**SELECTION GUIDE**

	7C256-10	7C256-12	7C256-15	7C256-20	7C256-25	7C256-35	Unit
Maximum Address Access Time	10	12	15	20	25	35	ns
Maximum Output Enable Access Time	3	3	4	5	6	8	ns
Maximum Operating Current	120	115	110	100	90	80	mA
Maximum CMOS Standby Current	2.0	2.0	2.0	2.0	2.0	2.0	mA
	L	0.5	0.5	0.5	0.5	0.5	mA



## FUNCTIONAL DESCRIPTION

The AS7C256 is a high performance CMOS 262,144-bit Static Random Access Memory (SRAM) organized as 32,768 words  $\times$  8 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times ( $t_{AA}$ ,  $t_{RC}$ ,  $t_{WC}$ ) of 10/12/15/20/25/35 ns with output enable access times ( $t_{OE}$ ) of 3/3/4/5/6/8 ns are ideal for high performance applications. A chip enable ( $\overline{CE}$ ) input permits easy memory expansion with multiple-bank memory organizations.

When  $\overline{CE}$  is HIGH the device enters standby mode. The standard AS7C256 is guaranteed not to exceed 11 mW power consumption in standby mode; the L version is guaranteed not to exceed 2.75 mW, and typically requires only 500  $\mu$ W. The L version also offers 2.0V data retention, with maximum power consumption in this mode of 300  $\mu$ W.

A write cycle is accomplished by asserting chip enable ( $\overline{CE}$ ) and write enable ( $\overline{WE}$ ) LOW. Data on the input pins I/O0-I/O7 is written on the rising edge of  $\overline{WE}$  (write cycle 1) or  $\overline{CE}$  (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ( $\overline{OE}$ ) or write enable ( $\overline{WE}$ ).

A read cycle is accomplished by asserting chip enable ( $\overline{CE}$ ) and output enable ( $\overline{OE}$ ) LOW, with write enable ( $\overline{WE}$ ) HIGH. The chip drives I/O pins with the data word referenced by the input address. When chip enable or output enable is HIGH, or write enable is LOW, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible, and operation is from a single 5V supply. The AS7C256 is packaged in all high volume industry standard packages.

## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Voltage on Any Pin Relative to GND	$V_t$	-0.5	+7.0	V
Power Dissipation	$P_D$	-	1.0	W
Storage Temperature (Plastic)	$T_{stg}$	-55	+150	$^{\circ}$ C
Temperature Under Bias	$T_{bias}$	-10	+85	$^{\circ}$ C
DC Output Current	$I_{out}$	-	20	mA

**NOTE:** Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	High Z	Standby ( $I_{SB}$ , $I_{SB1}$ )
L	H	H	High Z	Output Disable
L	H	L	$D_{out}$	Read
L	L	X	$D_{in}$	Write

**Key:** X = Don't Care, L = LOW, H = HIGH



**RECOMMENDED OPERATING CONDITIONS**

( $T_a = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V
	GND	0.0	0.0	0.0	V
Input Voltage	$V_{IH}$	2.2	–	$V_{CC}+1$	V
	$V_{IL}$	-0.5*	–	0.8	V

\* $V_{IL}$  min = -3.0V for pulse width less than  $t_{RC}/2$ .

**DC OPERATING CHARACTERISTICS<sup>1</sup>**

( $V_{CC} = 5V \pm 10\%$ , GND = 0V,  $T_a = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Test Conditions	-10		-12		-15		-20		-25		-35		Unit	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Input Leakage Current	$I_{L L}$	$V_{CC} = \text{Max}$ , $V_{in} = \text{GND to } V_{CC}$	–	1	–	1	–	1	–	1	–	1	–	1	$\mu\text{A}$	
Output Leakage Current	$I_{L O}$	$\overline{CE} = V_{IH}$ , $V_{CC} = \text{Max}$ , $V_{out} = \text{GND to } V_{CC}$	–	1	–	1	–	1	–	1	–	1	–	1	$\mu\text{A}$	
Operating Power Supply Current	$I_{CC}$	$\overline{CE} = V_{IL}$ , $f = f_{max}$ , $I_{out} = 0 \text{ mA}$		–	120	–	115	–	110	–	100	–	90	–	80	mA
			L	–	115	–	110	–	105	–	95	–	85	–	75	mA
Standby Power Supply Current	$I_{SB}$	$\overline{CE} = V_{IH}$ , $f = f_{max}$		–	45	–	40	–	30	–	30	–	25	–	25	mA
			L	–	40	–	35	–	25	–	25	–	20	–	20	mA
	$I_{SB1}$	$\overline{CE} > V_{CC}-0.2V$ , $f = 0$ , $V_{in} \leq 0.2V$ or $V_{in} \geq V_{CC}-0.2V$		–	2.0	–	2.0	–	2.0	–	2.0	–	2.0	–	2.0	mA
Output Voltage	$V_{OL}$	$I_{OL} = 8 \text{ mA}$ , $V_{CC} = \text{Min}$	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	V	
	$V_{OH}$	$I_{OH} = -4 \text{ mA}$ , $V_{CC} = \text{Min}$	2.4	–	2.4	–	2.4	–	2.4	–	2.4	–	2.4	–	V	

**CAPACITANCE<sup>2</sup>**

( $f = 1 \text{ MHz}$ ,  $T_a = \text{Room Temperature}$ ,  $V_{CC} = 5V$ )

Parameter	Symbol	Signals	Test Conditions	Max	Unit
Input Capacitance	$C_{IN}$	A, $\overline{CE}$ , $\overline{WE}$ , $\overline{OE}$	$V_{in} = 0V$	5	pF
I/O Capacitance	$C_{I/O}$	I/O	$V_{in} = V_{out} = 0V$	7	pF



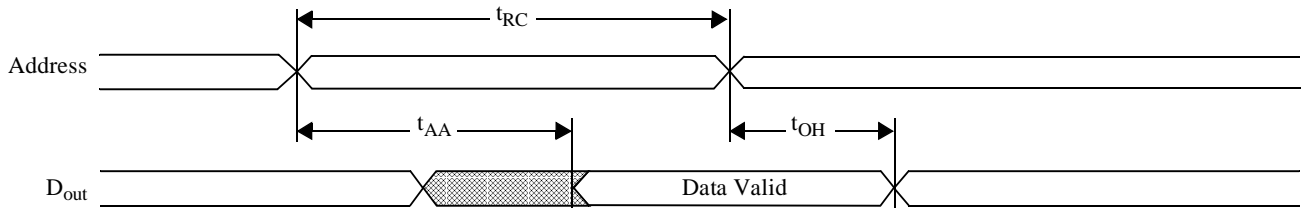
**READ CYCLE**<sup>3, 9</sup>

( $V_{CC} = 5V \pm 10\%$ ,  $GND = 0V$ ,  $T_a = 0^\circ C$  to  $+70^\circ C$ )

Parameter	Symbol	-10		-12		-15		-20		-25		-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	$t_{RC}$	10	-	12	-	15	-	20	-	25	-	35	-	ns	
Address Access Time	$t_{AA}$	-	10	-	12	-	15	-	20	-	25	-	35	ns	3
Chip Enable ( $\overline{CE}$ ) Access Time	$t_{ACE}$	-	10	-	12	-	15	-	20	-	25	-	35	ns	3
Output Enable ( $\overline{OE}$ ) Access Time	$t_{OE}$	-	3	-	3	-	4	-	5	-	6	-	8	ns	
Output Hold from Address Change	$t_{OH}$	2	-	3	-	3	-	3	-	3	-	3	-	ns	5
$\overline{CE}$ LOW to Output in Low Z	$t_{CLZ}$	3	-	3	-	3	-	3	-	3	-	3	-	ns	4, 5
$\overline{CE}$ HIGH to Output in High Z	$t_{CHZ}$	-	3	-	3	-	4	-	5	-	6	-	8	ns	4, 5
$\overline{OE}$ LOW to Output in Low Z	$t_{OLZ}$	0	-	0	-	0	-	0	-	0	-	0	-	ns	4, 5
$\overline{OE}$ HIGH to Output in High Z	$t_{OHZ}$	-	3	-	3	-	4	-	5	-	6	-	8	ns	4, 5
Power Up Time	$t_{PU}$	0	-	0	-	0	-	0	-	0	-	0	-	ns	4, 5
Power Down Time	$t_{PD}$	-	10	-	12	-	15	-	20	-	25	-	35	ns	4, 5

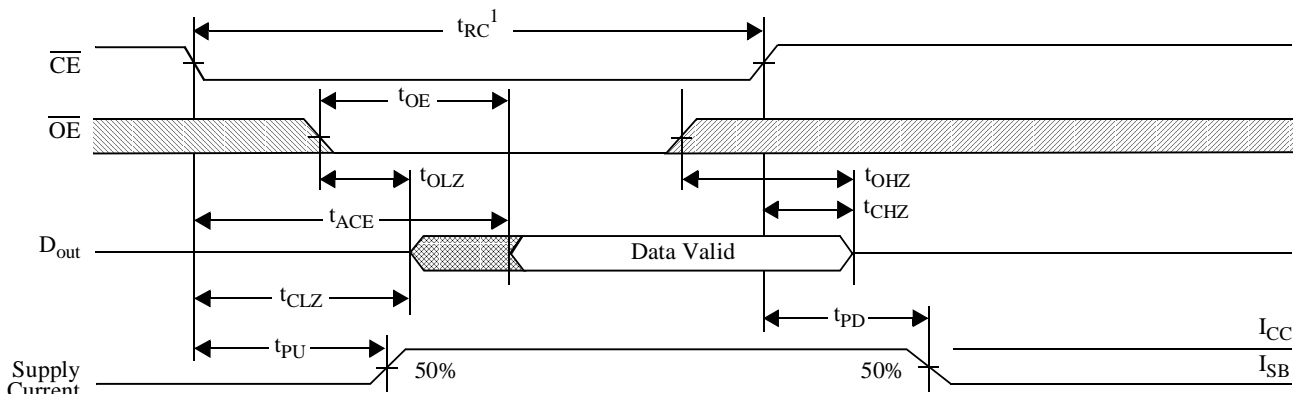
**TIMING WAVEFORM OF READ CYCLE 1**<sup>3, 6, 7, 9</sup>

(Address Controlled)



**TIMING WAVEFORM OF READ CYCLE 2**<sup>3, 6, 8, 9</sup>

( $\overline{CE}$  Controlled)



AS7C256-04



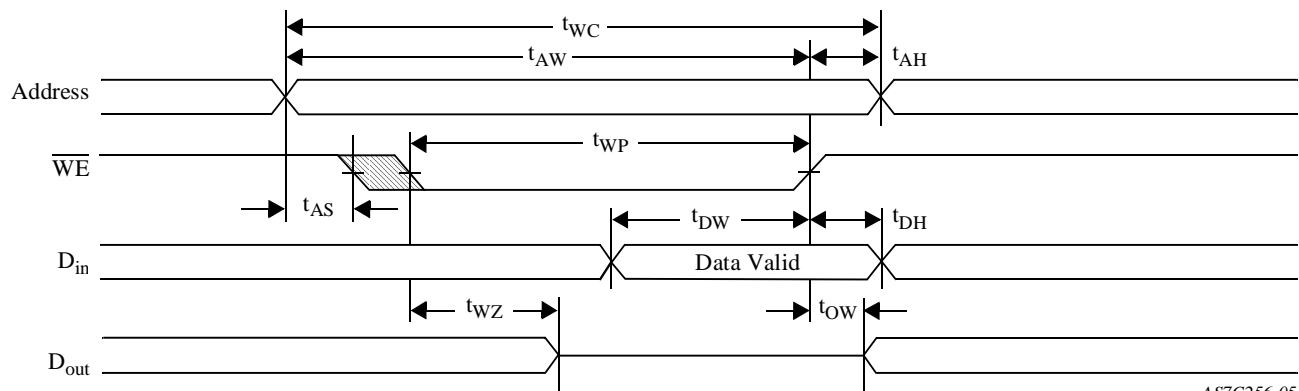
**WRITE CYCLE** <sup>11</sup>

( $V_{CC} = 5V \pm 10\%$ ,  $GND = 0V$ ,  $T_a = 0^\circ C$  to  $+70^\circ C$ )

Parameter	Symbol	-10		-12		-15		-20		-25		-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	$t_{WC}$	10	-	12	-	15	-	20	-	20	-	30	-	ns	
Chip Enable to Write End	$t_{CW}$	9	-	10	-	12	-	12	-	15	-	20	-	ns	
Address Setup to Write End	$t_{AW}$	9	-	10	-	12	-	12	-	15	-	20	-	ns	
Address Setup Time	$t_{AS}$	0	-	0	-	0	-	0	-	0	-	0	-	ns	
Write Pulse Width	$t_{WP}$	7	-	8	-	9	-	12	-	15	-	17	-	ns	
Address Hold From End of Write	$t_{AH}$	0	-	0	-	0	-	0	-	0	-	0	-	ns	
Data Valid to Write End	$t_{DW}$	6	-	6	-	8	-	10	-	10	-	15	-	ns	
Data Hold Time	$t_{DH}$	0	-	0	-	0	-	0	-	0	-	0	-	ns	4, 5
Write Enable to Output in High Z	$t_{WZ}$	-	5	-	5	-	5	-	5	-	5	-	5	ns	4, 5
Output Active from Write End	$t_{OW}$	3	-	3	-	3	-	3	-	3	-	3	-	ns	4, 5

**TIMING WAVEFORM OF WRITE CYCLE 1** <sup>10, 11</sup>

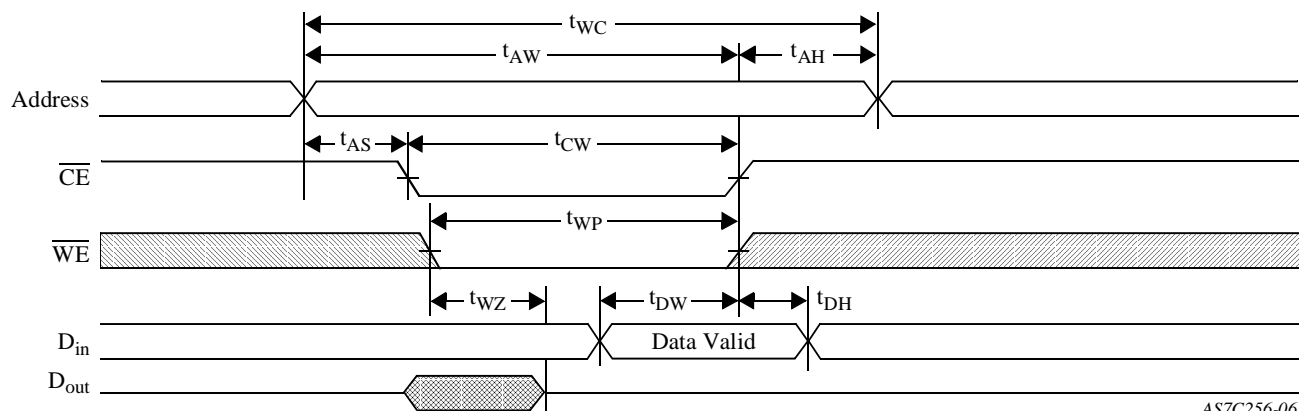
( $\overline{WE}$  Controlled)



AS7C256-05

**TIMING WAVEFORM OF WRITE CYCLE 2** <sup>10, 11</sup>

( $\overline{CE}$  Controlled)



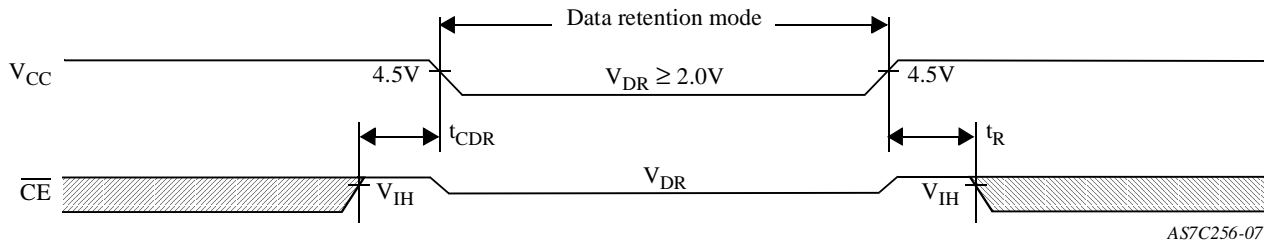
AS7C256-06



**DATA RETENTION CHARACTERISTICS** (L Version Only)

Parameter	Symbol	Test Conditions	Min	Max	Unit
V <sub>CC</sub> for Data Retention	V <sub>DR</sub>	V <sub>CC</sub> = 2.0V	2.0	–	V
Data Retention Current	I <sub>CCDR</sub>	$\overline{CE} \geq V_{CC} - 0.2V$	–	150	μA
Chip Enable to Data Retention Time	t <sub>CDR</sub>	V <sub>in</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>in</sub> ≤ 0.2V	0	–	ns
Operation Recovery Time	t <sub>R</sub>		t <sub>RC</sub>	–	ns
Input Leakage Current	I <sub>LI</sub>		–	1	μA

**DATA RETENTION WAVEFORM** (L Version Only)



**AC TEST CONDITIONS**

- Output load: see Figure B, except for t<sub>CLZ</sub> and t<sub>CHZ</sub> see Figure C.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 5 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

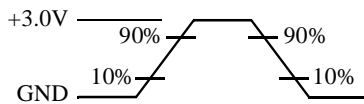


Figure A: Input Waveform  
AS7C256-08

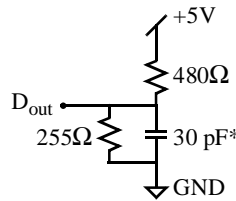


Figure B: Output Load  
AS7C256-09

Thevenin Equivalent:  
D<sub>out</sub> ← 168Ω → +1.728V

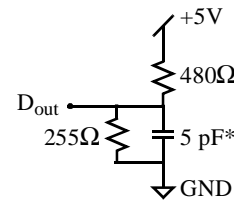


Figure C: Output Load for t<sub>CLZ</sub>, t<sub>CHZ</sub>  
AS7C256-10

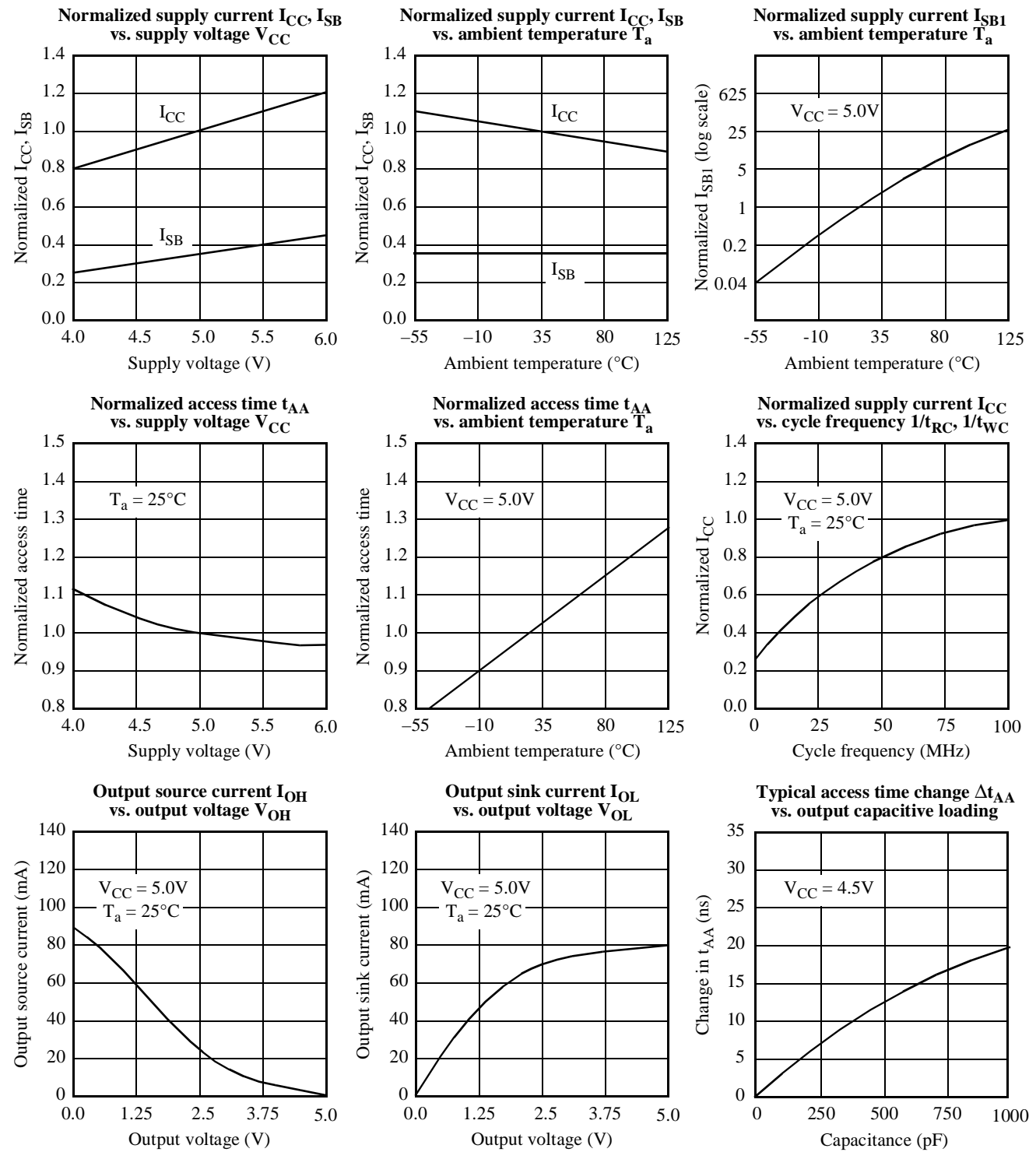
\*including scope and jig capacitance

**NOTES**

1. During V<sub>CC</sub> power-up, a pull-up resistor to V<sub>CC</sub> on  $\overline{CE}$  is required to meet I<sub>SB</sub> specification.
2. This parameter is sampled and not 100% tested.
3. For test conditions, see AC Test Conditions, Figures A, B, C.
4. t<sub>CLZ</sub> and t<sub>CHZ</sub> are specified with CL = 5pF as in Figure C. Transition is measured ±500mV from steady-state voltage.
5. This parameter is guaranteed but not tested.
6.  $\overline{WE}$  is HIGH for read cycle.
7.  $\overline{CE}$  and  $\overline{OE}$  are LOW for read cycle.
8. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
9. All read cycle timings are referenced from the last valid address to the first transitioning address.
10.  $\overline{CE}$  or  $\overline{WE}$  must be HIGH during address transitions.
11. All write cycle timings are referenced from the last valid address to the first transitioning address.



**TYPICAL DC AND AC CHARACTERISTICS**





**ORDERING CODES**

Package / Access Time	10 ns	12 ns	15 ns	20 ns	25 ns	35 ns
Plastic DIP, 300 mil	AS7C256-10PC AS7C256L-10PC	AS7C256-12PC AS7C256L-12PC	AS7C256-15PC AS7C256L-15PC	AS7C256-20PC AS7C256L-20PC	AS7C256-25PC AS7C256L-25PC	AS7C256-35PC AS7C256L-35PC
Plastic SOJ, 300 mil	AS7C256-10JC AS7C256L-10JC	AS7C256-12JC AS7C256L-12JC	AS7C256-15JC AS7C256L-15JC	AS7C256-20JC AS7C256L-20JC	AS7C256-25JC AS7C256L-25JC	AS7C256-35JC AS7C256L-35JC
Plastic SOIC, 330 mil	AS7C256-10SC AS7C256L-10SC	AS7C256-12SC AS7C256L-12SC	AS7C256-15SC AS7C256L-15SC	AS7C256-20SC AS7C256L-20SC	AS7C256-25SC AS7C256L-25SC	AS7C256-35SC AS7C256L-35SC
TSOP 8x13.4	AS7C256-10TC AS7C256L-10TC	AS7C256-12TC AS7C256L-12TC	AS7C256-15TC AS7C256L-15TC	AS7C256-20TC AS7C256L-20TC	AS7C256-25TC AS7C256L-25TC	AS7C256-35TC AS7C256L-35TC

**PART NUMBERING SYSTEM**

AS7C	256	X	-XX	X	C	
SRAM Prefix	Device Number	Blank L	= Standard Power = Low Power	Access Time	Package: P = PDIP 300 mil J = SOJ 300 mil S = SOIC 330 mil T = TSOP 8x14	Commercial Temperature Range, 0°C to 70 °C

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