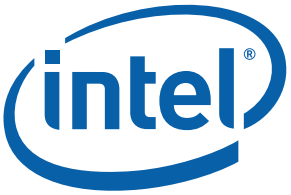

Intel® 8 Series / C220 Series Chipset Family Platform Controller Hub (PCH)

Specification Update

July 2018

Revision 005

Notice: The Intel® 8 Series / C220 Series Chipset Family Platform Controller Hub (PCH) may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Order Number: 328905-005

Contents

Revision History

Revision	Description	Date
001	• Initial Release	June 2013
002	• Errata — Added errata 23-26	January 2014
003	• Errata — Added erratum 27 • Added C2 Stepping • Updated Identification Information, Markings Table.	May 2014
004	• Errata — Added errata 28-29	October 2014
005	• Errata — Added errata 30-31 — Updated erratum 28	July 2018

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Preface

This document is an update to the specifications contained in the Affected Documents/ Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents / Related Documents

Title	Document Number
Intel® 8 Series / C220 Series Chipset Family Platform Controller Hub (PCH) Datasheet	328904

Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the PCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Summary of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes that apply to the product. Intel may fix some of the errata in a future stepping of the component and account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations.

Codes Used in Summary Tables

Stepping

X:	Erratum exists in the stepping indicated. Specification Change that applies to the stepping indicated.
(No mark) or (Blank box):	This erratum is fixed or not applicable in listed stepping or Specification Change does not apply to listed stepping.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Erratum Number	Stepping		Status	ERRATA
	C1	C2		
1	X	X	No Fix	USB Isoch In Transfer Error Issue
2	X	X	No Fix	USB Babble Detected with SW Overscheduling
3	X	X	No Fix	USB Full-/low-speed EOP Issue
4	X	X	No Fix	Asynchronous Retries Prioritized Over Periodic Transfers
5	X	X	No Fix	USB FS/LS Incorrect Number of Retries
6	X	X	No Fix	USB Full-/Low-speed Port Reset or Clear TT Buffer Request
7	X	X	No Fix	xHC Data Packet Header and Payload Mismatch Error Condition
8	X	X	No Fix	USB SuperSpeed Packet with Invalid Type Field Issue
9	X	X	No Fix	xHC Behavior with Three Consecutive Failed U3 Entry Attempts
10	X	X	No Fix	Incorrect IRQ(x) Vector Returned for 8259 Interrupts With RAEOI Enabled
11	X	X	No Fix	USB RMH Think Time Issue
12	X	X	No Fix	Max Packet Size and Transfer Descriptor Length Mismatch
13	X	X	No Fix	USB Full-/low-speed Device Removal Issue
14	X	X	No Fix	PCIe Root Ports Unsupported Request Completion
15	X	X	No Fix	SATA Signal Voltage Level Violation
16	X	X	No Fix	LPT CRT DAC VESA INL Spec Violation
17	X		Fixed	SuperSpeed Device Re-Enumeration
18	X	X	No Fix	Display Port Aux Clock Jitter Issues
19	X	X	No Fix	Set Latency Tolerance Value Command Completion Event Issue
20	X	X	No Fix	LFPS Detect Threshold
21	X	X	No Fix	SMBus Hold Time
22	X	X	No Fix	RMH Port Disabled Due to Device Initiated Remote Wake
23	X	X	No Fix	Enumeration Issue when Resuming for Sx
24	X	X	No Fix	SATA Lock Lost with During Link Negotiation
25	X	X	No Fix	PCIe* Clocking Mode Switch Issue
26	X	X	No Fix	USB xHCI may Execute a Stale Transfer Request Block (TRB)
27	X	X	No Fix	Clearing xHCI PME_EN May Not Disable USB 2.0 Wake Events
28	X	X	No Fix	xHCI Controller May Delayed Transactions Due to Short Packets Issue
29	X	X	No Fix	xHCI Controller D3 Entry Issue – External
30	X	X	No Fix	xHCI USB2.0 Split-Transactions Error Counter Reset Issue
31	X	X	No Fix	Unexpected USB 2.0 HS Controller Signal Amplitude.

Specification Changes

Spec Change Number	Stepping		SPECIFICATION CHANGES
	C1	C2	
			There are no specification Changes in this revision of the specification update.

Specification Clarifications

Spec Clarification Number	SPECIFICATION CHANGES
1	Intel® Ethernet Network Connection 1127

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Identification Information

Markings

PCH Stepping	Top Marking (S-Spec)	Notes
C1	SR137	Desktop Intel® Series Chipset Q87
C1	SR138	Desktop Intel® Series Chipset Q85
C1	SR139	Desktop Intel® Series Chipset H87
C1	SR13A	Desktop Intel® Series Chipset Z87
C1	SR13C	Desktop Intel® Series Chipset B85
C1	SR13B	Desktop Intel® Series Chipset H81
C1	SR13D	Server/Workstation Intel® Series Chipset C226
C1	SR13E	Server Intel® Series Chipset C224
C1	SR13F	Server Intel® Series Chipset C222
C1	SR13G	Mobile Intel® Series Chipset QM87
C1	SR13H	Mobile Intel® Series Chipset HM87
C1	SR13J	Mobile Intel® Series Chipset HM86
C2	SR173	Desktop Intel® Series Chipset HQ87
C2	SR174	Desktop Intel® Series Chipset Q85
C2	SR175	Desktop Intel® Series Chipset H87
C2	SR176	Desktop Intel® Series Chipset Z87
C2	SR177	Desktop Intel® Series Chipset H81
C2	SR178	Desktop Intel® Series Chipset B85
C2	SR17C	Mobile Intel® Series Chipset QM87
C2	SR17D	Mobile Intel® Series Chipset HM87
C2	SR17E	Mobile Intel® Series Chipset HM86
C2	SR17A	Server Intel® Series Chipset C224
C2	SR17B	Server Intel® Series Chipset C222
C2	SR179	Server/Workstation Intel® Series Chipset C226

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Errata

1. USB Isoch In Transfer Error Issue

Problem: If a USB full-speed inbound isochronous transaction with a packet length 190 bytes or greater is started near the end of a microframe the PCH may see more than 189 bytes in the next microframe.

Implication: If the PCH sees more than 189 bytes for a microframe an error will be sent to software and the isochronous transfer will be lost. If a single data packet is lost no perceptible impact for the end user is expected.

Note: Intel has only observed the issue in a synthetic test environment where precise control of packet scheduling is available, and has not observed this failure in its compatibility validation testing.

- Isochronous traffic is periodic and cannot be retried thus it is considered good practice for software to schedule isochronous transactions to start at the beginning of a microframe. Known software solutions follow this practice.
- To sensitize the system to the issue additional traffic such as other isochronous transactions or retries of asynchronous transactions would be required to push the inbound isochronous transaction to the end of the microframe.

Workaround: None.

Status: No Plan to Fix

2. USB Babble Detected with SW Overscheduling

Problem: If software violates USB periodic scheduling rules for full-speed isochronous traffic by overscheduling, the RMH may not handle the error condition properly and return a completion split with more data than the length expected.

Implication: If the RMH returns more data than expected, the endpoint will detect packet babble for that transaction and the packet will be dropped. Since overscheduling occurred to create the error condition, the packet would be dropped regardless of RMH behavior. If a single isochronous data packet is lost, no perceptible impact to the end user is expected.

Note: USB software overscheduling occurs when the amount of data scheduled for a microframe exceeds the maximum budget. This is an error condition that violates the USB periodic scheduling rule.

Note: This failure has only been recreated synthetically with USB software intentionally overscheduling traffic to hit the error condition.

Workaround: None.

Status: No Plan to Fix

3. USB Full-/low-speed EOP Issue

Problem: If the EOP of the last packet in a USB Isochronous split transaction (Transaction >189 bytes) is dropped or delayed 3 ms or longer the following may occur:

- If there are no other pending low-speed or full-speed transactions the RMH will not send SOF, or Keep-Alive. Devices connected to the RMH will interpret this condition as idle and will enter suspend.
- If there is other pending low-speed or full-speed transactions, the RMH will drop the isochronous transaction and resume normal operation.

Implication:

- If there are no other transactions pending, the RMH is unaware a device entered suspend and may starting sending a transaction without waking the device. The implication is device dependent, but a device may stall and require a reset to resume functionality.
- If there are other transactions present, only the initial isochronous transaction may be lost. The loss of a single isochronous transaction may not result in end user perceptible impact.

Note: Intel has only observed this failure when using software that does not comply with the USB specification and violates the hardware isochronous scheduling threshold by terminating transactions that are already in progress

Workaround: None.

Status: No Plan to Fix

4. Asynchronous Retries Prioritized Over Periodic Transfers

Problem: The integrated USB RMH incorrectly prioritizes full-speed and low-speed asynchronous retries over dispatchable periodic transfers.

Implication: Periodic transfers may be delayed or aborted. If the asynchronous retry latency causes the periodic transfer to be aborted, the impact varies depending on the nature of periodic transfer:

- If a periodic interrupt transfer is aborted, the data may be recovered by the next instance of the interrupt or the data could be dropped.
- If a periodic isochronous transfer is aborted, the data will be dropped. A single dropped periodic transaction should not be noticeable by end user.

Note: This issue has only been seen in a synthetic environment. The USB spec does not consider the occasional loss of periodic traffic a violation.

Workaround: None.

Status: No Plan to Fix

5. USB FS/LS Incorrect Number of Retries

Problem: A USB low-speed transaction may be retried more than three times, and a USB full-speed transaction may be retried less than three times if all of the following conditions are met:

- A USB low-speed transaction with errors, or the first retry of the transaction occurs near the end of a microframe, and there is not enough time to complete another retry of the low-speed transaction in the same microframe.
- There is pending USB full-speed traffic and there is enough time left in the microframe to complete one or more attempts of the full-speed transaction.
- Both the low-speed and full-speed transactions must be asynchronous (Bulk/Control) and must have the same direction either in or out.

Note: Per the USB EHCI Specification a transaction with errors should be attempted a maximum of 3 times if it continues to fail.

Implication:

- For low-speed transactions the extra retry(s) allow a transaction additional chance(s) to recover regardless of if the full-speed transaction has errors or not.
- If the full-speed transactions also have errors, the PCH may retry the transaction fewer times than required, stalling the device prematurely. Once stalled, the implication is software dependent, but the device may be reset by software.

Workaround: None

Status: No Plan to Fix

6. USB Full-/Low-speed Port Reset or Clear TT Buffer Request

Problem: One or more full-/low-speed USB devices on the same RMH controller may be affected if the devices are not suspended and either (a) software issues a Port Reset OR (b) software issues a Clear TT Buffer request to a port executing a split full-/low-speed Asynchronous Out command.

- The small window of exposure for full-speed device is around 1.5 microseconds and around 12 microseconds for a low-speed device.

Implication: The affected port may stall or receive stale data for a newly arrived split transfer occurring at the time of the Port Reset or Clear TT Buffer request.

Note: This issue has only been observed in a synthetic test environment.

Workaround: None.

Status: No Plan to Fix

7. xHC Data Packet Header and Payload Mismatch Error Condition

Problem: If a SuperSpeed device sends a DPH (Data Packet Header) to the xHC with a data length field that specifies less data than is actually sent in the DPP (Data Packet Payload), the xHC will accept the packet instead of discarding the packet as invalid.

Note: The USB 3.0 specification requires a device to send a DPP matching the amount of data specified by the DPH.

Implication: The amount of data specified in the DPH will be accepted by the xHC and the remaining data will be discarded and may result in anomalous system behavior.

Note: This issue has only been observed in a synthetic test environment with a synthetic device.

Workaround: None.

Status: No Plan to Fix

8. USB SuperSpeed Packet with Invalid Type Field Issue

Problem: If the encoding for the “type” field for a SuperSpeed packet is set to a reserved value and the encoding for the “subtype” field is set to “ACK”, the xHC may accept the packet as a valid acknowledgement transaction packet instead of ignoring the packet.

Note: The USB 3.0 specification requires that a device never set any defined fields to reserved values.

Implication: System implication is dependent on the misbehaving device and may result in anomalous system behavior.

Note: This issue has only been observed in a synthetic test environment with a synthetic device.

Workaround: None.

Status: No Plan to Fix

9. xHC Behavior with Three Consecutive Failed U3 Entry Attempts

Problem: The xHC does not transition to the SS.Inactive USB 3.0 LTSSM (Link Training and Status State Machine) state after a SuperSpeed device fails to enter U3 upon three consecutive attempts.

Note: The USB 3.0 specification requires a SuperSpeed device to enter U3 when directed.

Implication: The xHC will continue to try to initiate U3. The implication is driver and operating system dependent.

Workaround: None.

Status: No Plan to Fix

10. Incorrect IRQ(x) Vector Returned for 8259 Interrupts With RAEOI Enabled

Problem: If multiple interrupts are active prior to an interrupt acknowledge cycle with Rotating Automatic End of Interrupt (RAEOI) mode of operation enabled for 8259 interrupts (0-7), an incorrect IRQ(x) vector may be returned to the processor.

Implication: Implications of an incorrect IRQ(x) vector being returned to the CPU are SW implementation dependent.

Note: This issue has only been observed in a synthetic test environment.

Workaround: None.

Status: No Plan to Fix

11. USB RMH Think Time Issue

Problem: The USB RMH Think Time may exceed its declared value in the RMH hub descriptor register of 8 full-speed bit times.

Implication: If the USB driver fully subscribes a USB microframe, LS/FS transactions may exceed the microframe boundary.

Note: No functional failures have been observed.

Workaround: None.

Status: No Plan to Fix

12. Max Packet Size and Transfer Descriptor Length Mismatch

Problem: The xHC may incorrectly handle a request from a low-speed or full-speed device when all the following conditions are true:

- The sum of the packet fragments equals the length specified by the TD (Transfer Descriptor)
- The TD length is less than the MPS (Max Packet Size) for the device
- The last packet received in the transfer is “0” or babble bytes

Implication: The xHC will halt the endpoint if all the above conditions are met. All functions associated with the endpoint will stop functioning until the device is unplugged and reinserted.

Workaround: None.

Status: No Plan to Fix

13. USB Full-/low-speed Device Removal Issue

Problem: If two or more USB full-/low-speed devices are connected to the same USB controller, the devices are not suspended, and one device is removed, one or more of the devices remaining in the system may be affected by the disconnect.

Implication: The implication is device dependent. A device may experience a delayed transaction, stall and be recovered via software, or stall and require a reset such as a hot plug to resume normal functionality.

Workaround: None.

Status: No Plan to Fix

14. PCIe Root Ports Unsupported Request Completion

Problem: The PCIe* root ports may return an Unsupported Request (UR) completion with an incorrect lower address field in response to a memory read if any of the following occur:

- Bus Master Enable is disabled in the PCIe Root Port’s Command register (PCICMD bit 2 =0)
- Address Type (AT) field of the Transaction Layer Packet (TLP) header is non-zero
- The requested upstream address falls within the memory range claimed by the secondary side of the bridge
- Requester ID with Bus Number of 0

Implication: The UR Completion with an incorrect lower address field may be handled as a Malformed TLP causing the Requestor to send an ERR_NONFATAL or ERR_FATAL message upstream to the root port.

Workaround: None.

Status: No Plan to Fix

15. SATA Signal Voltage Level Violation

Problem: SATA transmit buffers have been designed to maximize performance and robustness over a variety of rouuting scenarios. As a result, the SATA transmit signaling voltage levels may exceed the maximum motherboard TX connector and device RX connector voltage specifications as defined in section 7.2.2.3 of the Serial ATA specification, rev 3.1. This issue applies to Gen 1 (1.5 Gb/s).

Implication: None known.

Workaround: None.

Status: No Plan to Fix

16. LPT CRT DAC VESA INL Spec Violation

Problem: A limited number of parts operating close to Vmin on VCCADAC1_5 or at low temperature may exceed the Integral Linearity Error (INL) limit of +/- 1 Least Significant Bit (LSB) defined by the Video Electronics Standards Association (VESA) for display digital-to-analog converters (DACs).

Implication: A slight brightness or color degradation may occur at the brightest or most color saturated area of the display and may not be noticeable to the end user.

Workaround: None.

Status: No Plan to Fix

17. SuperSpeed Device Re-Enumeration

Problem: If a SuperSpeed device is connected to the xHC and an unexpected device pulse occurs on the USB3R{n,p} signals during an exit from U3 low power link state, the xHC may falsely detect a connection event.

Implication: The SuperSpeed device may re-enumerate when resuming from U3. Implications of reenumeration are driver, application and operating system dependent.
Note: A SuperSpeed device may enter the U3 low power link state during S3 or selective suspend. There are no known cases of data loss since the SuperSpeed device always re-enumerates.

Workaround: None.

Status: For the steppings affected, see the Summary of Changes.

18. Display Port Aux Clock Jitter Issues

Problem: The DisplayPort Aux Channel Clock may exceed the maximum allowed jitter.

There are no known functional failures due to this issue.

Workaround: None.

Status: No Plan to Fix

19. Set Latency Tolerance Value Command Completion Event Issue

Problem: The xHCI controller does not return a value of ‘0’ for slot ID in the command completion event TRB (Transfer Request Block) for a set latency tolerance value command.

Note: This violates the command completion event TRB description in section 6.4.2.2 of the eXtensible Host Controller Interface for Universal Serial Bus (xHCI) specification, revision 1.0.

Implication: There are no known functional failures due to this issue.

Note: Set latency tolerance value command is specific to the controller and not the slot. Software knows which command was issued and which fields are valid to check for the event.

Workaround: None.

Status: No Plan to Fix

20. LFPS Detect Threshold

Problem: The xHC LFPS (Low Frequency Periodic Signal) detect threshold of 400 mV is higher than the USB 3.0 specification maximum of 300 mV.

Implication: The xHC may not recognize LFPS from SuperSpeed devices transmitting at the minimum low power peak-to-peak differential voltage (400 mV) as defined by USB 3.0 specification.

Note: The low power peak-to-peak voltage transmission level is intended for devices soldered down to the motherboard.

Workaround: None.

Note: For optimal interoperability across all implementations, Intel recommends that designs utilize soldered down SuperSpeed devices that support standard peak-to-peak differential voltage levels (800 mV minimum).

Status: No Plan to Fix

21. SMBus Hold Time

Problem: The SMBus data hold time may be less than the 300 ns minimum defined by the Intel 8 Series / C220 Series Chipset Family Platform Controller Hub External Design Specification (EDS).

Implication: There are no known functional failures due to this issue.

Workaround: None.

Status: No Plan to Fix

22. RMH Port Disabled Due to Device Initiated Remote Wake

Problem: During resume from Global Suspend, the RMH controller may not send SOF soon enough to prevent a device from entering suspend again. A collision on the port may occur if a device initiated remote wake occurs before the RMH controller sends SOF.

Note: Intel has only observed this issue when two USB devices on the same RMH controller send remote wake within 30ms window while RMH controller is resuming from Global Suspend

Implication: The RMH host controller may detect the collision as babble and disable the port.

Workaround: Intel recommends system software to check bit 3 (Port Enable/Disable Change) together with bit 7 (Suspend) of Port N Status and Control PORTC registers when determining which port(s) have initiated remote wake.

Status: No plan to fix.

23. Enumeration Issue when Resuming for Sx

Problem: If a device is attached while the platform is in S3 or S4 and the device is assigned the highest assignable Slot ID upon resume, the xHC may attempt to access an unassigned main memory address.

Implication: Accessing unassigned main memory address may cause a system software timeout leading to possible system hang.

Workaround: System Software can detect the timeout and perform a host controller reset to avoid the system hang.

Note: Microsoft* Windows 8* xHC in-box driver detects and performs a host controller reset. The Intel Windows 7* xHC driver revision 2.5.0.19 or later will also detect and perform the host controller reset.

Status: No Plan to Fix

24. SATA Lock Lost with During Link Negotiation

Problem: During link speed negotiation, if a receiver error occurs after host SATA controller locks on a device's ALIGN primitive, the host SATA controller may be unable to train the link.

Note: This issue only occurs when SSC is disabled on the drive and has only been observed at SATA Gen2 speeds.

Implication: A SATA device connected to the SATA controller may fail to train and become inoperative.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No plan to fix

25. PCIe* Clocking Mode Switch Issue

Problem: The PCIe link may become unstable when switching from non-common clock mode to common clock mode with some PCIe devices.

Implication: The PCIe link may report link errors or train to a lower speed. Implication is device dependent.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No plan to fix.

26. USB xHCI may Execute a Stale Transfer Request Block (TRB)

Problem: When a USB 3.0 or USB 2.0 hub with numerous active Full-Speed (FS) or Low-Speed (LS) periodic endpoints attached is removed and then reconnected to an USB xHCI port, the xHCI controller may fail to fully refresh its cache of TRB records. The controller may read and execute a stale TRB and place a pointer to it in a Transfer Event TRB.

Implication: In some cases, the xHCI controller may read de-allocated memory pointed to by a TRB of a disabled slot. The xHCI controller may also place a pointer to that memory in the event ring, causing the xHCI driver to access that memory and process its contents, resulting in system hang, failure to enumerate devices, or other anomalous system behavior.

Note: This issue has only been observed in a stress test environment.

Workaround: None.

Note: A BIOS code change has been identified to reduce the occurrence and may be implemented as a mitigation for this erratum.

Status: No plan to fix.

27. Clearing xHCI PME_EN May Not Disable USB 2.0 Wake Events

Problem: System software writes to clear the xHCI PME_EN bit 8 in the Power Management Control / Status Register (B0:D20:F0, Offset 0x74) may not have any functional impact.

Implication: System software may be unable to prevent xHCI port USB 2.0 wake events from occurring during S3/S4/S5.

Workaround: System software can clear the xHCI Port Power bit 9 in the Port N Status and Control USB2 Register to disable USB wake events during S3/S4/S5. System software must set the bit upon resume from S3/S4/S5 for normal operation.

Note: This workaround needs to be applied to the xHC on a port-by-port basis for portswhich USB 2.0 wake events are not desired.

Status: No Plan to Fix.

28. xHCI Controller May Delayed Transactions Due to Short Packets Issue

Problem: If the software driver for a device continuously schedules large Transfer Descriptors (TDs) and the device frequently responds with a short packet (defined in the USB specification), the xHCI Host controller may delay service to other device's endpoints.

Implication: The implication is device dependent.

- Full-speed and Low-speed devices with Interrupt IN endpoints connected to the xHCI controller behind a USB 2.0 hub may experience split transaction errors causing the USB 2.0 hub and USB devices behind the hub to be re-enumerated.
- Isochronous devices connected to the xHCI controller may experience dropped packets
  - — Dropped audio or video packets may or may not result in end user detectable impact.

Note: Intel has observed these implications only with limited devices using bulk transfers to continuously send TDs: certain models of high resolution SuperSpeed cameras and High-speed scanners.

Workaround: None

Status: No plan to fix.

29. xHCI Controller D3 Entry Issue – External

Problem: xHCI Host Controller may not enter D3 if a USB 2.0 device wake event happens when software is writing to the USB xHCI—PWR_CNTL_STS (D20:F0:0x74) register to enter D3.

Implication: All xHCI Ports may become non-functional.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Plan to Fix.

30. xHCI USB2.0 Split-Transactions Error Counter Reset Issue

Problem: The xHCI controller may not reset its split transaction error counter if a high-speed USB hub propagates a mal-formed bit from a low-speed or full-speed USB device exhibiting non-USB specification compliant signal quality.

Implication: The implication is device dependent.

- Full Speed and Low Speed devices behind the hub may be re-numerated and may cause a device to not function as expected.

Workaround: None

Status: For the steppings affected, see the Summary of Changes.

31. Unexpected USB 2.0 HS Controller Signal Amplitude.

Problem: USB2.0 High Speed (HS) devices connected to the xHCI controller through long USB cables may see packet errors following SOF due to unexpected shift in the USB 2.0 HS Host signal amplitude.

Implication: May cause multiple transaction errors causing software to drop the USB device.
Note: USB 2.0 HS Device devices connected to the EHCI Host recover and not drop.

Workaround: None. Contact your Intel representative for possible mitigation.

Status: For the steppings affected, see the Summary of Changes.

Specification Changes

There are no specification changes in this revision of the specification update.

Specification Clarifications

1. Intel® Ethernet Network Connection 1127

There is a typo in the Datasheet Functional Description chapter when referencing the Intel Ethernet Network Connection 1127 networking part. The part number is 1127, not l127.

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