PMV117EN

μTrenchMOS™ enhanced logic level FET

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1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS™ technology.

1.2 Features

- Logic level threshold
- Subminiature surface-mounted package
- Very fast switching

1.3 Applications

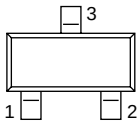
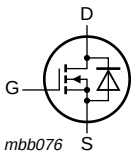
- Battery management
- High-speed switch
- Low power DC-to-DC converter

1.4 Quick reference data

- $V_{DS} \leq 30$ V
- $R_{DSon} \leq 117$ mΩ (V_{GS} = 10 V)
- $I_D \leq 2.5$ A
- $P_{tot} \leq 0.83$ W

2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1	gate (G)		
2	source (S)		
3	drain (D)		

SOT23

3. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
PMV117EN	TO-236AB	plastic surface mounted package; 3 leads	SOT23

4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	25 °C ≤ T_j ≤ 150 °C	-	30	V
V_{DGR}	drain-gate voltage (DC)	25 °C ≤ T_j ≤ 150 °C; R_{GS} = 20 kΩ	-	30	V
V_{GS}	gate-source voltage (DC)		-	±20	V
I_D	drain current (DC)	T_{sp} = 25 °C; V_{GS} = 10 V; Figure 2 and 3	-	2.5	A
		T_{sp} = 100 °C; V_{GS} = 10 V; Figure 2	-	1.6	A
I_{DM}	peak drain current	T_{sp} = 25 °C; pulsed; t_p ≤ 10 μs; Figure 3	-	10	A
P_{tot}	total power dissipation	T_{sp} = 25 °C; Figure 1	-	0.83	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–65	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	T_{sp} = 25 °C	-	0.8	A
I_{SM}	peak source (diode forward) current	T_{sp} = 25 °C; pulsed; t_p ≤ 10 μs	-	3.3	A

5. Characteristics

Table 4: Characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0 V				
		T_j = 25 °C	30	37	-	V
		T_j = –55 °C	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 9 and 10				
		T_j = 25 °C	1.5	2	-	V
		T_j = 150 °C	1.1	-	-	V
		T_j = –55 °C	-	-	2.7	V
I_{DSS}	drain-source leakage current	V_{DS} = 24 V; V_{GS} = 0 V				
		T_j = 25 °C	-	0.01	0.5	μA
		T_j = 150 °C	-	-	10	μA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 500 mA; Figure 6 and 8				
		T_j = 25 °C	-	74	117	mΩ
		V_{GS} = 4.5 V; I_D = 500 mA; Figure 6 and 8	-			
		T_j = 25 °C	-	117	190	mΩ
		T_j = 150 °C		188	300	mΩ
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	I_D = 0.5 A; V_{DD} = 15 V; V_{GS} = 10 V; Figure 11	-	4.6	-	nC
Q_{gs}	gate-source charge		-	0.6	-	nC
Q_{gd}	gate-drain (Miller) charge		-	1.35	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 10 V; f = 1 MHz; Figure 13	-	147	-	pF
C_{oss}	output capacitance		-	65	-	pF
C_{rss}	reverse transfer capacitance		-	41	-	pF
$t_{d(on)}$	turn-on delay time	V_{DD} = 15 V; R_L = 15 Ω; V_{GS} = 10 V	-	4	-	ns
t_r	rise time		-	7.5	-	ns
$t_{d(off)}$	turn-off delay time		-	18	-	ns
t_f	fall time		-	13	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 0.83 A; V_{GS} = 0 V; Figure 12	-	0.7	1.2	V
t_{rr}	reverse recovery time	I_S = 1 A; dI_S/dt = –100 A/μs; V_{GS} = 0 V; V_{DS} = 25 V	-	69	-	ns