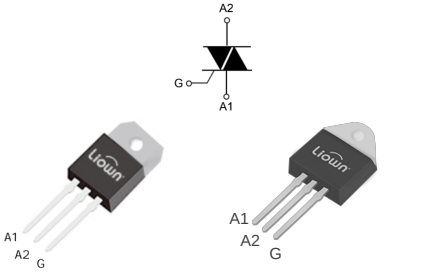
LTR24A,LTR24B,LTR26A,LTR26B,LTR25
25A standard and Snubberless™ Triacs

Symbol	LTR24A	LTR24B	LTR26A	LTR26B	LTR25	Unit
$I_{T(RMS)}$	24	24	26	26	25	A
V_{DRM}/V_{RRM}	800	800	800	800	800	V
I_{GT} (Snubberless)	30 to 70	30 to 70	30 to 70	-	35	mA
I_{GT} (Standard)	-	35	35	50	-	mA

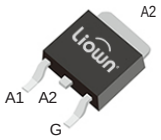
Features

- High current triac
- Low thermal resistance with clip bonding
- High commutation (4 quadrant) or very high commutation (3 quadrant) capability



TO-220AB Insulated (LTR24)

TOP3 (LTR26)



D2PAK(LTR25)

Applications

Applications include the ON/OFF function in applications such as static relays, heating regulation, induction motor starting circuits, etc., or for phase control operation in light dimmers, motor speed controllers, and similar.

The snubberless versions are especially recommended for use on inductive loads, due to their high commutation performances.

Description

Available either in through-hole or surface-mount packages, the LTR24, LTR25 and LTR26 triac series is suitable for general purpose mains power AC switching.

Absolute maximum ratings

Symbol	Parameter			Value	Unit
$I_{T(RMS)}$	RMS on-state current (full sine wave)	TOP3	T_c = 105° C	25	A
		D^2PAK / TO-220AB	T_c = 100° C		
		RD91 Ins/ TOP3 Ins.	T_c = 100° C		
		TO-220AB Ins.	T_c = 75° C		
I_{TSM}	Non repetitive surge peak on-state current (full cycle, T_j initial = 25° C)	F = 50 Hz	t = 20 ms	240	A
		F = 60 Hz	t = 16.7 ms	260	
I^2t	I^2t Value for fusing	t_p = 10 ms		340	A^2s
dI/dt	Critical rate of rise of on-state current I_G = 2 x I_{GT} , $t_r \leq$ 100 ns	F = 120 Hz	T_j = 125° C	50	A/µs
V_{DSM}/V_{RSM}	Non repetitive surge peak off-state voltage	t_p = 10 ms	T_j = 25° C	V_{DRM}/V_{RRM} + 100	V
I_{GM}	Peak gate current	t_p = 20 µs	T_j = 125° C	4	A
$P_{G(AV)}$	Average gate power dissipation		T_j = 125° C	1	W
T_{stg} T_j	Storage junction temperature range Operating junction temperature range			- 40 to + 150 - 40 to + 125	° C

Electrical characteristics (T_j = 25° C, unless otherwise specified), Snubberless and logic level (3 quadrants)

Symbol	Test Conditions	Quadrant		LTR25	LTRA / LTRB		Unit
				LTR2535	CW	BW	
I_{GT} (1)	V_D = 12 V R_L = 33 Ω	I - II - III	MAX.	35	35	70	mA
V_{GT}		I - II - III	MAX.	1.3			V
V_{GD}	$V_D = V_{DRM}$ R_L = 3.3 kΩ T_j = 125° C	I - II - III	MIN.	0.2			V
I_H (2)	I_T = 500 mA		MAX.	50	50	75	mA
I_L	I_G = 1.2 I_{GT}	I - III	MAX.	70	70	80	mA
		II		80	80	100	
dV/dt (2)	V_D = 67 %V_{DRM} gate open	T_j = 125° C	MIN.	500	500	1000	V/µs
(dI/dt)c (2)	Without snubber	T_j = 125° C	MIN.	13	13	22	A/ms

1. minimum I_{GT} is guaranted at 5% of I_{GT} max.
2. for both polarities of A2 referenced to A1.

Electrical characteristics (T_j = 25° C, unless otherwise specified), standard (4 quadrants)

Symbol	Test Conditions	Quadrant		Value	Unit
I_{GT} (1)	V_D = 12 V R_L = 33 Ω	I - II - III	MAX.	50	mA
		IV		100	
V_{GT}		ALL	MAX.	1.3	V
V_{GD}	$V_D = V_{DRM}$ R_L = 3.3 kΩ T_j = 125° C	ALL	MIN.	0.2	V
I_H(2))	I_T = 500 mA		MAX.	80	mA
I_L	I_G = 1.2 I_{GT}	I - III - IV	MAX.	70	mA
		II		160	
dV/dt(2)	V_D = 67 %V_{DRM} gate open	T_j = 125° C	MIN.	500	V/µs
(dV/dt)c (2)	(dI/dt)c = 13.3 A/ms	T_j = 125° C	MIN.	10	V/µs

1. minimum I_{GT} is guaranted at 5% of I_{GT} max.
2. for both polarities of A2 referenced to A1.

Static characteristics

Symbol	Test Conditions			Value	Unit
V_{TM} (1)	I_{TM} = 35 A t_p = 380 µs	T_j = 25° C	MAX.	1.35	V
V_{t0} (1)	Threshold voltage	T_j = 125° C	MAX.	0.85	V
R_d (1)	Dynamic resistance	T_j = 125° C	MAX.	16	mΩ
I_{DRM}	$V^{DRM} = V^{RRM}$	T_j = 25° C	MAX.	5	µA
I_{RRM}		T_j = 125° C		3	mA

1. for both polarities of A2 referenced to A1.

Thermal resistance

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	Junction to case (AC)	TOP 3	0.6	° C/W
		D^2PAK / TO-220AB	0.8	
		RD91 Insulated / TOP3 Insulated	0.9	
		TO-220AB Insulated	1.7	
$R_{th(j-a)}$	Junction to ambient (1)S = 1 cm^2	D^2PAK	45	° C/W
		TOP3 / TOP3 Insulated	50	
		TO-220AB / TO-220AB Insulated	60	

1. S = Copper surface under tab.

Figure 1. Maximum power dissipation versus RMS on-state current (full cycle)

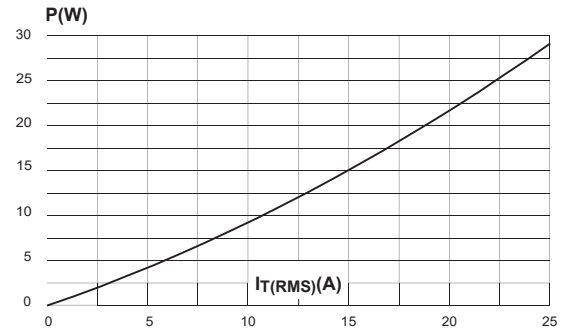


Figure 2. RMS on-state current versus case temperature (full cycle)

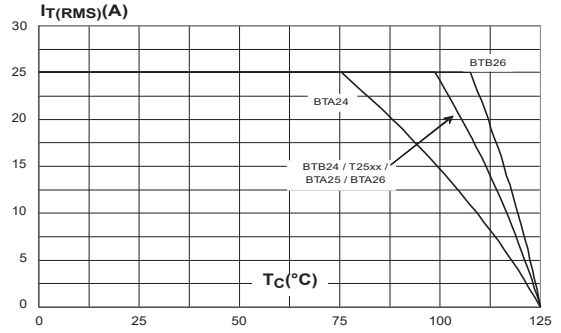


Figure 3. D^2PAK RMS on-state current versus ambient temperature (printed circuit board FR4, copper thickness: 35µm) (full cycle)

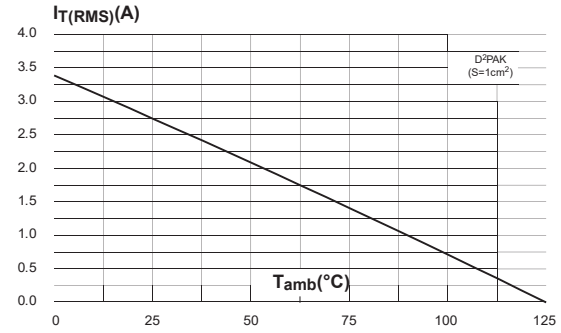


Figure 4. Relative variation of thermal impedance versus pulse duration

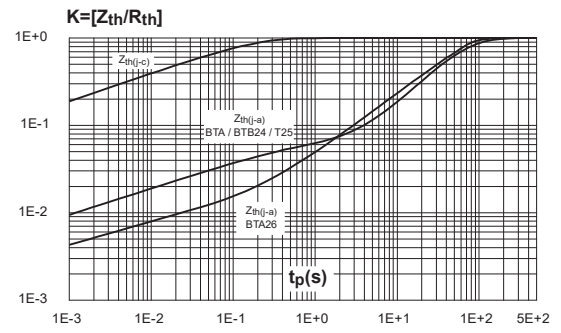


Figure 5. On-state characteristics (maximum values)

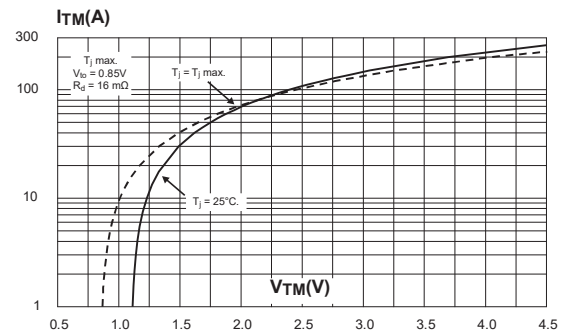


Figure 6. Surge peak on-state current versus number of cycles

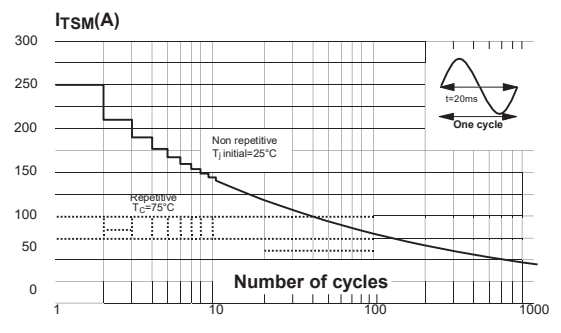


Figure 7. Non-repetitive surge peak on-state current for a sinusoidal pulse with width t_p < 10 ms and corresponding value of I^2t

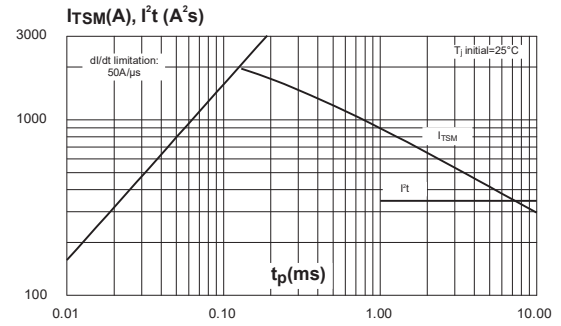


Figure 8. Relative variation of gate trigger current, holding current and latching current versus junction temperature (typical values)

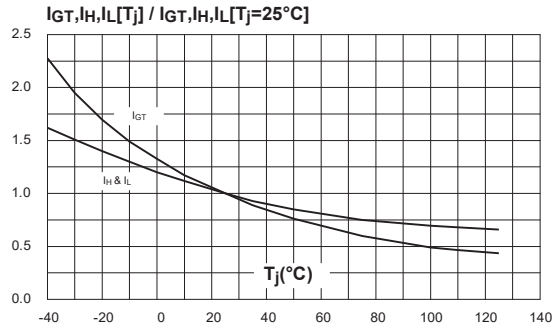


Figure 9. Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values)

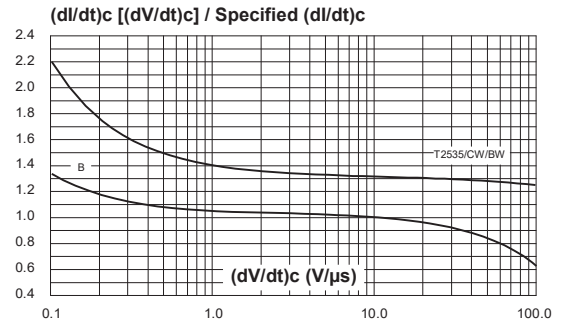


Figure 10. Relative variation of critical rate of decrease of main current versus T_j

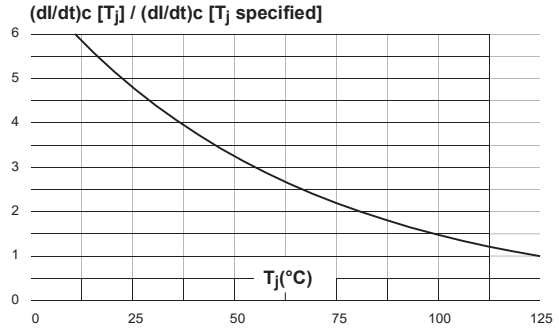


Figure 11. D^2PAK thermal resistance junction to ambient versus copper surface under tab (printed circuit board FR4, copper thickness: 35 µm)