

# 74HCT32

## Quad 2-Input OR Gate with LSTTL-Compatible Inputs

### High-Performance Silicon-Gate CMOS

The 74HCT32 is identical in pinout to the LS32. The device has TTL-compatible inputs.

#### Features

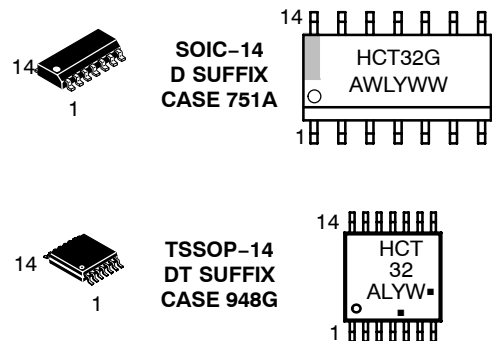
- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7A Requirements
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 48 FETs or 12 Equivalent Gates
- These are Pb-Free Devices



ON Semiconductor®

<http://onsemi.com>

#### MARKING DIAGRAMS



HCT32 = Device Code  
A = Assembly Location  
L, WL = Wafer Lot  
Y = Year  
W, WW = Work Week  
G or ■ = Pb-Free Package

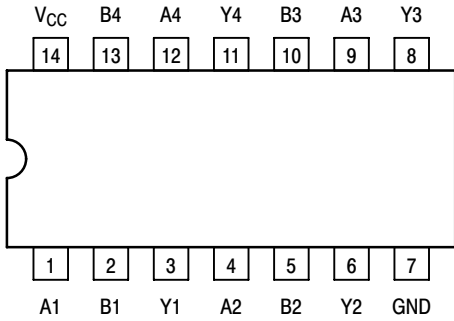
(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# 74HCT32

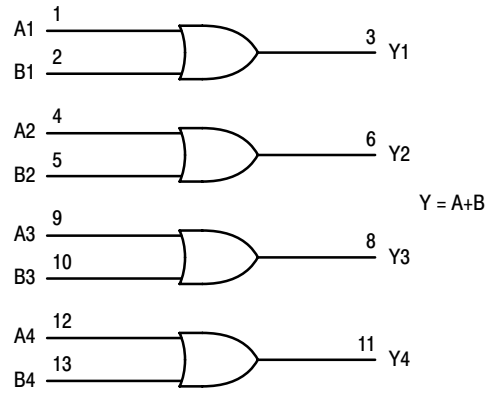
## Pinout: 14-Lead Packages (Top View)



## FUNCTION TABLE

| Inputs |   | Output |
|--------|---|--------|
| A      | B | Y      |
| L      | L | L      |
| L      | H | H      |
| H      | L | H      |
| H      | H | H      |

## LOGIC DIAGRAM



PIN 14 = V<sub>CC</sub>  
PIN 7 = GND

## ORDERING INFORMATION

| Device       | Package              | Shipping <sup>†</sup> |
|--------------|----------------------|-----------------------|
| 74HCT32DR2G  | SOIC-14<br>(Pb-Free) | 2500 / Tape & Reel    |
| 74HCT32DTR2G | TSSOP-14*            |                       |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

# 74HCT32

## MAXIMUM RATINGS

| Symbol    | Parameter  | Value                   | Unit |
|-----------|--|-------------------------|------|
| $V_{CC}$  | DC Supply Voltage (Referenced to GND)                                    | - 0.5 to + 7.0          | V    |
| $V_{in}$  | DC Input Voltage (Referenced to GND)                                     | - 0.5 to $V_{CC} + 0.5$ | V    |
| $V_{out}$ | DC Output Voltage (Referenced to GND)                                    | - 0.5 to $V_{CC} + 0.5$ | V    |
| $I_{in}$  | DC Input Current, per Pin  | $\pm 20$                | mA   |
| $I_{out}$ | DC Output Current, per Pin   | $\pm 25$                | mA   |
| $I_{CC}$  | DC Supply Current, $V_{CC}$ and GND Pins                                 | $\pm 50$                | mA   |
| $P_D$     | Power Dissipation in Still Air, SOIC Package†<br>TSSOP Package†          | 500<br>450              | mW   |
| $T_{stg}$ | Storage Temperature  | - 65 to + 150           | °C   |
| $T_L$     | Lead Temperature, 1 mm from Case for 10 Seconds<br>SOIC or TSSOP Package | 260                     | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — SOIC Package: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

## RECOMMENDED OPERATING CONDITIONS

| Symbol            | Parameter  | Min  | Max      | Unit |
|-------------------|--|------|----------|------|
| $V_{CC}$          | DC Supply Voltage (Referenced to GND)                | 4.5  | 5.5      | V    |
| $V_{in}, V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0    | $V_{CC}$ | V    |
| $T_A$             | Operating Temperature, All Package Types             | - 55 | + 125    | °C   |
| $t_r, t_f$        | Input Rise and Fall Time<br>(Figure 1)               |      |          |      |
|                   | $V_{CC} = 2.0 \text{ V}$                             | 0    | 1000     | ns   |
|                   | $V_{CC} = 4.5 \text{ V}$                             | 0    | 500      |      |
|                   | $V_{CC} = 6.0 \text{ V}$                             | 0    | 400      |      |

# 74HCT32

## DC CHARACTERISTICS (Voltages Referenced to GND)

| Symbol           | Parameter                                      | Condition   | V <sub>CC</sub><br>(V) | Guaranteed Limit |             |        | Unit |
|------------------|--|---|------------------------|------------------|-------------|--------|------|
|                  |  |   |                        | -55 to 25°C      | ≤85°C       | ≤125°C |      |
| V <sub>IH</sub>  | Minimum High-Level Input Voltage               | V <sub>out</sub> = 0.1V<br> I <sub>out</sub>   ≤ 20μA   | 4.5                    | 2.0              | 2.0         | 2.0    | V    |
|                  |  |   | 5.5                    | 2.0              | 2.0         | 2.0    |      |
| V <sub>IL</sub>  | Maximum Low-Level Input Voltage                | V <sub>out</sub> = V <sub>CC</sub> - 0.1V<br> I <sub>out</sub>   ≤ 20μA   | 4.5                    | 0.8              | 0.8         | 0.8    | V    |
|                  |  |   | 5.5                    | 0.8              | 0.8         | 0.8    |      |
| V <sub>OH</sub>  | Minimum High-Level Output Voltage              | V <sub>in</sub> = V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20μA   | 4.5                    | 4.4              | 4.4         | 4.4    | V    |
|                  |  | V <sub>in</sub> = V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0mA   | 5.5                    | 5.4              | 5.4         | 5.4    |      |
| V <sub>OL</sub>  | Maximum Low-Level Output Voltage               | V <sub>in</sub> = V <sub>IH</sub><br> I <sub>out</sub>   ≤ 20μA   | 4.5                    | 0.1              | 0.1         | 0.1    | V    |
|                  |  | V <sub>in</sub> = V <sub>IH</sub>  I <sub>out</sub>   ≤ 4.0mA   | 5.5                    | 0.1              | 0.1         | 0.1    |      |
| I <sub>in</sub>  | Maximum Input Leakage Current                  | V <sub>in</sub> = V <sub>CC</sub> or GND  | 5.5                    | ±0.1             | ±1.0        | ±1.0   | μA   |
| I <sub>CC</sub>  | Maximum Quiescent Supply Current (per Package) | V <sub>in</sub> = V <sub>CC</sub> or GND<br>I <sub>out</sub> = 0μA  | 5.5                    | 2.0              | 20          | 40     | μA   |
| ΔI <sub>CC</sub> | Additional Quiescent Supply Current            | V <sub>in</sub> = 2.4V, Any One Input<br>V <sub>in</sub> = V <sub>CC</sub> or GND, Other Inputs<br>I <sub>out</sub> = 0μA | 5.5                    | ≥ -55°C          | 25 to 125°C |        | mA   |
|                  |  |   |                        | 2.9              | 2.4         |        |      |

- Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).
- Total Supply Current = I<sub>CC</sub> + ΣΔI<sub>CC</sub>.

## AC CHARACTERISTICS (C<sub>L</sub> = 50pF, Input t<sub>r</sub> = t<sub>f</sub> = 6ns)

| Symbol                                 | Parameter  | V <sub>CC</sub><br>(V) | Guaranteed Limit |       |        | Unit |
|--|--|------------------------|------------------|-------|--------|------|
|  |  |                        | -55 to 25°C      | ≤85°C | ≤125°C |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Input A or B to Output Y<br>(Figures 1 and 2) | 4.5                    | 15               | 19    | 22     | ns   |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Maximum Output Transition Time, Any Output<br>(Figures 1 and 2)          | 4.5                    | 15               | 19    | 22     | ns   |
| C <sub>in</sub>                        | Maximum Input Capacitance  |                        | 10               | 10    | 10     | pF   |

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

| C <sub>PD</sub> | Power Dissipation Capacitance (Per Buffer)* | Typical @ 25°C, V <sub>CC</sub> = 5.0 V, V <sub>EE</sub> = 0 V |  | pF |
|-----------------|---|--|--|----|
|                 |   | 20   |  |    |
|                 |   |  |  |    |

\* Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>. For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

# 74HCT32

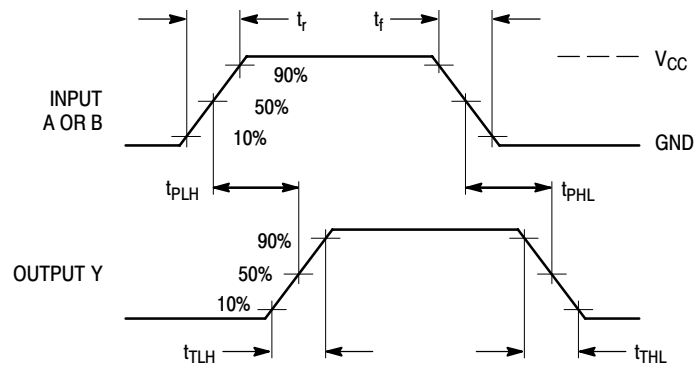
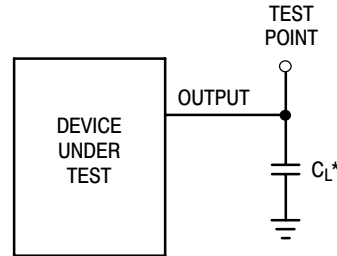


Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance

Figure 2. Test Circuit

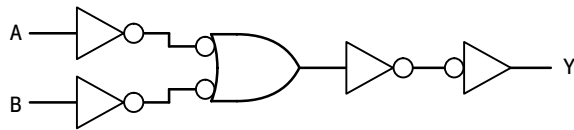


Figure 3. Expanded Logic Diagram  
(1/4 of the Device)

# 74HCT32

## PACKAGE DIMENSIONS

SOIC-14  
CASE 751A-03  
ISSUE H

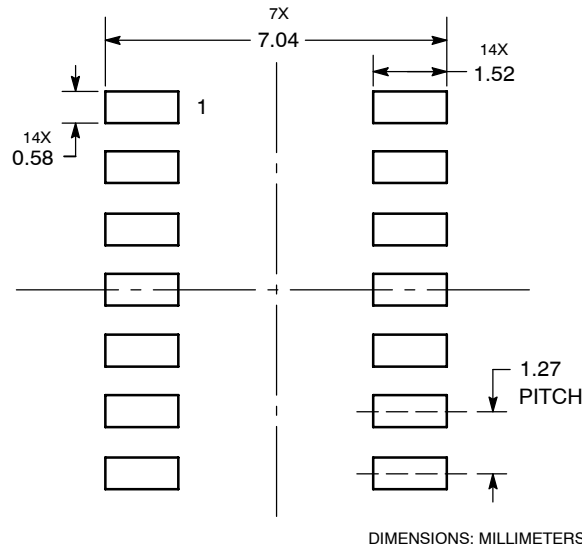


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 8.55        | 8.75 | 0.337     | 0.344 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.054     | 0.068 |
| D   | 0.35        | 0.49 | 0.014     | 0.019 |
| F   | 0.40        | 1.25 | 0.016     | 0.049 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| J   | 0.19        | 0.25 | 0.008     | 0.009 |
| K   | 0.10        | 0.25 | 0.004     | 0.009 |
| M   | 0°          | 7°   | 0°        | 7°    |
| P   | 5.80        | 6.20 | 0.228     | 0.244 |
| R   | 0.25        | 0.50 | 0.010     | 0.019 |

**SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



**ON Semiconductor** and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local  
Sales Representative