

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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MOS FIELD EFFECT TRANSISTOR
 μ PA2703GR

SWITCHING
 N-CHANNEL POWER MOS FET

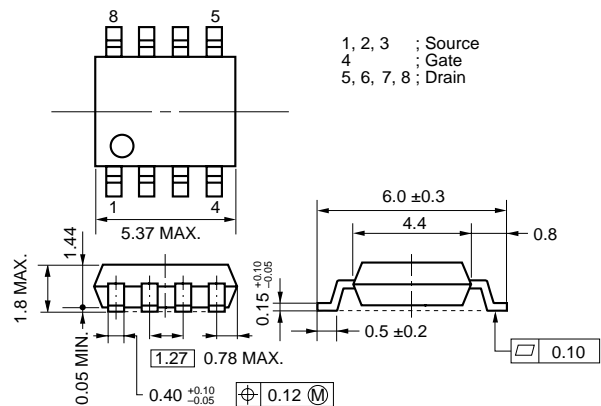
DESCRIPTION

The μ PA2703GR is N-Channel MOS Field Effect Transistor designed for DC/DC converters and power management applications of notebook computers.

FEATURES

- Low on-state resistance
 $R_{DS(on)1} = 4.2 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 9.0 \text{ A)}$
 $R_{DS(on)2} = 6.4 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 9.0 \text{ A)}$
- Low C_{iss} : $C_{iss} = 2600 \text{ pF TYP. (} V_{DS} = 10 \text{ V, } V_{GS} = 0 \text{ V)}$
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit: mm)



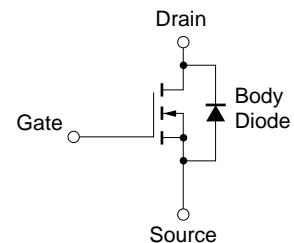
ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA2703GR	Power SOP8

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, All terminals are connected.)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DS}	30	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 17	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 68	A
Total Power Dissipation ($T_A = 25^\circ\text{C}$) ^{Note2}	P_T	2.2	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	$-55 \text{ to } +150$	$^\circ\text{C}$
Single Avalanche Current ^{Note3}	I_{AS}	17	A
Single Avalanche Energy ^{Note3}	E_{AS}	28.9	mJ

EQUIVALENT CIRCUIT



- Notes**
1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$
 2. Mounted on ceramic substrate of $1200 \text{ mm}^2 \times 2.2 \text{ mm}$
 3. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 15 \text{ V}$, $R_G = 25 \Omega$, $L = 100 \mu\text{H}$, $V_{GS} = 20 \rightarrow 0 \text{ V}$

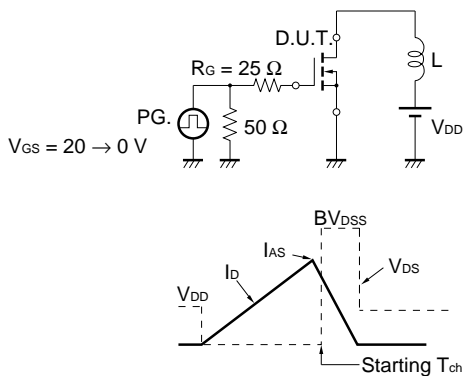
Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.
 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

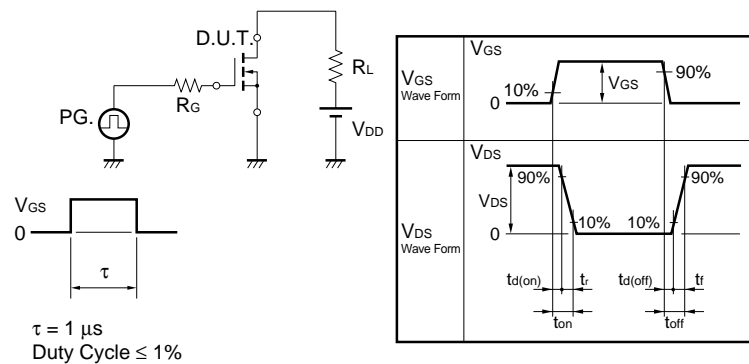
ELECTRICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±100	nA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5		2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 9.0 A	11	21.5		S
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 9.0 A		3.3	4.2	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 9.0 A		4.5	6.4	mΩ
	R _{DS(on)3}	V _{GS} = 4.0 V, I _D = 9.0 A		5.7	7.6	mΩ
Input Capacitance	C _{iss}	V _{DS} = 10 V		2600		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		1000		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		340		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 15 V, I _D = 9.0 A		20		ns
Rise Time	t _r	V _{GS} = 10 V		24		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		75		ns
Fall Time	t _f			22		ns
Total Gate Charge	Q _G	V _{DD} = 15 V		26		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 5 V		7		nC
Gate to Drain Charge	Q _{GD}	I _D = 17 A		11		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 17 A, V _{GS} = 0 V		0.8	1.2	V
Reverse Recovery Time	t _{rr}	I _F = 17 A, V _{GS} = 0 V		50		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		51		nC

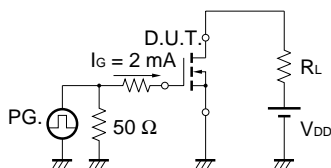
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE



[MEMO]

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