General Description

The 8400110 is a Low Jitter Telecom Rate-Conversion PLL that provides accurate and reliable frequency conversion.

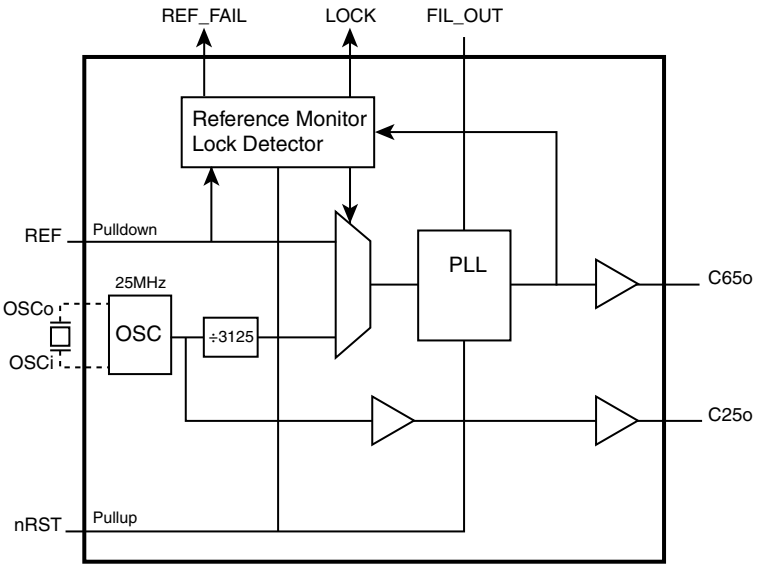
The 8400110 generates a 65.536MHz clock that is either locked to the input reference or locked to the external crystal or oscillator.

In the locked mode, the reference input is continuously monitored for a failure condition. In the event of a failure, the PLL continues to provide a stable free-running clock, ensuring system reliability.

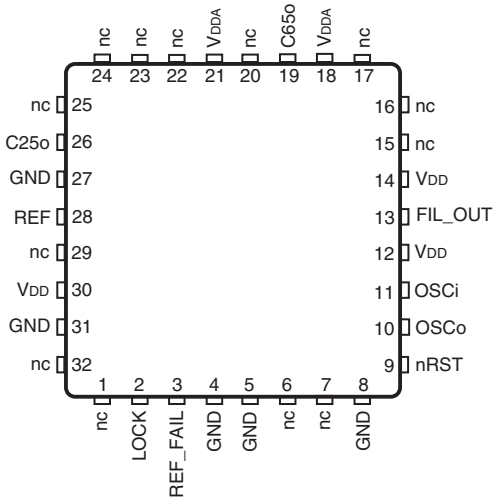
Features

- One 65.536MHz output, synchronized to 8kHz reference
- One 25MHz output, buffered version of the internal osc output
- Provides lock and reference fail indication
- Free run mode when reference clock (REF) fails
- Automatic switch-over to reference when good reference (REF) is available
- 25MHz external master clock source: crystal or oscillator
- Full 3.3V operation
- -40°C to 85°C ambient operating temperature
- Available in a lead-free (RoHS 6) package

Block Diagram



Pin Assignment



8400110

32-Lead VFQFN
5mm x 5mm x 0.925mm package body
K Package
Top View

Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 6, 7, 15, 16, 17, 20, 22, 23, 24, 25, 29, 32	nc	Unused		No connect.
2	LOCK	Output		Lock indicator. When HIGH, the PLL is frequency locked to a valid input reference. LVCMOS/LVTTL interface levels.
3	REF_FAIL	Output		Reference fail indicator. A logic HIGH at this output indicates that the reference (REF) frequency is exhibiting abrupt phase or frequency change. LVCMOS/LVTTL interface levels.
4, 5, 8, 27, 31	GND	Power		Power supply ground.
9	nRST	Input	Pullup	Reset. A logic LOW at this input resets the device. In Reset state, all outputs are forced into high-impedance. LVCMOS/LVTTL interface levels.
10	OSCo	Output		Crystal out.
11	OSCi	Input		Crystal in or single ended clock input.
12, 14, 30	V_{DD}	Power		Core supply pins.
13	FIL_OUT	Output		Filter output pin connected to 4.7µF capacitor.
18, 21	V_{DDA}	Power		Analog supply pins.
19	C65o	Output		Single-ended clock output, 65.536MHz frequency. This output is used for general TDM applications. LVCMOS/LVTTL interface levels.
26	C25o	Output		Single-ended clock output, 25MHz frequency. This is a buffered version of internal crystal oscillator. The phase and frequency accuracy of this output tracks that of the external crystal or oscillator. LVCMOS/LVTTL interface levels.
28	REF	Input	Pulldown	This is the input reference source used for synchronization. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance	V_{DDO} = 3.6V		17		Ω

Functional Description

The PLL of 8400110 consists of a phase detector, a loop filter and a Voltage Controlled Oscillator (VCO). In the normal mode of operation, the VCO provides an output clock signal that is frequency and phase locked to the input reference clock (REF). In free-run mode, VCO is locked to 25MHz input with an accuracy equal to the accuracy of the OSCi 25MHz clock.

Lock Indicator

The Lock detector monitors if the output clock phase is within 90° of the input reference (REF). If the difference between input reference clock (REF) and output is more than 90°, LOCK output is LOW. The monitor than looks for eight consecutive clocks within 22.5° of the reference, before setting the LOCK to a HIGH.

REF_FAIL

The REF_FAIL signal is HIGH when reference clock (REF) shows greater than 130ppm variation in frequency, there are more than three consecutive edges missing, or there is an abrupt phase shift in the reference clock REF. Under any of these circumstances the PLL input will be switched from primary reference clock (REF) to crystal. When the primary reference clock (REF) is restored and REF_FAIL sets to LOW, the PLL input is switched back to the primary reference clock (REF).

Modes of Operation

The 8400110 device has two modes of operation; normal mode and free-run mode. The device powers up in free-run mode, it automatically transitions to normal mode if a valid reference clock (REF) is available and transitions to free-run mode if the reference fails. RESET signal also will puts the device in free-run mode.

Freerun Mode

The freerun mode is typically used when an asynchronous clock source is required or it is used immediately following system power-up before synchronization is achieved. In free-run mode, 8400110 provides an output clock based on oscillator frequency. The output is not synchronized to the reference input clock (REF). In the free-run mode the accuracy of output frequency is equal to the accuracy of the frequency of the oscillator.

Normal Mode

The normal mode is typically used when a synchronous clock is required. In normal mode, 8400110 provides an output clock which is synchronized to the input (REF).

Lock Time

This is the time it takes the PLL to lock to the input reference clock REF. Lock occurs when the input signal and output signal are aligned in phase and frequency with respect to each other. LOCK time is affected by many factors which include:

- Initial input to output phase difference
- Initial input to output frequency difference
- PLL loop bandwidth

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	37°C/W
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.0	3.3	3.6	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.075	3.3	V_{DD}	V
I_{DD}	Power Supply Current	Output Frequency = 65MHz			130	mA
I_{DDA}	Analog Supply Current	Output Frequency = 65MHz			15	mA

Table 3B. LVCMOS DC Characteristics, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input Current High	REF	V_{DD} = V_{IN} = 3.6V			150	µA
		nRST	V_{DD} = V_{IN} = 3.6V			5	µA
I_{IL}	Input Current Low	REF	V_{DD} = 3.6V, V_{IN} = 0V	-5			µA
		nRST	V_{DD} = 3.6V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage	C65o, C25o, REF_FAIL, LOCK	V_{DD} = 3.6V, I_{OH} = -12mA	2.6			V
V_{OL}	Output Low Voltage	C65o, C25o, REF_FAIL, LOCK	V_{DD} = 3.6V, I_{OL} = 12mA			0.5	V

Table 4. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

AC Electrical Characteristics

Table 5. AC Characteristics, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
t_{REFW}	Reference Pulse Width High or Low	f = 8kHz	15			ns
t_{C65L}	C65o Pulse Width Low	f = 65.536MHz	7.0		8	ns
t_{ORF}	Output Clock Rise or Fall Time	Rise/Fall Time, 20% to 80%, 15pF Load	1.05		2.1	ns
t_{C25L}	C25o Pulse Width Low		19		21	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

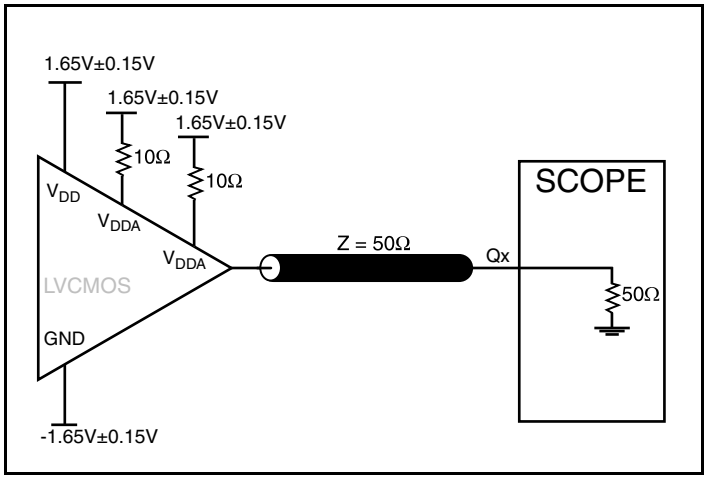
Performance Characteristics

Table 6. Functional Performance Characteristics

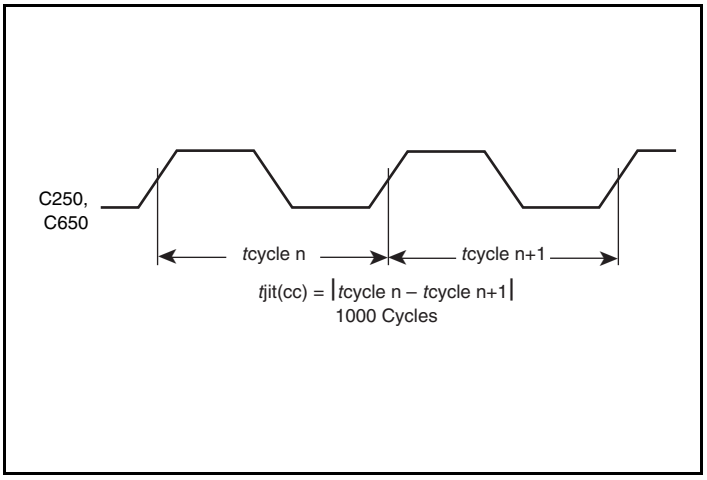
Characteristics	Test Conditions	Minimum	Typical	Maximum	Units
PLL Capture Range		-150		150	ppm
PLL Lock Time	REF = 8kHz			1	s
C65o Cycle-to-Cycle Jitter	C65o = 65.536MHz			100	ps
Peak-to-Peak Jitter C65.536; NOTE 1	C65o = 65.536MHz			175	ps
RMS Phase Jitter C25o	25MHz Crystal Input, 12kHz to 5MHz		1		ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Peak-to-Peak jitter was calculated with RMS Period jitter data multiplied by BER 14.

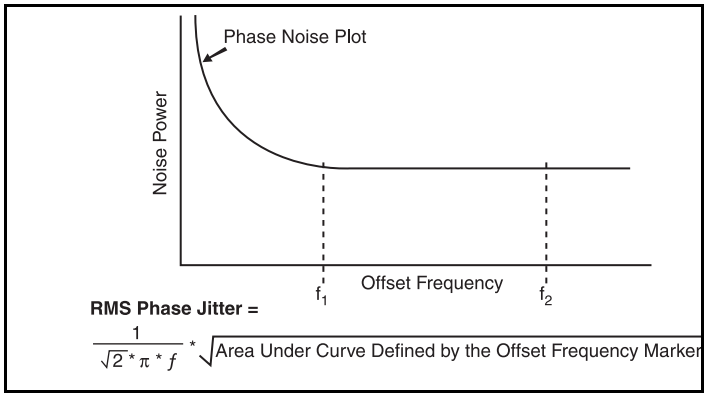
Parameter Measurement Information



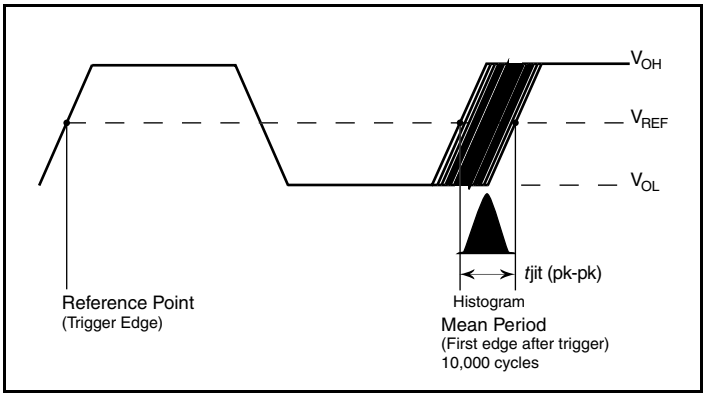
Output Load AC Test Circuit



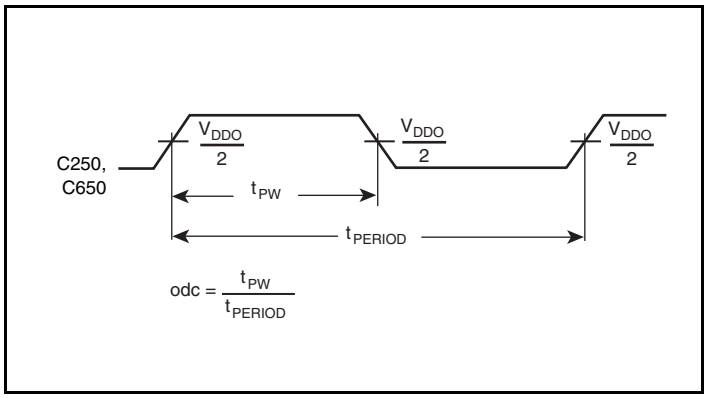
Cycle-to-Cycle Jitter



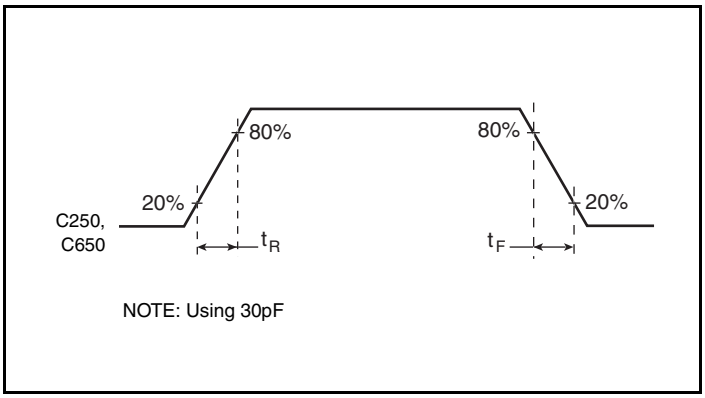
RMS Phase Jitter



Period Jitter Peak-to-Peak

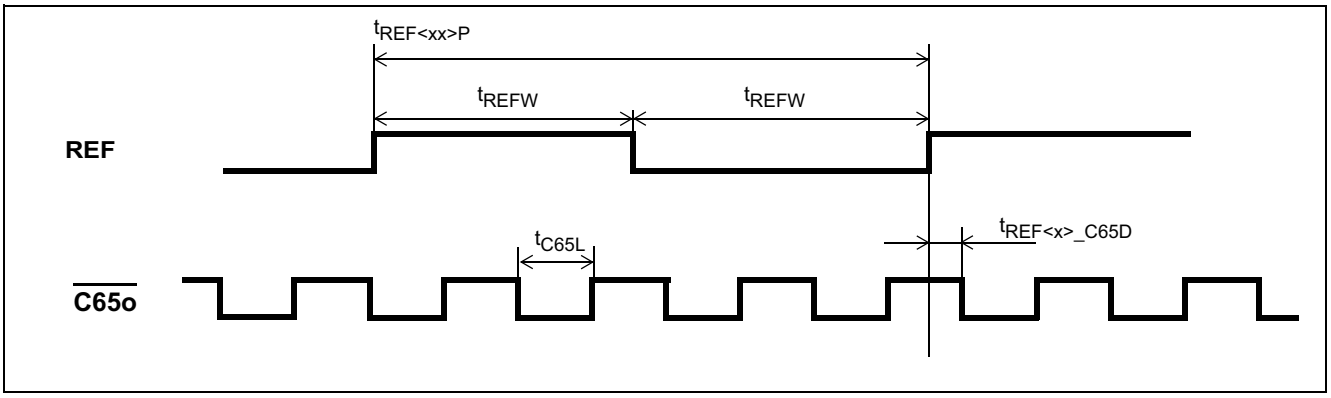


Output Pulse Width



Output Rise/Fall Time

Parameter Measurement Information, continued



Input-to-Output Timing for Synchronous Clock

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 8400110 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

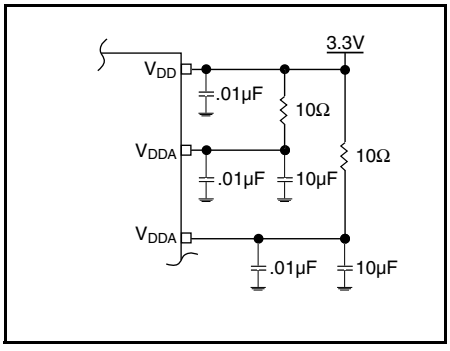


Figure 1. Power Supply Filtering

Crystal Input Interface

The 8400110 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

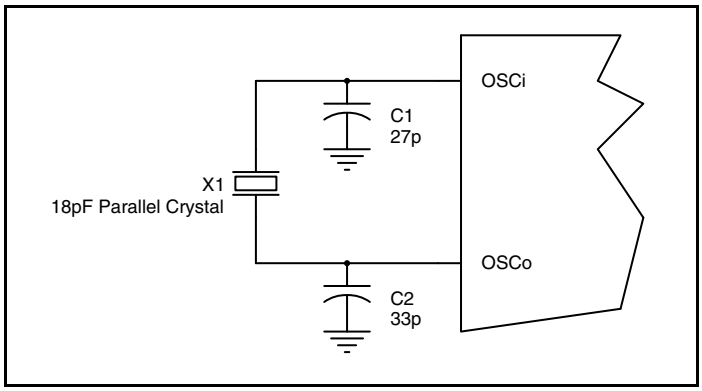


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The OSCi input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The OSCo pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

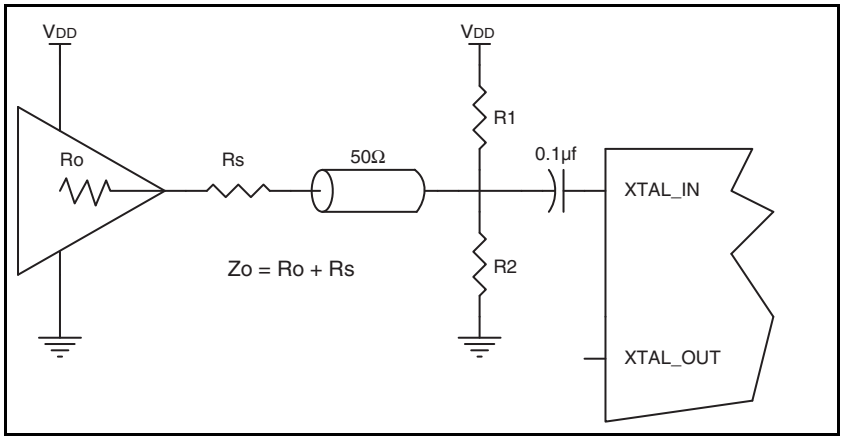


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

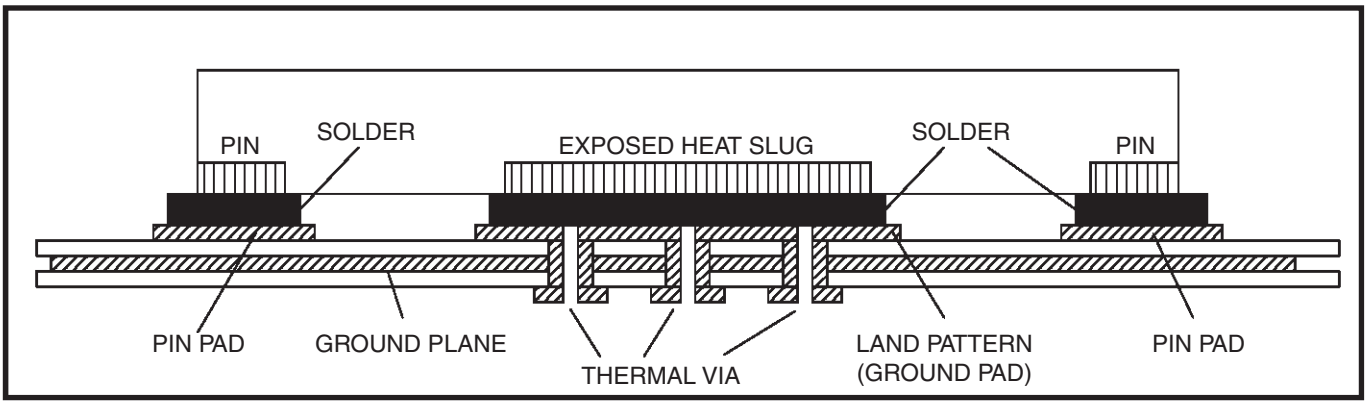


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the 8400110.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8400110 is the sum of the core power plus the analog power plus the power dissipation in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 0.3V = 3.6V, which gives worst case results.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD} + I_{DDA})$ = 3.6V *(130mA + 15mA) = **522mW**
- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to $V_{DD}/2$
  Output Current $I_{OUT} = V_{DD\_MAX} / [2 * (50Ω + R_{OUT})]$ = 3.6V / [2 * (50Ω + 17Ω)] = **26.9mA**
- Power Dissipation on the R_{OUT} per LVCMOS output
  Power $(R_{OUT}) = R_{OUT} * (I_{OUT})^2$ = 17Ω * $(26.9mA)^2$ = **12.3mW per output**
- Total Power Dissipation on the R_{OUT}
  Total Power (R_{OUT}) = 12.3mW * 2 = **24.6mW**

Total Power Dissipation

- **Total Power**
  = Power $(core)_{MAX}$ + Total Power (R_{OUT})
  = 522mW + 24.6mW
  = 546.6mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature for devices is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.547W *37°C/W = 105.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

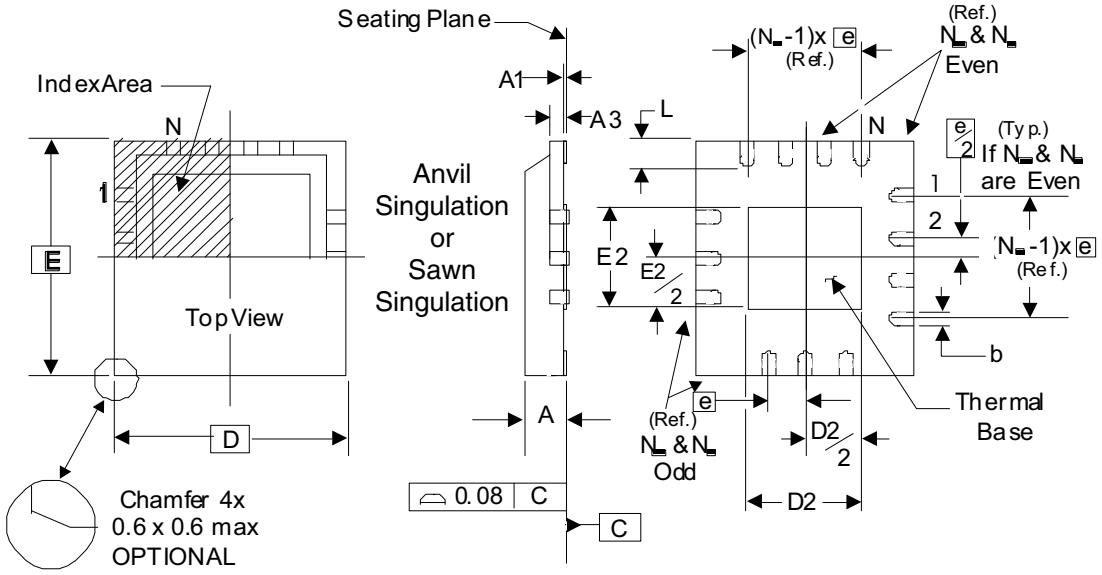
θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

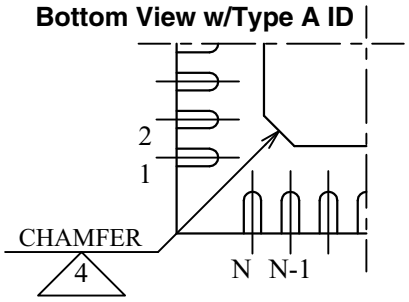
Transistor Count

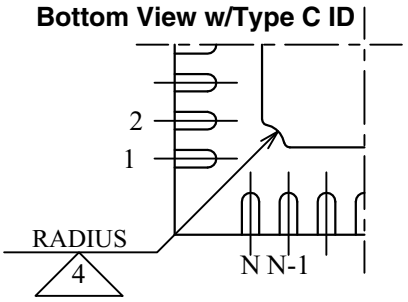
The transistor count for 8400110 is: 4007

Package Outline and Package Dimensions

Package Outline - K Suffix for 32 Lead VFQFN







There are 2 methods of indicating pin 1 corner at the back of the VFQFN package:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

Table 9. Package Dimensions for 32 Lead VFQFN

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A	0.80		1.00
A1	0		0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D & N_E			8
D & E		5.00 Basic	
D2 & E2	3.0		3.3
e		0.50 Basic	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 9.

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8400110EKILF	ICS00110EIL	“Lead-Free” 32 Lead VFQFN	Tray	-40°C to 85°C
8400110EKILFT	ICS00110EIL	“Lead-Free” 32 Lead VFQFN	Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T10	1 13	"General Description" - deleted *HiperClocks* logo. Ordering Information Table - deleted *Tape & Reel count*. Deleted all *HiperClocks* references throughout the datasheet. Deleted *ICS* prefix from part number throughout the datasheet. Updated datasheet header/footer.	1/20/16

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