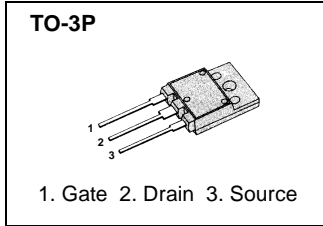


**FEATURES**

- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current: 25µA (Max.) @  $V_{DS} = 900V$
- Lower  $R_{DS(ON)}$ : 1.247Ω (Typ.)

$BV_{DSS} = 900V$   
 $R_{DS(ON)} = 1.8\Omega$   
 $I_D = 5A$



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Characteristics	Value	Units
$V_{DSS}$	Drain-to-Source Voltage	900	V
$I_D$	Continuous Drain Current ( $T_C = 25^\circ C$ )	5	A
	Continuous Drain Current ( $T_C = 100^\circ C$ )	3.2	
$I_{DM}$	Drain Current-Pulsed ①	28	A
$V_{GS}$	Gate-to-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy ②	794	mJ
$I_{AR}$	Avalanche Current ①	5	A
$E_{AR}$	Repetitive Avalanche Energy ①	9.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	1.5	V/ns
$P_D$	Total Power Dissipation ( $T_C = 25^\circ C$ )	95	W
	Linear Derating Factor	0.76	
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 to +150	$^\circ C$
$T_L$	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

**THERMAL RESISTANCE**

Symbol	Characteristics	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	-	1.32	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient	-	40	

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise specified)

Symbol	Characteristics	Min.	Typ.	Max.	Units	Test Conditions
$BV_{DSS}$	Drain-Source Breakdown Voltage	900	–	–	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	–	1.06	–	V/ $^\circ\text{C}$	$I_D=250\mu A$ , <b>See Fig 7</b>
$V_{GS(th)}$	Gate Threshold Voltage	2.0	–	3.5	V	$V_{DS}=5V, I_D=250\mu A$
$I_{GSS}$	Gate-Source Leakage, Forward	–	–	100	nA	$V_{GS}=30V$
	Gate-Source Leakage, Reverse	–	–	–100		$V_{GS}= -30V$
$I_{DSS}$	Drain-to-Source Leakage Current	–	–	25	$\mu A$	$V_{DS}=900V$
		–	–	250		$V_{DS}=720V, T_C=125^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-State Resistance	–	–	1.8	$\Omega$	$V_{GS}=10V, I_D=2.5A$ ④
$g_{fs}$	Forward Transconductance	–	4.72	–	S	$V_{DS}=50V, I_D=2.5A$ ④
$C_{iss}$	Input Capacitance	–	2070	2690	pF	$V_{GS}=0V, V_{DS}=25V$ $f=1\text{MHz}$ <b>See Fig 5</b>
$C_{oss}$	Output Capacitance	–	185	215		
$C_{rss}$	Reverse Transfer Capacitance	–	78	90		
$t_{d(on)}$	Turn-On Delay Time	–	25	60	ns	$V_{DD}=450V, I_D=8A$ $R_G=10\Omega$ <b>See Fig 13</b> ④ ⑤
$t_r$	Rise Time	–	35	85		
$t_{d(off)}$	Turn-Off Delay Time	–	122	255		
$t_f$	Fall Time	–	41	90		
$Q_g$	Total Gate Charge	–	94	123	nC	$V_{DS}=720V, V_{GS}=10V$ $I_D=8A$ <b>See Fig 6 &amp; Fig 12</b> ④ ⑤
$Q_{gs}$	Gate-Source Charge	–	14.9	–		
$Q_{gd}$	Gate-Drain (Miller) Charge	–	43.5	–		

**SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS**

Symbol	Characteristics	Min.	Typ.	Max.	Units	Test Conditions
$I_S$	Continuous Source Current	–	–	5	A	Integral reverse pn-diode in the MOSFET
$I_{SM}$	Pulsed-Source Current ①	–	–	28		
$V_{SD}$	Diode Forward Voltage ④	–	–	1.4	V	$T_J=25^\circ\text{C}, I_S=5A, V_{GS}=0V$
$t_{rr}$	Reverse Recovery Time	–	620	–	ns	$T_J=25^\circ\text{C}, I_F=8A$
$Q_{rr}$	Reverse Recovery Charge	–	9.3	–	$\mu\text{C}$	$di_F/dt=100A/\mu\text{s}$ ④

**Notes:**

- ① Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
- ②  $L=60\text{mH}, I_{AS}=5A, V_{DD}=50V, R_G=27\Omega$ , Starting  $T_J=25^\circ\text{C}$
- ③  $I_{SD} \leq 8A, di/dt \leq 170A/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J=25^\circ\text{C}$
- ④ Pulse Test: Pulse Width  $\leq 250\mu\text{s}$ , Duty Cycle  $\leq 2\%$
- ⑤ Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

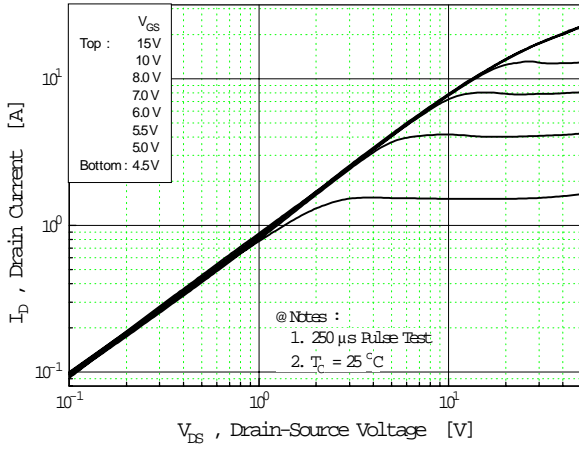


Fig 2. Transfer Characteristics

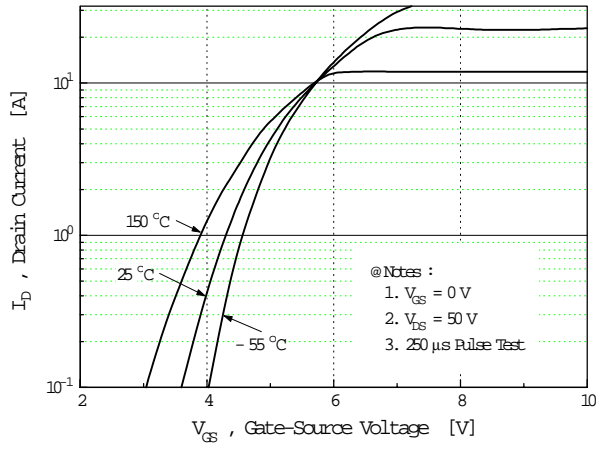


Fig 3. On-Resistance vs. Drain Current

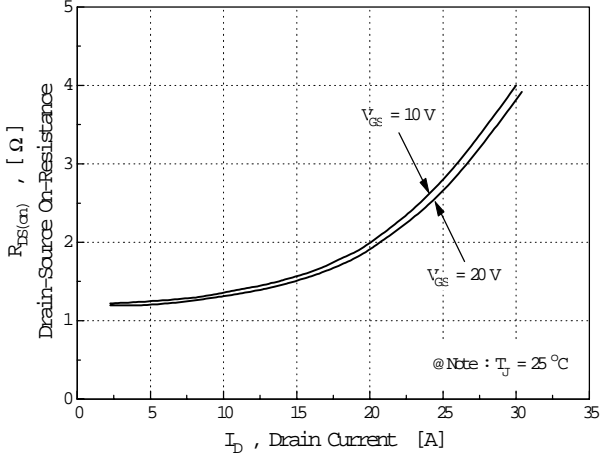


Fig 4. Source-Drain Diode Forward Voltage

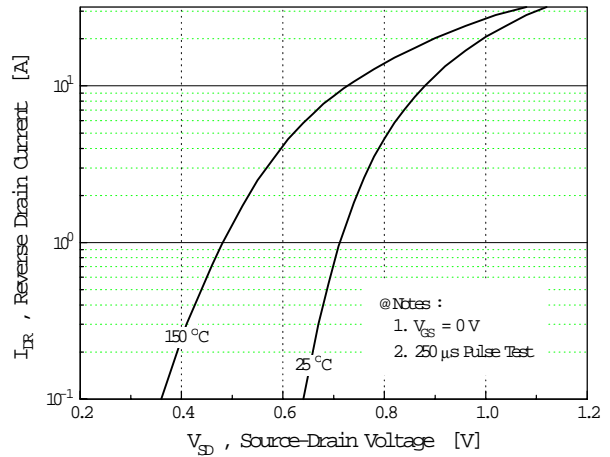


Fig 5. Capacitance vs. Drain-Source Voltage

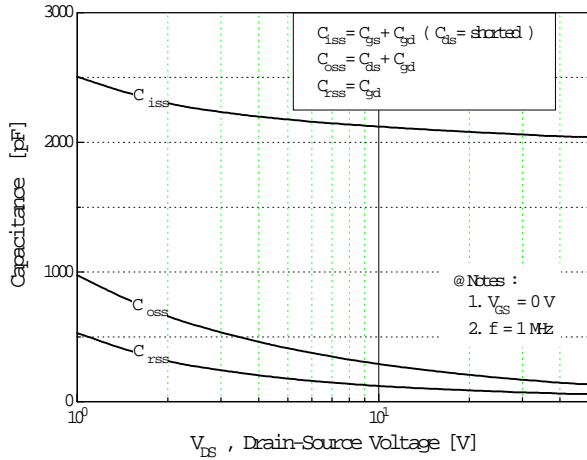


Fig 6. Gate Charge vs. Gate-Source Voltage

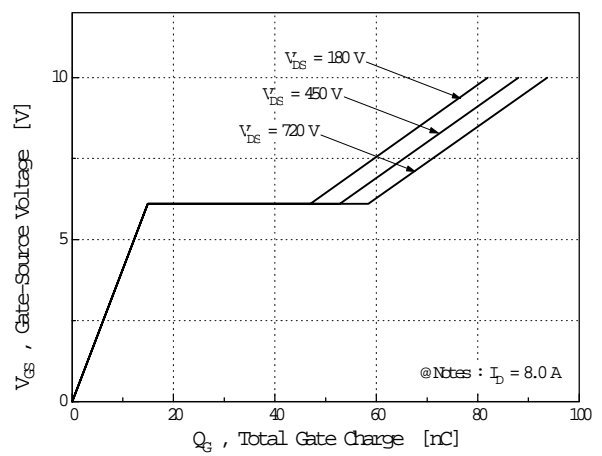


Fig 7. Breakdown Voltage vs. Temperature

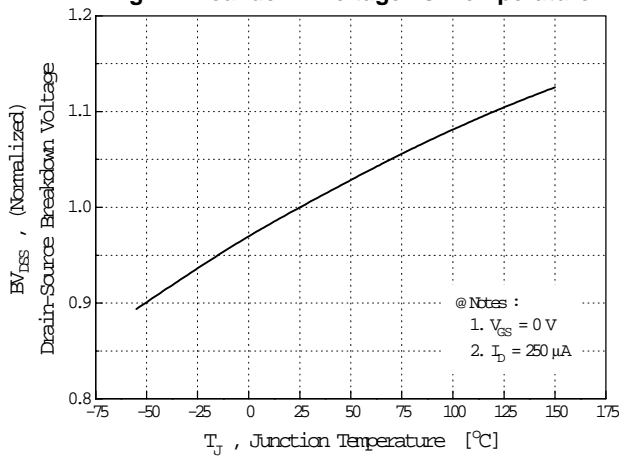


Fig 8. On-Resistance vs. Temperature

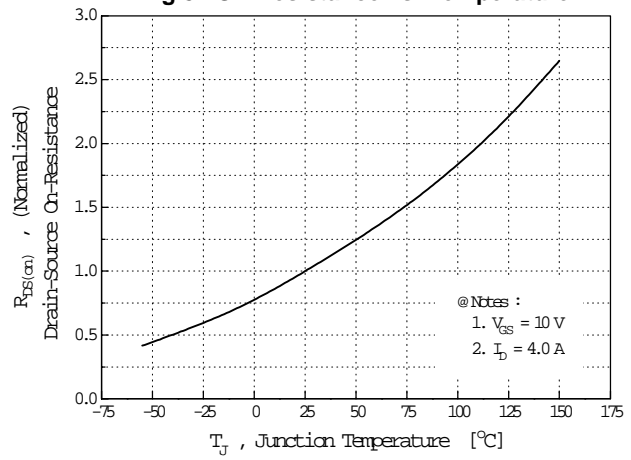


Fig 9. Max. Safe Operating Area

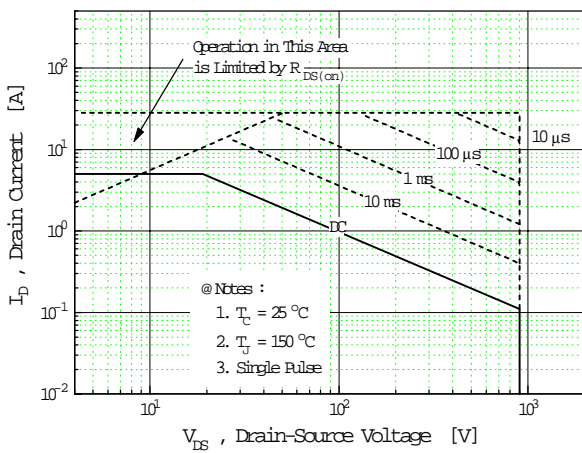


Fig 10. Max. Drain Current vs. Case Temperature

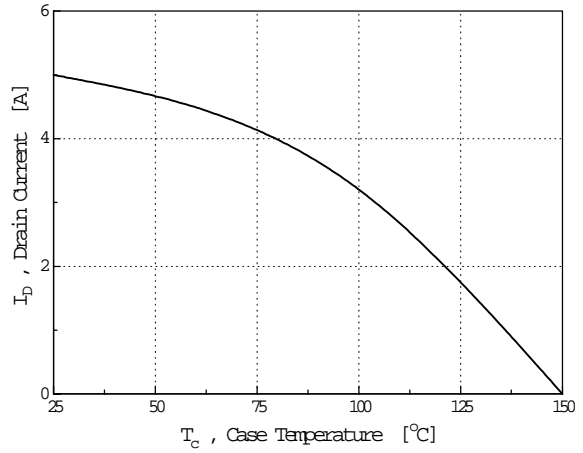


Fig 11. Thermal Response

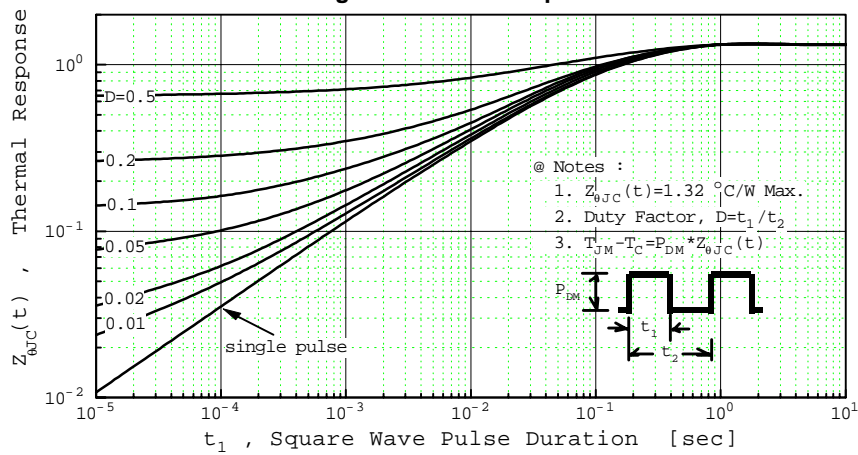


Fig 12. Gate Charge Test Circuit & Waveform

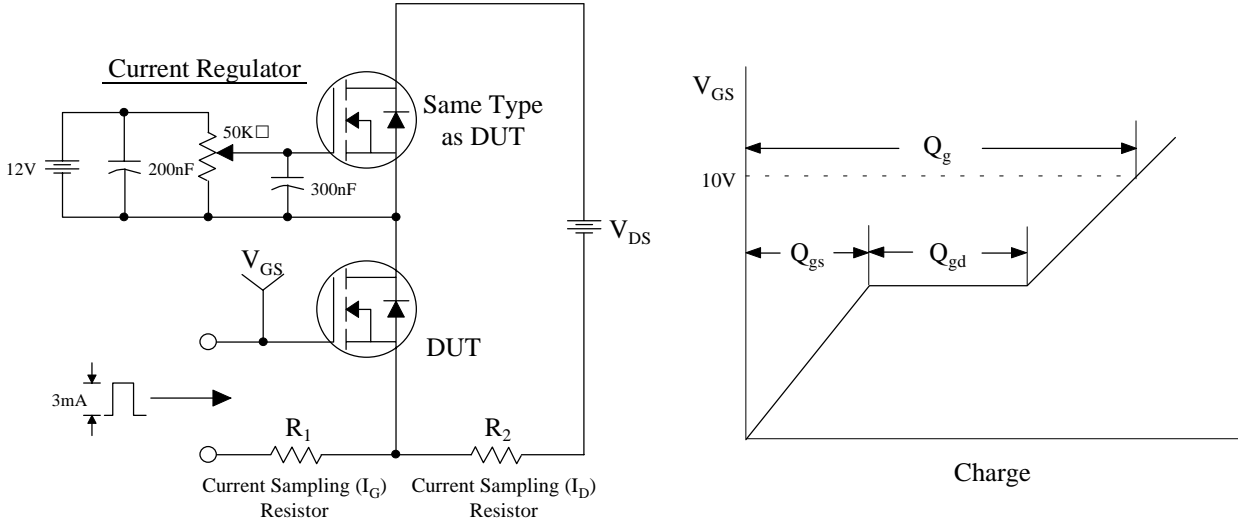


Fig 13. Resistive Switching Test Circuit & Waveforms

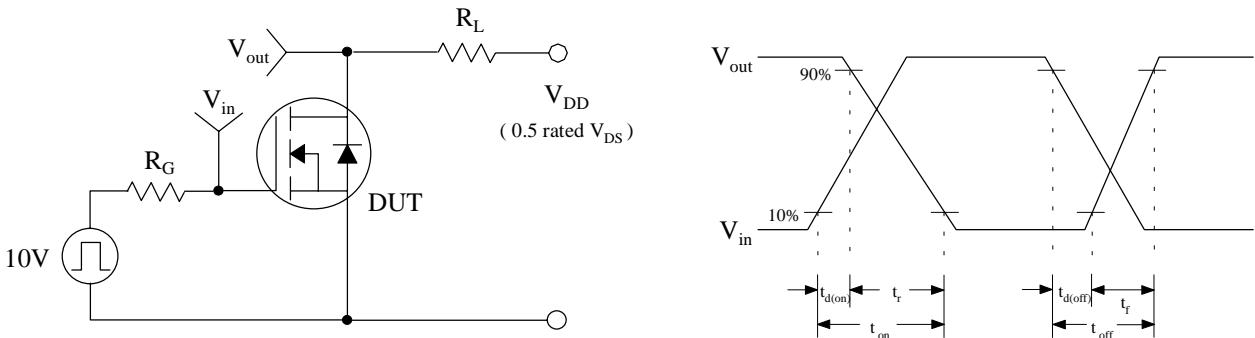


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

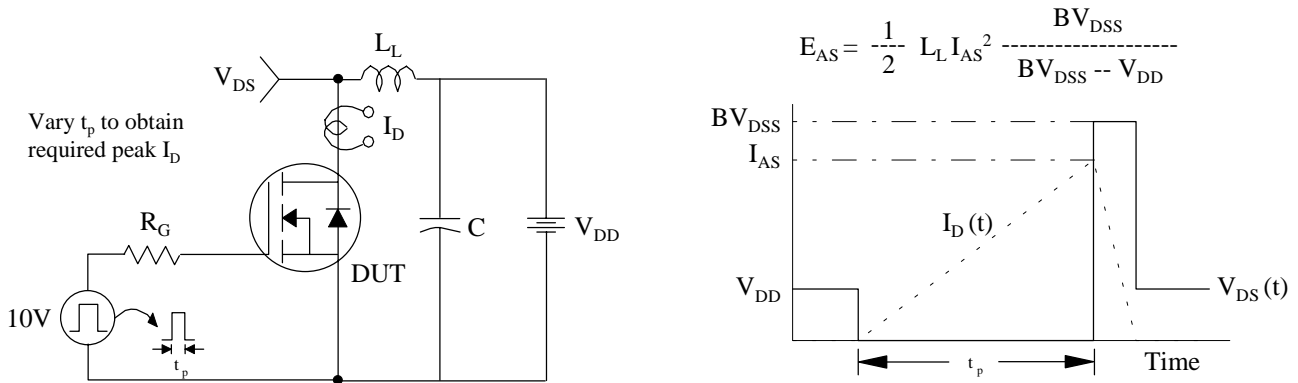
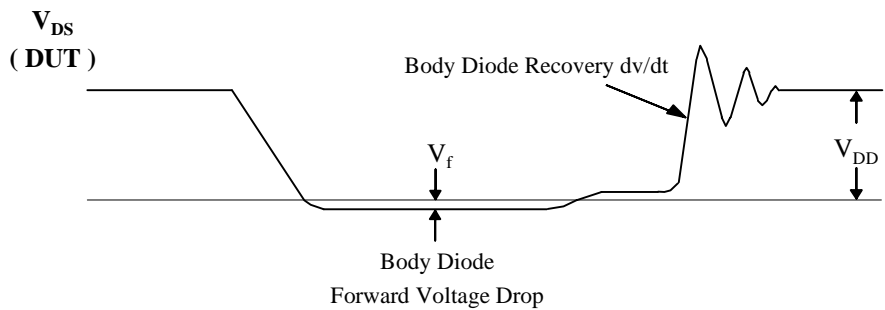
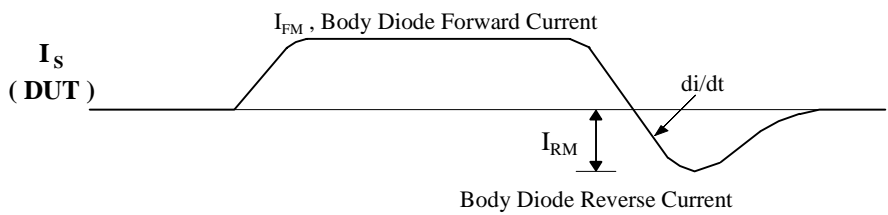
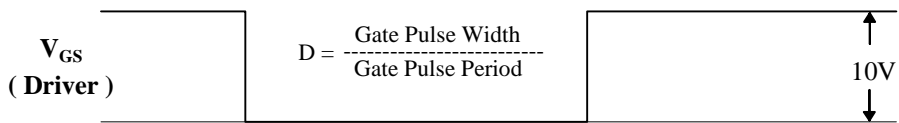
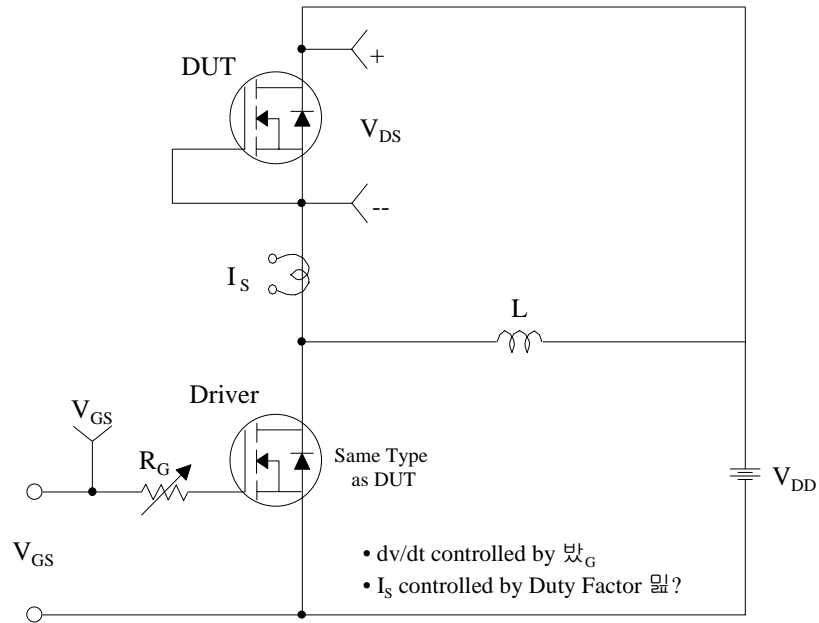


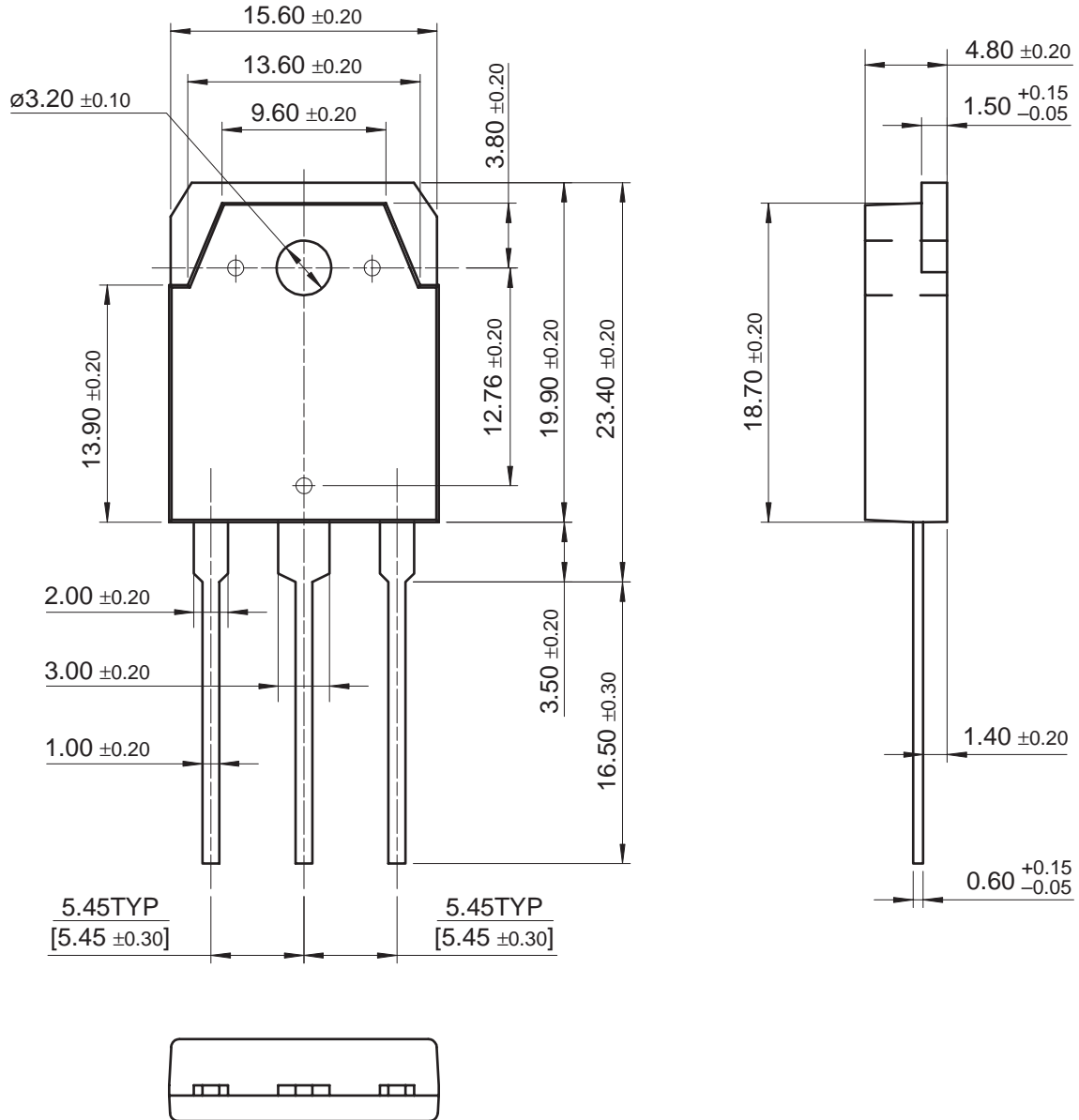
Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



# TO-3P Package Dimensions



## TO-3P (FS PKG CODE AF)



Dimensions in Millimeters

August 1999, Rev B

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HiSeC™	SuperSOT™-8	

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