SOJ, TSOP, FP-BGA
Commercial Temp
Industrial Temp

128K x 8
1Mb Asynchronous SRAM

10, 12, 15ns
3.3V V_{DD}
Center V_{DD} & V_{SS}

Features

- Fast access time: 10, 12, 15ns
- CMOS low power operation: 90/85/70 mA at min. cycle time.
- Single 3.3V ± 0.3V power supply
- All inputs and outputs are TTL compatible
- Fully static operation
- Industrial Temperature Option: -40° to 85°C
- Package line up
  - J: 400mil, 32 pin SOJ package
  - TP: 400mil, 32 pin TSOP Type II package
  - SJ: 300 mil, 32 pin SOJ package
  - U: 6 mm x 8 mm Fine Pitch Ball Grid Array package

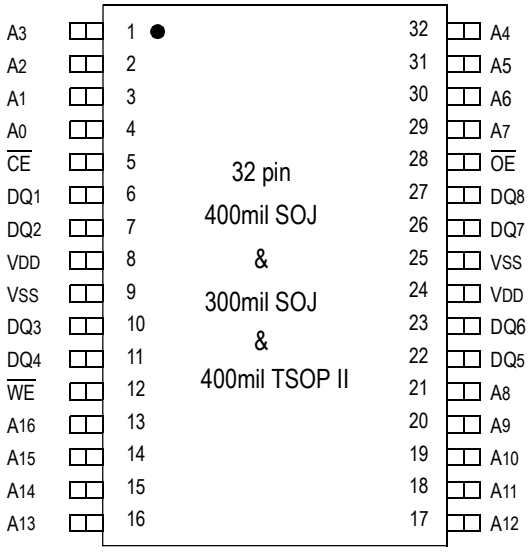
Description

The GS71108 is a high speed CMOS static RAM organized as 131,072-words by 8-bits. Static design eliminates the need for external clocks or timing strobes. Operating on a single 3.3V power supply and all inputs and outputs are TTL compatible. The GS71108 is available in a 6x8 mm Fine Pitch BGA package as well as in 300mil and 400 mil SOJ and 400 mil TSOP Type-II packages.

Pin Descriptions

Symbol	Description
A_0 to A_{16}	Address input
DQ_1 to DQ_8	Data input/output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
V_{DD}	+3.3V power supply
V_{SS}	Ground
NC	No connect

SOJ & TSOP-II 128K x 8 Pin Configuration

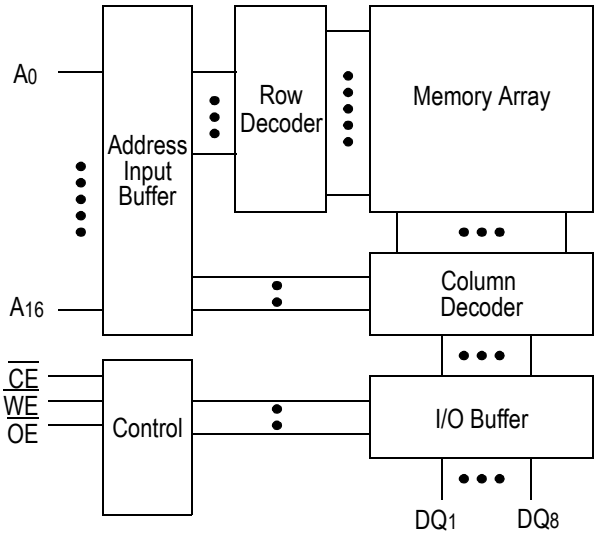


Fine Pitch BGA 128K x 8 Bump Configuration

	1	2	3	4	5	6
A	NC	$\overline{OE}$	A_2	A_6	A_7	NC
B	DQ_1	NC	A_1	A_5	$\overline{CE}$	DQ_8
C	DQ_2	NC	A_0	A_4	NC	DQ_7
D	V_{SS}	NC	NC	A_3	NC	V_{DD}
E	V_{DD}	NC	NC	NC	NC	V_{SS}
F	DQ_3	NC	A_{14}	A_{11}	DQ_5	DQ_6
G	DQ_4	NC	A_{15}	A_{12}	$\overline{WE}$	A_8
H	NC	A_{10}	A_{16}	A_{13}	A_9	NC

6mm x 8mm, 0.75mm Bump Pitch
Top View

Block Diagram



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ1 to DQ8	VDD Current
H	X	X	Not Selected	ISB1, ISB2
L	L	H	Read	IDD
L	X	L	Write	
L	H	H	High Z	

Note: X: "H" or "L"

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	VDD	-0.5 to +4.6	V
Input Voltage	VIN	-0.5 to VDD+0.5 (≤ 4.6V max.)	V
Output Voltage	VOUT	-0.5 to VDD+0.5 (≤ 4.6V max.)	V
Allowable power dissipation	PD	0.7	W
Storage temperature	TSTG	-55 to 150	°C

Note:
Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended

Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage for -/12/15	V_{DD}	3.0	3.3	3.6	V
Supply Voltage for -10	V_{DD}	3.135	3.3	3.6	V
Input High Voltage	V_{IH}	2.0	-	V_{DD}+0.3	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Ambient Temperature, Commercial Range	T_{Ac}	0	-	70	°C
Ambient Temperature, Industrial Range	T_{AI}	-40	-	85	°C

Note:
1. Input overshoot voltage should be less than V_{DD}+2V and not exceed 20ns.
2. Input undershoot voltage should be greater than -2V and not exceed 20ns.

Capacitance

Parameter	Symbol	Test Condition	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	7	pF

Notes:
1. Tested at T_A=25°C, f=1MHz
2. These parameters are sampled and are not 100% tested

DC I/O Pin Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current	I_{IL}	V_{IN} = 0 to V_{DD}	-1uA	1uA
Output Leakage Current	I_{LO}	Output High Z V_{OUT} = 0 to V_{DD}	-1uA	1uA
Output High Voltage	V_{OH}	I_{OH} = - 4mA	2.4	
Output Low Voltage	V_{OL}	I_{LO} = + 4mA		0.4V

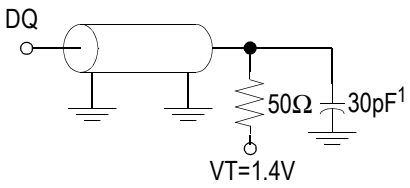
Power Supply Currents

Parameter	Symbol	Test Conditions	0 to 70°C			-40 to 85°C		
			10ns	12ns	15ns	10ns	12ns	15ns
Operating Supply Current	I_{DD}	$\overline{CE} \leq V_{IL}$ All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Min. cycle time I_{OUT} = 0 mA	90mA	85mA	70mA	115mA	100mA	85mA
Standby Current	I_{SB1}	$\overline{CE} \geq V_{IH}$ All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Min. cycle time	45mA	40mA	35mA	50mA	45mA	40mA
Standby Current	I_{SB2}	$CE \geq V_{DD}$ - 0.2V All other inputs $\geq V_{DD}$ - 0.2V or $\leq$ 0.2V	10mA			15mA		

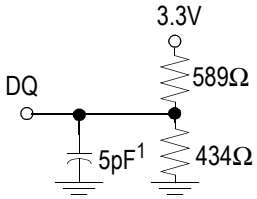
AC Test Conditions

Parameter	Conditions
Input high level	V_{IH}=2.4V
Input low level	V_{IL}=0.4V
Input rise time	tr=1V/ns
Input fall time	tf=1V/ns
Input reference level	1.4V
Output reference level	1.4V
Output load	Fig. 1& 2

Output Load 1



Output Load 2



Note:
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted
3. Output load 2 for t_{LZ}, t_{HZ}, t_{OLZ} and t_{OHZ}.

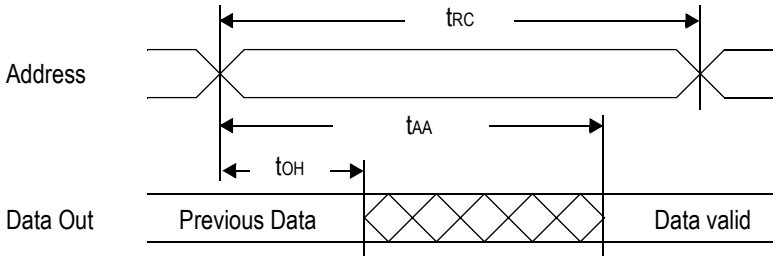
AC Characteristics

Read Cycle

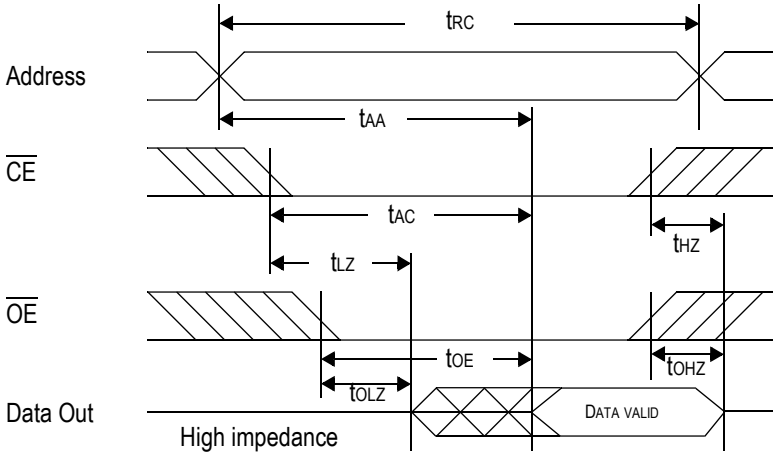
Parameter	Symbol	-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	10	---	12	---	15	---	ns
Address access time	t_{AA}	---	10	---	12	---	15	ns
Chip enable access time ($\overline{CE}$)	t_{AC}	---	10	---	12	---	15	ns
Output enable to output valid ($\overline{OE}$)	t_{OE}	---	4	---	5	---	6	ns
Output hold from address change	t_{OH}	3	---	3	---	3	---	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	3	---	3	---	3	---	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	0	---	0	---	0	---	ns
Chip disable to output in High Z ($\overline{CE}$)	t_{HZ}*	---	5	---	6	---	7	ns
Output disable to output in High Z ($\overline{OE}$)	t_{OHZ}*	---	4	---	5	---	6	ns

* These parameters are sampled and are not 100% tested

Read Cycle 1: $\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}



Read Cycle 2: $\overline{WE}$ = V_{IH}

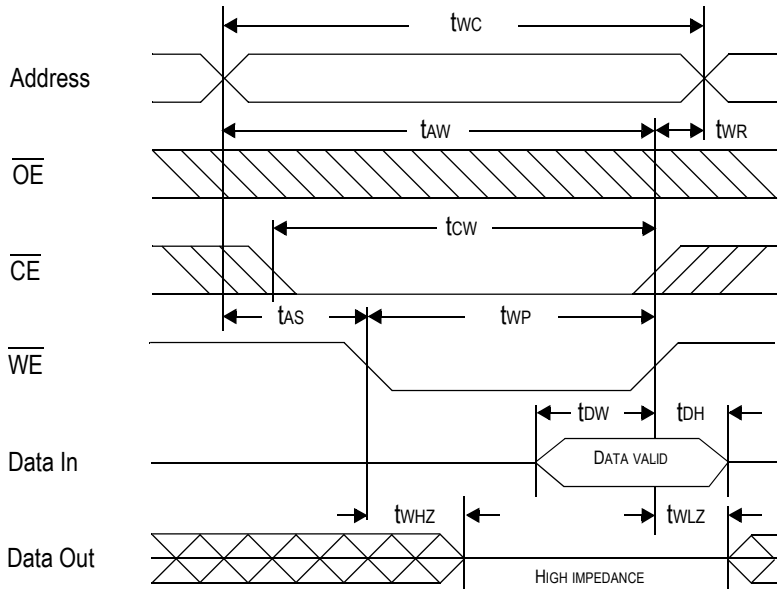


Write Cycle

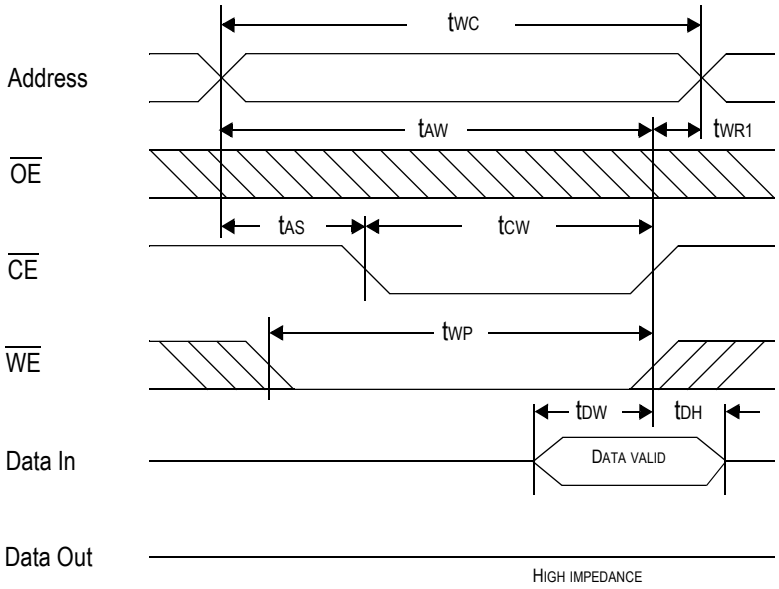
Parameter	Symbol	-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	tWC	10	---	12	---	15	---	ns
Address valid to end of write	tAW	7	---	8	---	10	---	ns
Chip enable to end of write	tCW	7	---	8	---	10	---	ns
Data set up time	tDW	5	---	6	---	7	---	ns
Data hold time	tDH	0	---	0	---	0	---	ns
Write pulse width	tWP	7	---	8	---	10	---	ns
Address set up time	tAS	0	---	0	---	0	---	ns
Write recovery time ($\overline{WE}$)	tWR	0	---	0	---	0	---	ns
Write recovery time ($\overline{CE}$)	tWR1	0	---	0	---	0	---	ns
Output Low Z from end of write	tWLZ*	3	---	3	---	3	---	ns
Write to output in High Z	tWHZ*	---	4	---	5	---	6	ns

* These parameters are sampled and are not 100% tested

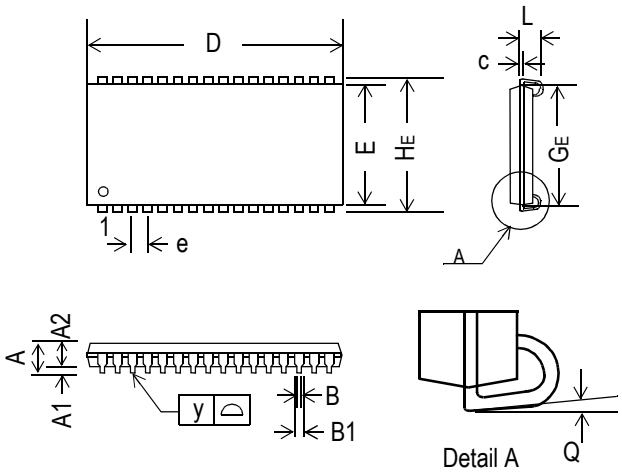
Write Cycle 1: $\overline{WE}$ control



Write Cycle 2: $\overline{CE}$ control



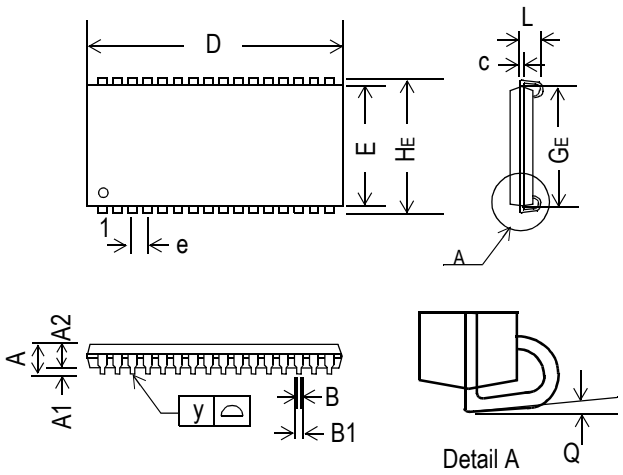
32 Pin SOJ, 300 mil



Symbol	Dimension in inch			Dimension in mm		
	min	nom	max	min	nom	max
A	0.125	-	0.148	3.175	-	3.76
A1	0.026	-	-	0.66	-	-
A2	0.095	0.100	0.105	2.41	2.54	2.67
B	0.013	0.017	0.021	0.33	0.43	0.53
B1	0.024	0.028	0.032	0.61	0.71	0.81
c	0.006	0.008	0.012	0.15	0.20	0.30
D	0.820	0.825	0.830	20.82	20.95	21.08
E	0.295	0.300	0.305	7.49	7.62	7.75
e	-	0.05	-	-	1.27	-
HE	0.330	0.335	0.340	8.38	8.51	8.64
GE	0.255	0.267	0.275	6.48	6.78	6.985
L	0.082	-	-	2.08	-	-
y	-	-	0.004	-	-	0.10
Q	0^o	-	10^o	0^o	-	10^o

Note:
1. Dimension D& E do not include interlead flash
2. Dimension B1 does not include dambar protrusion / intrusion
3. Controlling dimension: inches

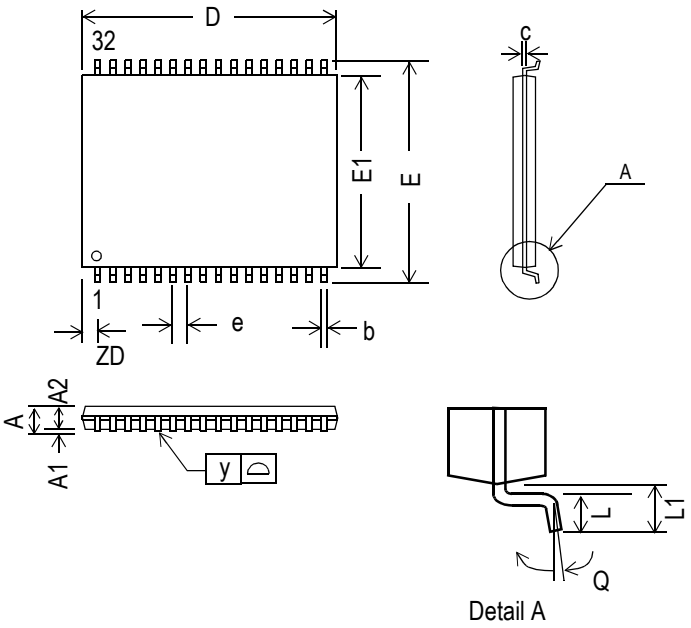
32 Pin SOJ, 400 mil



Symbol	Dimension in inch			Dimension in mm		
	min	nom	max	min	nom	max
A	-	-	0.146	-	-	3.70
A1	0.026	-	-	0.66	-	-
A2	0.105	0.110	0.115	2.67	2.80	2.92
B	0.013	0.017	0.021	0.33	0.43	0.53
B1	0.024	0.028	0.032	0.61	0.71	0.81
c	0.006	0.008	0.012	0.15	0.20	0.30
D	0.820	0.824	0.829	20.83	20.93	21.06
E	0.395	0.400	0.405	10.04	10.16	10.28
e	-	0.05	-	-	1.27	-
HE	0.430	0.435	0.440	10.93	11.05	11.17
GE	0.354	0.366	0.378	9.00	9.30	9.60
L	0.082	-	-	2.08	-	-
y	-	-	0.004	-	-	0.10
Q	0^o	-	10^o	0^o	-	10^o

Note:
1. Dimension D& E do not include interlead flash
2. Dimension B1 does not include dambar protrusion / intrusion
3. Controlling dimension: inches

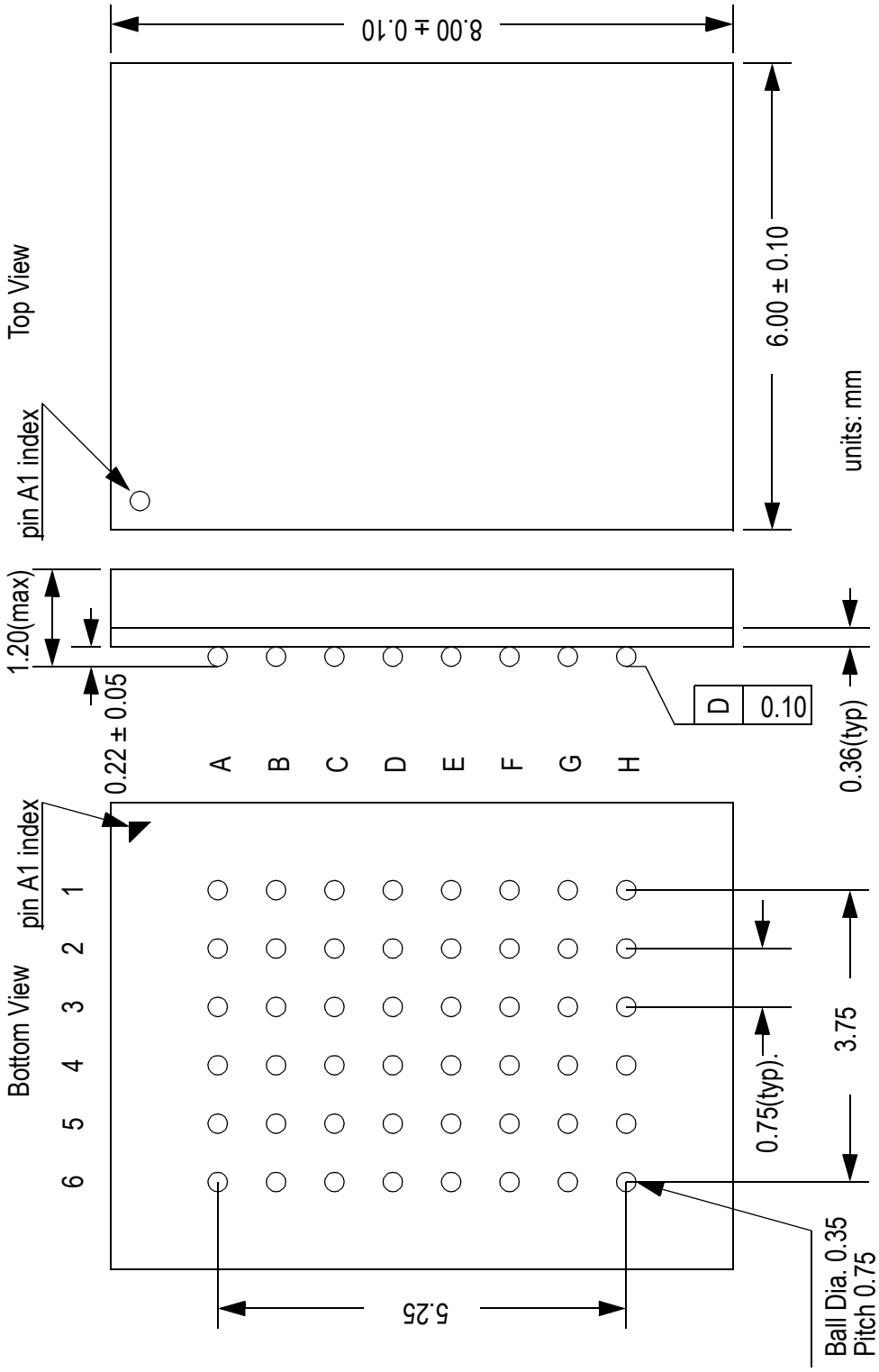
32 Pin TSOP-II, 400mil



Symbol	Dimension in inch			Dimension in mm		
	min	nom	max	min	nom	max
A	0.039	-	0.05	-	-	1.27
A1	0.002	-	0.006	0.01	-	0.15
A2	0.037	0.040	0.045	0.90	1.02	1.14
b	0.012	0.016	0.018	0.30	0.40	0.45
c	0.0047	0.0051	0.0062	0.12	0.13	0.16
D	0.820	0.825	0.830	20.82	20.95	21.08
ZD	-	0.037	-	-	0.95	-
E	0.455	0.463	0.471	11.56	11.76	11.96
E1	0.395	0.400	0.405	10.03	10.16	10.29
e	-	0.05	-	-	1.27	-
L	0.017	0.020	0.023	0.40	0.50	0.60
L1	0.024	0.031	0.039	0.60	0.80	1.00
y	0.00	-	0.003	0.00	-	0.76
Q	0^o	-	5^o	0^o	-	5^o

Note:
1.Dimension D includes mold flash, protrusions or gate burrs.
2. Dimension E does not include interlead flash
3. Controlling dimension: mm

6mm x 8mm Fine Pitch BGA



Ordering Information

Part Number*	Package	Access Time	Temp. Range	Status
GS71108TP-10	400 mil TSOP-II	10 ns	Commercial	
GS71108TP-12	400 mil TSOP-II	12 ns	Commercial	
GS71108TP-15	400 mil TSOP-II	15 ns	Commercial	
GS71108TP-10I	400 mil TSOP-II	10 ns	Industrial	
GS71108TP-12I	400 mil TSOP-II	12 ns	Industrial	
GS71108TP-15I	400 mil TSOP-II	15 ns	Industrial	
GS71108SJ-10	300 mil SOJ	10 ns	Commercial	
GS71108SJ-12	300 mil SOJ	12 ns	Commercial	
GS71108SJ-15	300 mil SOJ	15 ns	Commercial	
GS71108SJ-10I	300 mil SOJ	10 ns	Industrial	
GS71108SJ-12I	300 mil SOJ	12 ns	Industrial	
GS71108SJ-15I	300 mil SOJ	15 ns	Industrial	
GS71108J-10	400 mil SOJ	10 ns	Commercial	
GS71108J-12	400 mil SOJ	12 ns	Commercial	
GS71108J-15	400 mil SOJ	15 ns	Commercial	
GS71108J-10I	400 mil SOJ	10 ns	Industrial	
GS71108J-12I	400 mil SOJ	12 ns	Industrial	
GS71108J-15I	400 mil SOJ	15 ns	Industrial	
GS71108U-10	Fine Pitch BGA	10 ns	Commercial	
GS71108U-12	Fine Pitch BGA	12 ns	Commercial	
GS71108U-15	Fine Pitch BGA	15 ns	Commercial	
GS71108U-10I	Fine Pitch BGA	10 ns	Industrial	
GS71108U-12I	Fine Pitch BGA	12 ns	Industrial	
GS71108U-15I	Fine Pitch BGA	15 ns	Industrial	

* Customers requiring delivery in Tape and Reel should add the character “T” to the end of the part number. For example: GS71108TP-10T

Revision History

Rev. Code: Old; New	Types of Changes Format or Content	Page #/Revisions/Reason
GS71108Rev2.01KRev 21 2/2000L	Format/Content	1. GSI Logo 2. Added Dimension D to 32 pin 400 ml TSOP II Package.
GS 71108 Rev 2.01 2/ 2000;Rev2.03 2/2000M	Content	1. Took all referenced to 8ns and 9ns speed bins out. 2. Heading, Power Supply Currents, Read and Writ eCycle table, Ordering information.

