

# P100FA7R5EN

## Power MOSFETs

75V, 100A, N-channel

### Feature

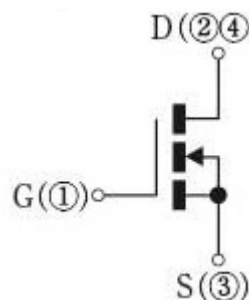
- N-channel
- Large Current
- Low Ron
- 10V Gate Drive
- Low Capacitance
- Pb free terminal
- RoHS:Yes

### OUTLINE

Package (House Name): FA  
 Package (JEDEC Code): TO-220AB  
 Package (JEITA Code): SC-46



### Equivalent circuit



### Absolute Maximum Ratings (unless otherwise specified : Tc=25°C)

Item	Symbol	Conditions	Ratings	Unit
Storage temperature	Tstg		-55 to 150	°C
Channel temperature	Tch		150	°C
Drain-source voltage	V <sub>DSS</sub>		75	V
Gate-source voltage	V <sub>GSS</sub>		±20	V
Continuous drain current(DC)	I <sub>D</sub>		100	A
Continuous drain current(Peak)	I <sub>DP</sub>	Pulse width 10μs, duty=1/100	400	A
Total power dissipation	P <sub>T</sub>		140	W
Single avalanche current	I <sub>AS</sub>	Starting T <sub>ch</sub> =25°C T <sub>ch</sub> ≤150°C	57	A
Single avalanche energy	E <sub>AS</sub>	Starting T <sub>ch</sub> =25°C T <sub>ch</sub> ≤150°C	300	mJ

\* : See the original Specifications

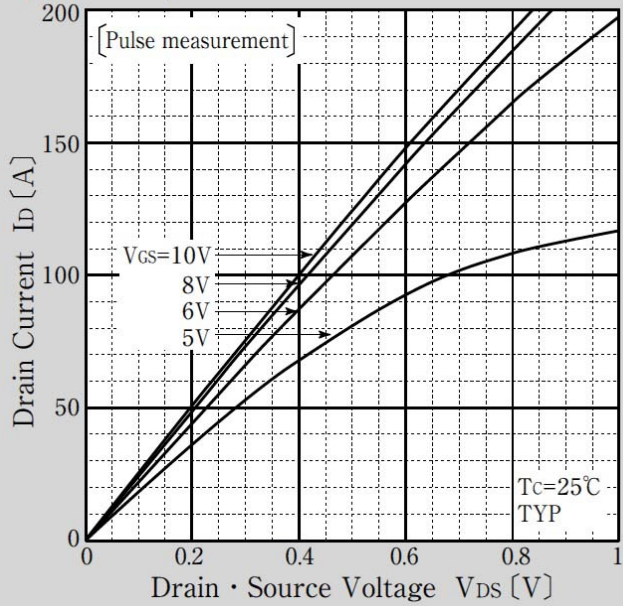
**Electrical Characteristics** (unless otherwise specified : Tc=25°C)

Item	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Drain-Source breakdown voltage	$V_{(BR)DSS}$	ID=1mA, VGS=0V	75			V
Zero gate voltage drain current	$I_{DSS}$	VDS=75V, VGS=0V			1	$\mu$ A
Gate-source leakage current	$I_{GSS}$	VGS= $\pm$ 20V, VDS=0V			$\pm$ 0.1	$\mu$ A
Forward transconductance	$g_{fs}$	ID=50A, VDS=10V	31			S
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=50A, VGS=10V		0.0042	0.005	$\Omega$
Gate threshold voltage	$V_{th}$	ID=1mA, VDS=10V	2	3	4	V
Source-drain diode forward voltage	$V_{SD}$	IS=100A, VGS=0V			1.5	V
Thermal resistance	$R_{th(j-c)}$	Junction to case			0.89	$^{\circ}$ C/W
Total gate charge	$Q_g$	VDD=60V, VGS=10V, ID=100A		104		nC
Gate to source charge	$Q_{gs}$	VDD=60V, VGS=10V, ID=100A		26		nC
Gate to drain charge	$Q_{gd}$	VDD=60V, VGS=10V, ID=100A		36		nC
Input capacitance	$C_{iss}$	VDS=25V, VGS=0V, f=1MHz		5720		pF
Reverse transfer capacitance	$C_{rss}$	VDS=25V, VGS=0V, f=1MHz		345		pF
Output capacitance	$C_{oss}$	VDS=25V, VGS=0V, f=1MHz		745		pF
Turn-on delay time	$t_{d(on)}$	ID=50A, RL=0.75 $\Omega$ , VDD=37.5V, Rg=0 $\Omega$ , VGS(+)=10V, VGS(-)=0V		12		ns
Rise time	$t_r$	ID=50A, RL=0.75 $\Omega$ , VDD=37.5V, Rg=0 $\Omega$ , VGS(+)=10V, VGS(-)=0V		46		ns
Turn-off delay time	$t_{d(off)}$	ID=50A, RL=0.75 $\Omega$ , VDD=37.5V, Rg=0 $\Omega$ , VGS(+)=10V, VGS(-)=0V		53		ns
Fall time	$t_f$	ID=50A, RL=0.75 $\Omega$ , VDD=37.5V, Rg=0 $\Omega$ , VGS(+)=10V, VGS(-)=0V		55		ns
Diode reverse recovery time	$t_{rr}$	IF=100A, VGS=0V, di/dt=100A/ $\mu$ s		55		ns
Diode reverse recovery charge	$Q_{rr}$	IF=100A, VGS=0V, di/dt=100A/ $\mu$ s		106		nC

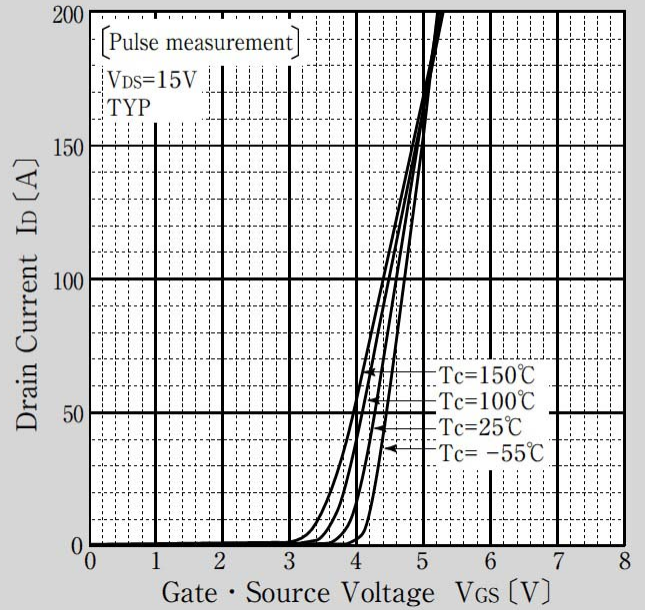
※ : See the original Specifications

# CHARACTERISTIC DIAGRAMS

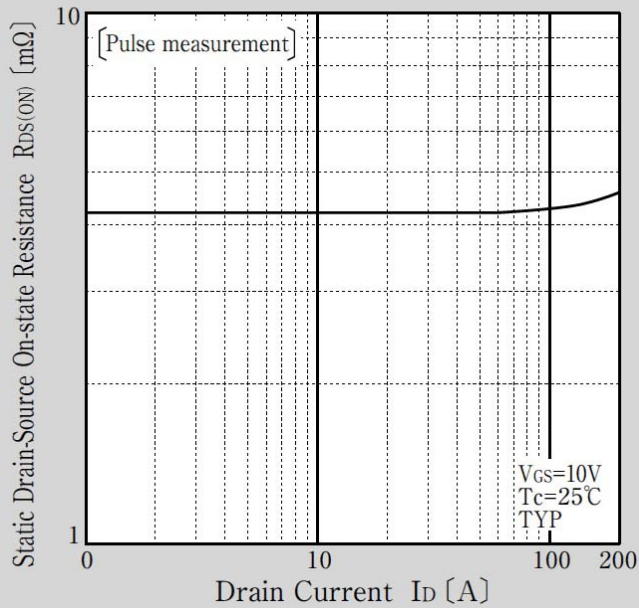
### Typical Output Characteristics



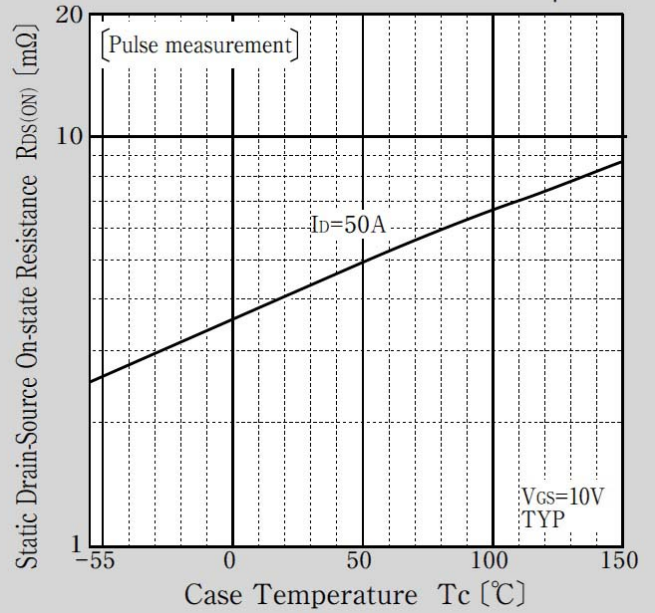
### Transfer Characteristics



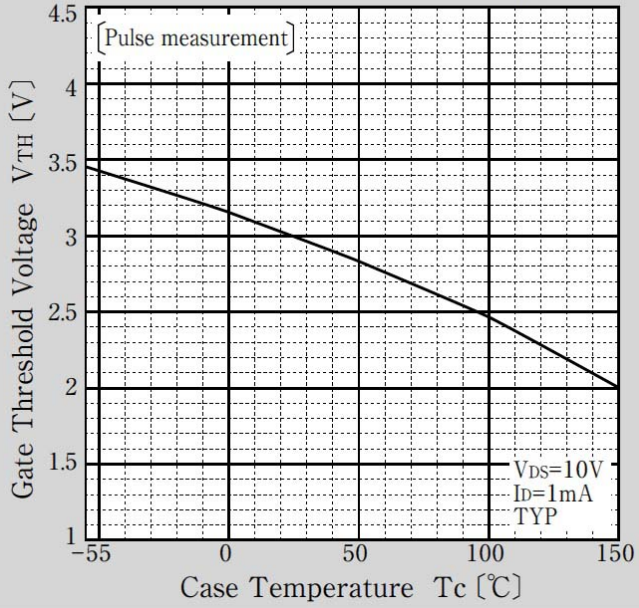
### Static Drain-Source On-state Resistance vs Drain Current



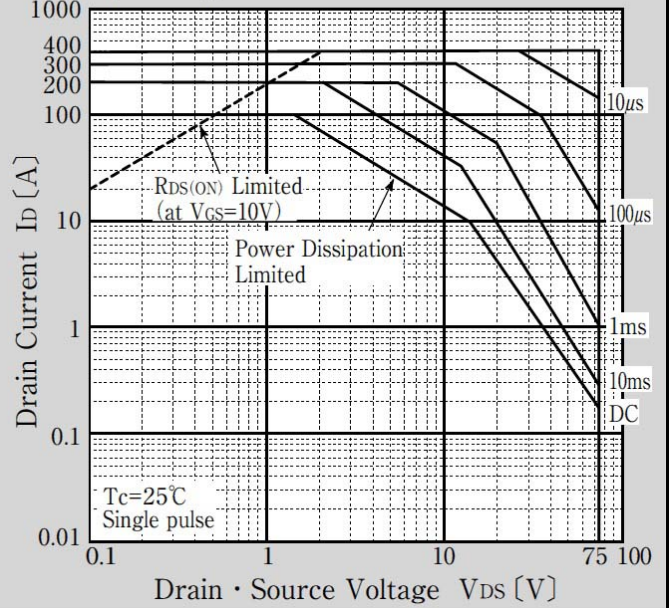
### Static Drain-Source On-state Resistance vs Case Temperature



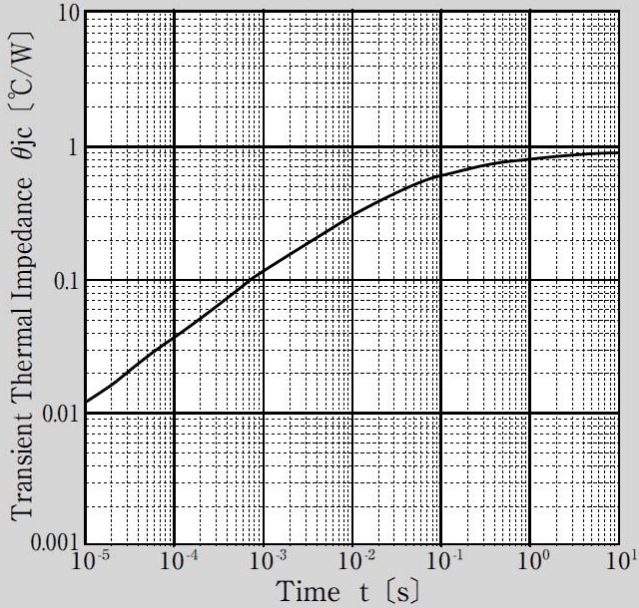
Gate Threshold Voltage vs Case Temperature



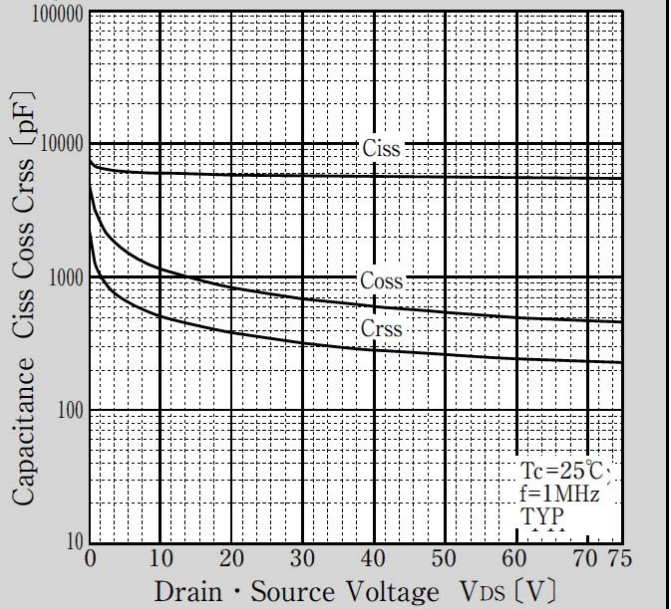
Safe Operating Area



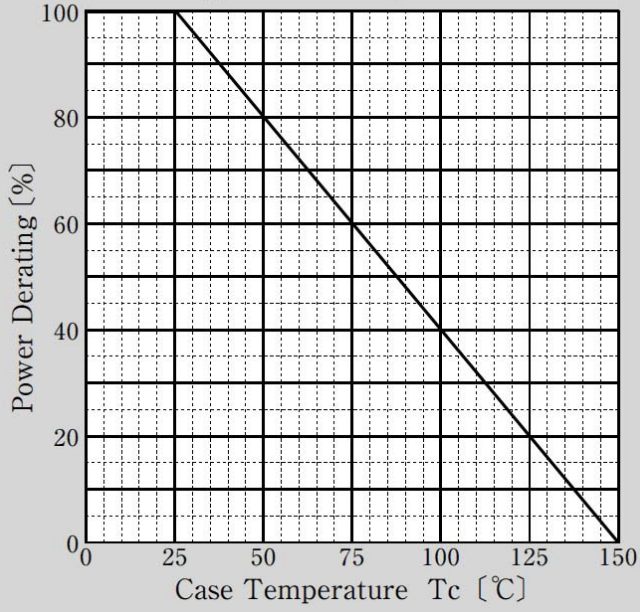
Transient Thermal Impedance



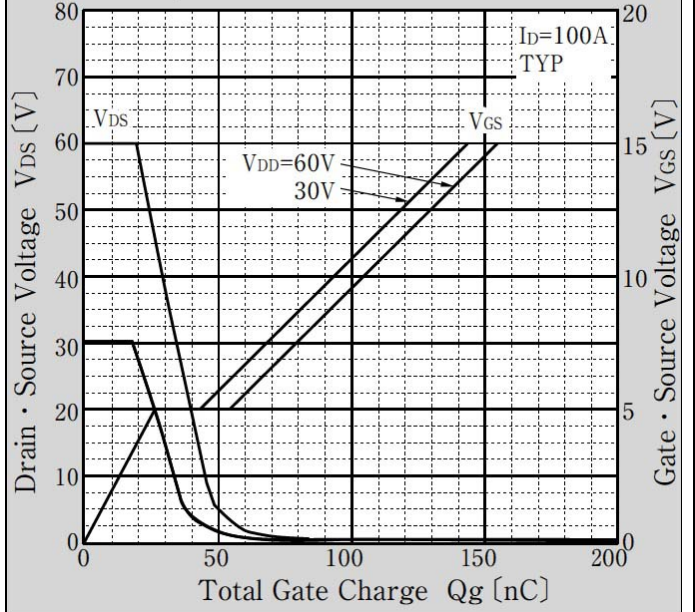
Capacitance Characteristics



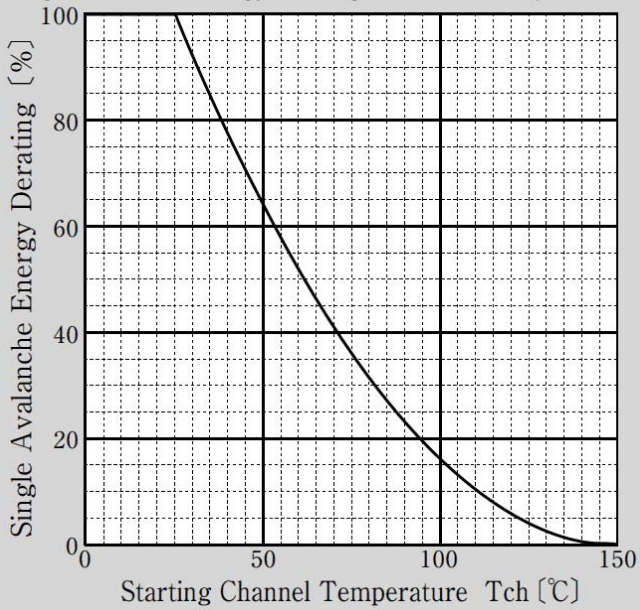
Power Derating - Case Temperature



Gate Charge Characteristics

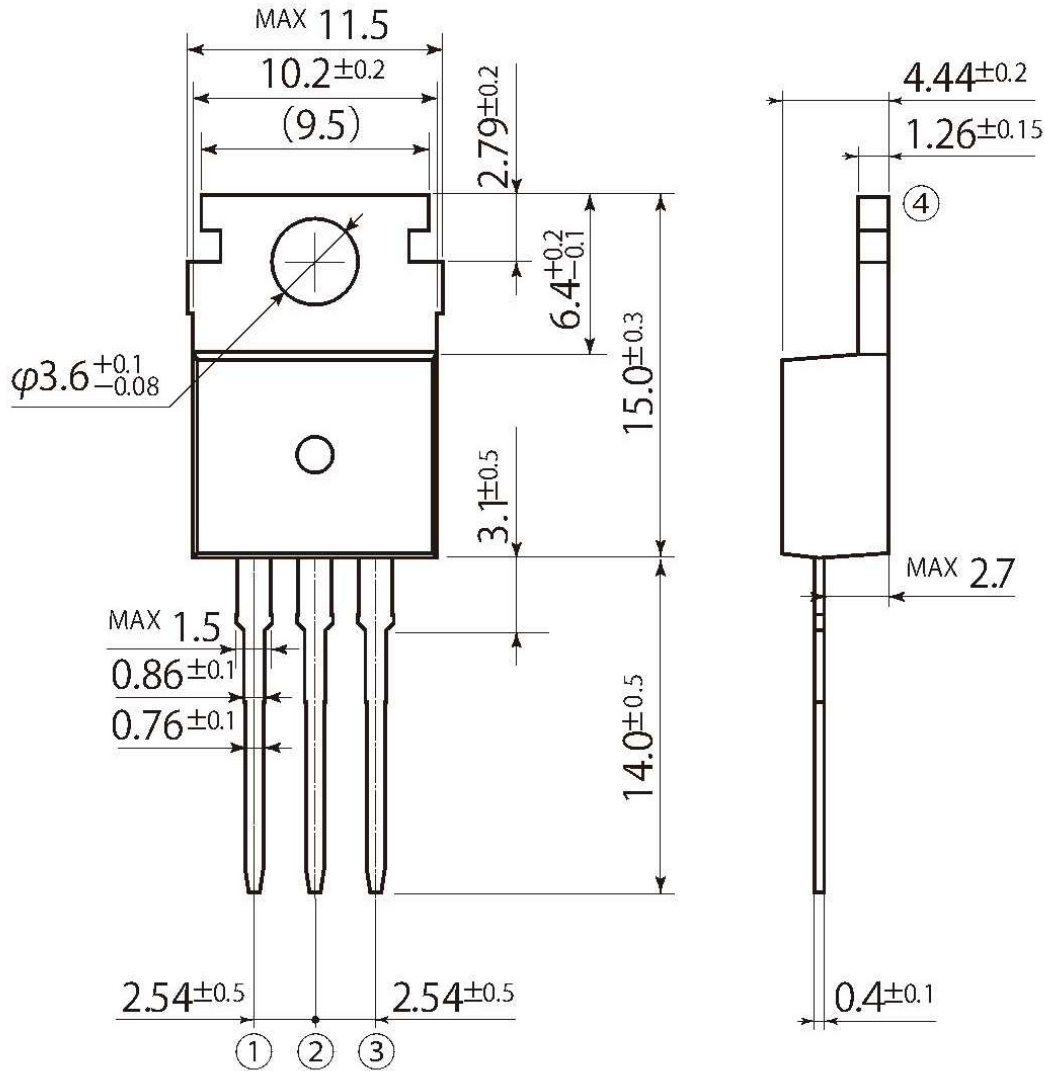


Single Avalanche Energy Derating vs Channel Temperature



J5

JEDEC Code	TO-220AB
JEITA Code	SC-46
House Name	FA



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