



CYPRESS

CY26121

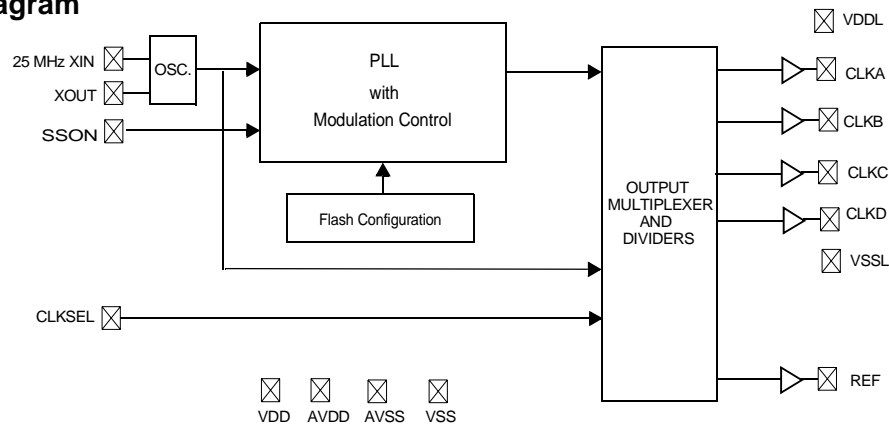
PacketClock™ Spread Spectrum Clock Generator

Features	Benefits
• Integrated phase-locked loop (PLL)	High-performance PLL tailored for Spread Spectrum application
• Low jitter, high-accuracy outputs	Meets critical timing requirements in complex system designs
• 3.3V operation	Enables application compatibility
• 25-MHz input frequency	Works with commonly available crystal or driven reference
• 66.66-MHz or 33.33-MHz selectable output frequency (orig, -3,-11,-31) • 33.33-MHz or 25-MHz selectable output frequency (-2,-21)	Downspread Spread Spectrum with 30-kHz nominal modulation frequency

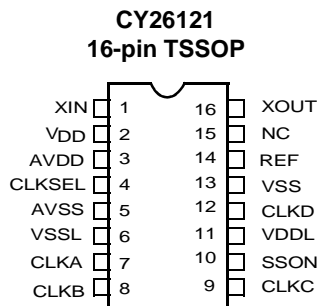
Frequency Table for CLKA-D

Part Number	CLKSEL=0	CLKSEL=1	Spread%	Parallel Crystal Load
CY26121	66.66 MHz	33.33	-2.8%	6 pF
CY26121-2	33.33 MHz	25.00	-2.8%	6 pF
CY26121-3	66.66 MHz	33.33	-1.4%	6 pF
CY26121-11	66.66 MHz	33.33	-2.8%	15 pF
CY26121-21	33.33 MHz	25.00	-2.8%	15 pF
CY26121-31	66.66 MHz	33.33	-1.4%	15 pF

Logic Block Diagram



Pin Configuration



**Pin Description**

Name	Pin Number	Description
XIN	1	Reference input or crystal input
VDD	2	3.3V voltage supply
AVDD	3	3.3V analog voltage
CLKSEL	4 (orig., -11,-3,-31)	0 = 66.66MHz out, 1 = 33.33 MHz out. Weak pull-up.
CLKSEL	4 (-2, -21)	0 = 33.33MHz out, 1 = 25 MHz out. Weak pull-up.
AVSS	5	Analog ground
VSSL	6	CLK ground
CLK(A:D)	7,8,9,12	Clock outputs at V <sub>DDL</sub> level
SSON	10	Spread Spectrum enable pin 0 = SS off; 1 = SS on. Weak pull-up.
VDDL	11	3.3V clock voltage supply
VSS	13	Ground
REF	14	Reference output at V <sub>DD</sub> level
NC	15	No Connect
XOUT <sup>[1]</sup>	16	Crystal Output

**Absolute Maximum Conditions**

Supply Voltage (V<sub>DD</sub>, AV<sub>DD</sub>, V<sub>DDL</sub>) ..... -0.5 to +7.0V  
 DC Input Voltage ..... -0.5V to V<sub>DD</sub> + 0.5  
 Storage Temperature  
 (Non-condensing) ..... -55°C to +125°C  
 Junction Temperature ..... -40°C to +125°C

Data Retention @ T<sub>j</sub> = 125°C ..... > 10 years  
 Package Power Dissipation ..... 350 mW  
 Static Discharge Voltage ..... ≥ 2000V  
 (per MIL-STD-883, Method 3015)  
 (Above which the useful life may be impaired. For user guidelines, not tested.)

**Recommended Operating Conditions**

Parameter	Description	Min.	Typ.	Max.	Unit
V <sub>DD</sub> , AV <sub>DD</sub>	Supply voltage	3.135	3.30	3.465	V
V <sub>DDL</sub>	Supply voltage for CLK (A-D)	3.135	3.30	3.465	V
T <sub>A</sub>	Ambient temperature (commercial temp. grade)	0		70	°C
T <sub>A</sub>	Ambient Temperature (industrial temp grade)	-40		85	°C
C <sub>LOAD</sub>	Max. output load capacitance			15	pF
F <sub>ref</sub>	Reference frequency		25		MHz

**Crystal Specification<sup>[2]</sup>**

Parameter	Name	Min.	Typ	Max.	Unit
CR <sub>load</sub>	Crystal load capacitance (original, -2, -3)		6		pF
CR <sub>load</sub>	Crystal load capacitance (-11,-21,-31)		15		pF
ESR	Equivalent series resistance			50	Ω

**Notes:**

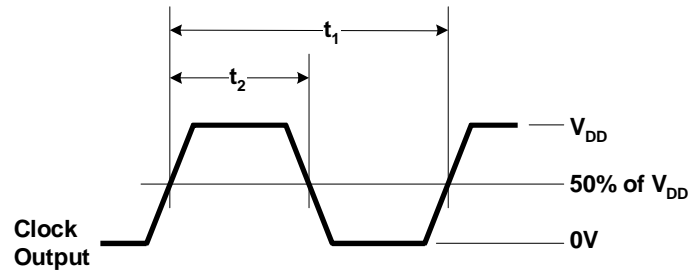
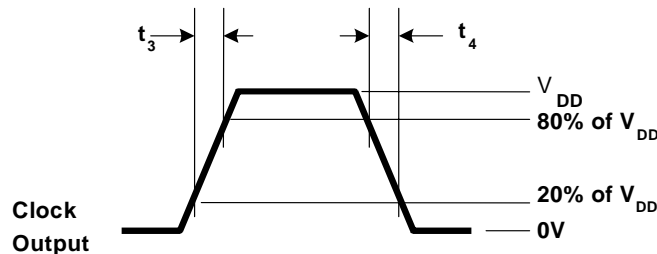
1. Float XOUT if XIN is externally driven.
2. A fundamental parallel resonant crystal must be used

**DC Electrical Specifications**

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
$I_{OH}$	Output High Current	$V_{OH} = V_{DD} - 0.5$ , $V_{DD}/V_{DDL}=3.3V$	12	24		mA
$I_{OL}$	Output Low Current	$V_{OL} = 0.5$ , $V_{DD}/V_{DDL} = 3.3V$	12	24		mA
$I_{IH}$	Input High Current	$V_{IH} = V_{DD}$		5	10	$\mu A$
$I_{IL}$	Input Low Current	$V_{IL} = 0V$			50	$\mu A$
$V_{IH}$	Input High Voltage	CMOS levels	0.7			$V_{DD}$
$V_{IL}$	Input Low Voltage	CMOS levels			0.3	$V_{DD}$
$C_{IN}^{[3]}$	Input Capacitance	Input pins excluding XIN			7	pF
$R_{UP}^{[3]}$	Pull-up resistor on input pins	$V_{DD} = 3.14$ to $3.47V$ , measured at $V_{IN} = 0V$	80	100	150	k $\Omega$
$I_{DD}$	Supply Current	$AV_{DD}/V_{DD}/V_{DDL}$ Current.		42	60	mA

**AC Electrical Specifications<sup>[3]</sup>**

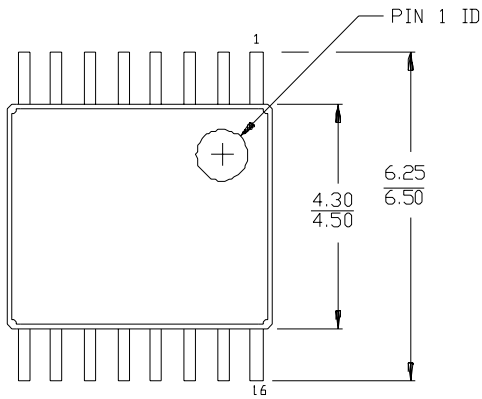
Parameter	Description	Condition	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Duty Cycle is defined in <i>Figure 1</i> , 50% of $V_{DD}$	45	50	55	%
ER	Rising Edge Rate	Output Clock Edge Rate, Measured from 20% to 80% of $V_{DD}$ , $C_{LOAD} = 15$ pF See <i>Figure 2</i> .	0.8	1.4		V/ns
EF	Falling Edge Rate	Output Clock Edge Rate, Measured from 80% to 20% of $V_{DD}$ , $C_{LOAD} = 15$ pF See <i>Figure 2</i> .	0.8	1.4		V/ns
tj	RMS Clock Cycle-to-Cycle Jitter	RMS cycle-to-cycle jitter with Spread on. Measured at $V_{DD}/2$ .		15	40	ps

**Voltage and Timing Definitions**

**Figure 1. Duty Cycle Definition**

**Figure 2.  $ER = (0.6 \times V_{DD}) / t_3$ ,  $EF = (0.6 \times V_{DD}) / t_4$** 
**Notes:**

3. Guaranteed by Characterization, not 100% tested.

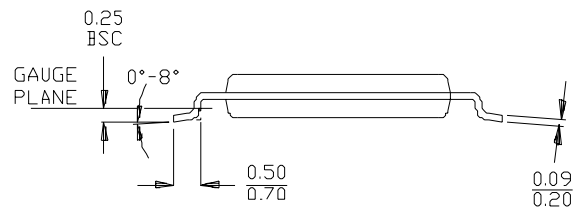
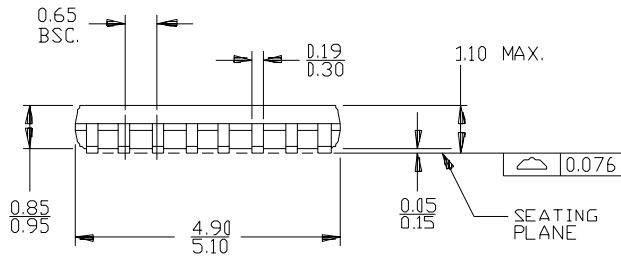
**Ordering Information**

<b>Ordering Code</b>	<b>Package Type</b>	<b>Operating Range</b>
CY26121ZC	16-pin TSSOP	Commercial, 0°C to 70°C
CY26121ZCT	16-pin TSSOP – Tape and Reel	Commercial, 0°C to 70°C
CY26121ZI	16-pin TSSOP	Industrial, –40°C to 85°C
CY26121ZIT	16-pin TSSOP – Tape and Reel	Industrial, –40°C to 85°C
CY26121ZC-2	16-pin TSSOP	Commercial, 0°C to 70°C
CY26121ZC-2T	16-pin TSSOP – Tape and Reel	Commercial, 0°C to 70°C
CY26121ZI-2	16-pin TSSOP	Industrial, –40°C to 85°C
CY26121ZI-2T	16-pin TSSOP – Tape and Reel	Industrial, –40°C to 85°C
CY26121ZC-3	16-pin TSSOP	Commercial, 0°C to 70°C
CY26121ZC-3T	16-pin TSSOP – Tape and Reel	Commercial, 0°C to 70°C
CY26121ZI-3	16-pin TSSOP	Industrial, –40°C to 85°C
CY26121ZI-3T	16-pin TSSOP – Tape and Reel	Industrial, –40°C to 85°C
CY26121ZC-11	16-pin TSSOP	Commercial, 0°C to 70°C
CY26121ZC-11T	16-pin TSSOP – Tape and Reel	Commercial, 0°C to 70°C
CY26121ZI-11	16-pin TSSOP	Industrial, –40°C to 85°C
CY26121ZI-11T	16-pin TSSOP – Tape and Reel	Industrial, –40°C to 85°C
CY26121ZC-21	16-pin TSSOP	Commercial, 0°C to 70°C
CY26121ZC-21T	16-pin TSSOP – Tape and Reel	Commercial, 0°C to 70°C
CY26121ZI-21	16-pin TSSOP	Industrial, –40°C to 85°C
CY26121ZI-21T	16-pin TSSOP – Tape and Reel	Industrial, –40°C to 85°C
CY26121ZC-31	16-pin TSSOP	Commercial, 0°C to 70°C
CY26121ZC-31T	16-pin TSSOP – Tape and Reel	Commercial, 0°C to 70°C
CY26121ZI-31	16-pin TSSOP	Industrial, –40°C to 85°C
CY26121ZI-31T	16-pin TSSOP – Tape and Reel	Industrial, –40°C to 85°C

**Package Drawing and Dimensions**
**16-lead Thin Shrunk Small Outline Package (4.40 MM Body) Z16**


DIMENSIONS IN MILLIMETERS.

MIN.
MAX.



51-85091-\*\*

Parameter	Inches			Millimeters		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.047	—	—	1.20
A <sub>1</sub>	0.002	—	0.006	0.05	—	0.15
A <sub>2</sub>	0.031	0.039	0.041	0.80	1.00	1.05
B	0.007	—	0.012	0.19	—	0.30
C	0.004	—	0.008	0.09	—	0.20
D	0.193	0.197	0.201	4.90	5.00	5.10
E	0.169	0.173	0.177	4.30	4.40	4.50
e	0.026 BSC			0.65 BSC		
H	0.244	0.252	0.260	6.20	6.40	6.60
L	0.018	0.024	0.030	0.45	0.60	0.75
a	0°	—	8°	0°	—	8°

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**Document History Page**

<b>Document Title: CY26121 PacketClock™ Spread Spectrum Clock Generator</b> <b>Document Number: 38-07350</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	121669	02/11/03	CKN	New Data Sheet

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