# LD8526U1

03/23/2021

# Synchronous Rectification Driver with Green Mode Function

*REV. 00*

## General Description

LD8526U1 is a secondary side synchronous rectification (SR) driver IC. It is suited for flyback low side and high side synchronous rectification in CCM, DCM and QR mode. For forward freewheeling rectification application, LD8526U1 can be applied in CCM and DCM operation.

In light load condition, LD8526U1 will enter green mode to reduce operation current by stopping SR MOSFET driving function.

LD8526U1 can generate its own supply voltage through low output voltage or high side rectification applications to charge battery.

## Features

- Suited for low side and high side flyback synchronous rectification in CCM, DCM and QR(valley lock) mode
- Suited for forward freewheeling rectification in CCM and DCM
- Self-supplying for operation with low output voltage and/or high–side rectification without an auxiliary winding.
- Suited for primary side with peak load function (max. frequency 130kHz)
- Suited for PD application, which output voltage range from 3V to 21V, and VCC range from 3V to 9V.
- Programmable turn-off level
- Fast turn-off total delay of 30ns
- 200μA ultra-low green mode operation current
- Gate source/sink capability: 0.5A/-3A

## Applications

- Switching AC/DC adaptor and battery charger
- Open frame switching power supply

## Typical Application

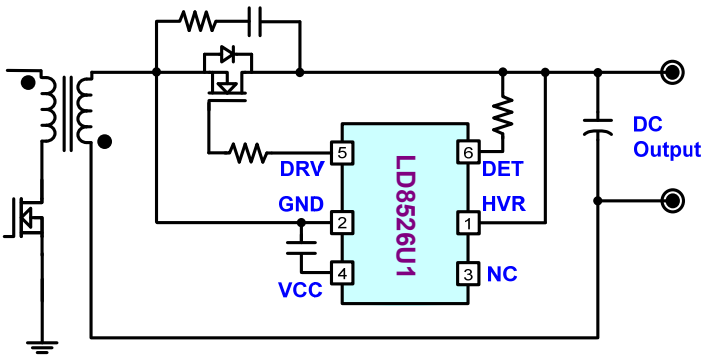



Fig. 1 Flyback High Side Synchronous Rectification

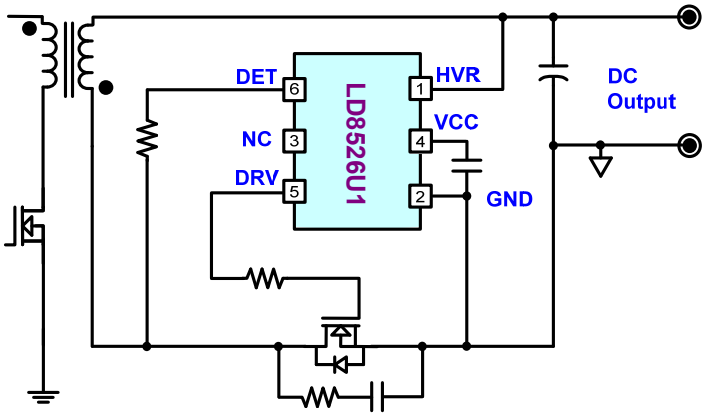
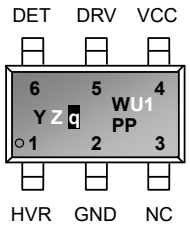



Fig. 2 Flyback Low Side Synchronous Rectification

## Pin Configuration

SOT-26 (TOP VIEW)




Y : Year code (D: 2004, E: 2005…..)
W : Week code
PP : Production code
Z□U1 : LD8526U1

## Ordering Information

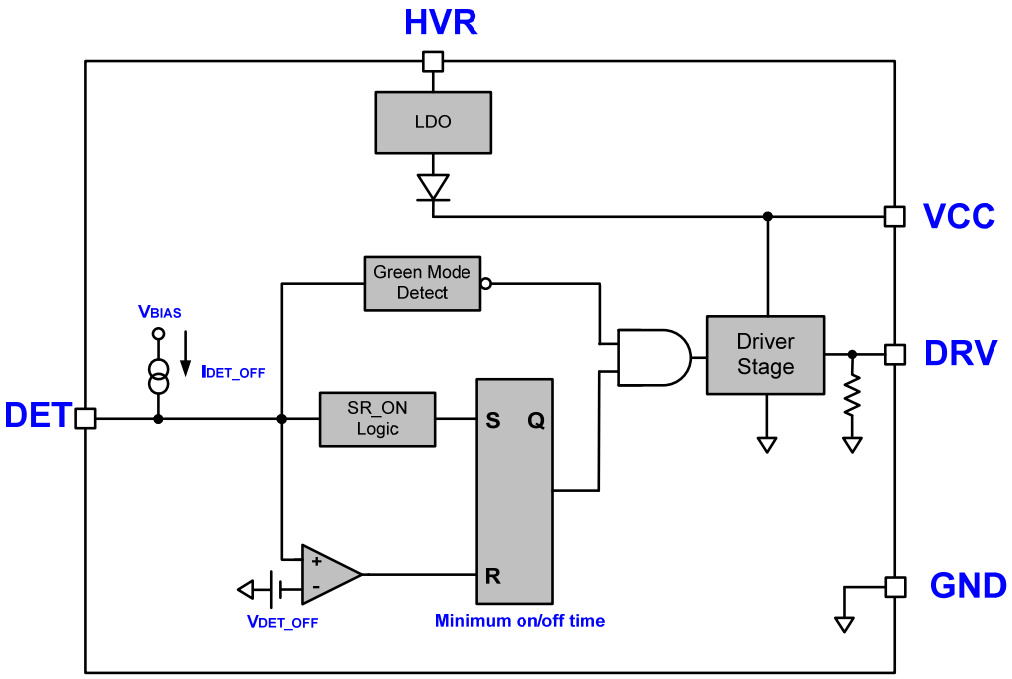
| Part number | Package | | Top Mark | Shipping |
|---|---|---|---|---|
| LD8526U1 GL | SOT-26 | Green Package | YZq/WU1/PP | 3000 / tape & reel |

The LD8526U1 is ROHS compliant/ green packaged.

## Pin Description

| PIN (SOT-26) | NAME | FUNCTION |
|---|---|---|
| 1 | HVR | HV linear regulator input |
| 2 | GND | Ground pin |
| 3 | NC | No connect |
| 4 | VCC | Supply voltage pin |
| 5 | DRV | Driving pin, connector to GATE pin of MOSFET directly or through a resistor |
| 6 | DET | Synchronous rectification detection |

## Block Diagram



## Absolute Maximum Ratings

| | |
|---|---|
| DET | -1V ~ 180V |
| HVR | -1V ~ 180V |
| VCC | -0.3V ~ 14V |
| DRV | -0.3V~VCC+0.3V |
| Maximum Junction Temperature | 150°C |
| Storage Temperature Range | -65°C to 150°C |
| Package Thermal Resistance (SOT-26, $\theta_{JA}$) | 200°C/W |
| Package Thermal Resistance (SOT-26, $\theta_{JC}$) | 115°C/W |
| Power Dissipation (SOT-26, at Ambient Temperature = 85°C) | 200mW |
| Lead temperature (Soldering, 10sec) | 260°C |

**Caution:**

Stresses beyond the ratings specified in "absolute maximum ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## Recommended Operating Conditions

| Item | Min. | Max. | Unit |
|---|---|---|---|
| Operating Junction Temperature | -40 | 125 | °C |
| Supply Voltage VCC | 3 | 12 | V |
| Power MOS Gate Threshold Voltage | 2 | 5 | V |
| Operating Frequency | | 130 | KHz |
| VCC capacitor | 2.2 | | μF |
| MOSFET Ciss (1) | 1000 | 5500 | pF |
| Turn-Off Rgate (1) | 0 | 5 | Ω |
| RDET | | 600 | Ω |

**Notes:**

1. When MOSFET Ciss is the maximum value, turn-off $R_{GATE}$ must be the minimum value. On the contrary, when MOSFET Ciss is the minimum, turn-off $R_{GATE}$ must be the maximum.

## Electrical Characteristics

($T_A$ = +25°C unless otherwise stated, VCC=10V)

| PARAMETER | CONDITIONS | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Supply Voltage (VCC Pin)** | | | | | | |
| UVLO (on) | | $V_{CC\_ON}$ | 2.8 | 3 | 3.2 | V |
| UVLO (off) | | $V_{CC\_OFF}$ | | 2.8 | | V |
| UVLO Hysteresis | | $V_{CC\_HYS}$ | | 0.2 | | V |
| VCC Operating Voltage | HVR=30V | $V_{VCC\_H1}$ | 8 | 9.5 | 11 | V |
| VCC maximum charging current | VCC=3.5V, HVR=30V | $I_{VCC\_CHG}$ | 60 | 66 | | mA |
| Operating Current | VCC=10V, DET=65kHz, 2.2nF on GATE pin | $I_{VCC\_OP1}$ | | 2.2 | 3 | mA |
| | Green mode | $I_{VCC\_OP2}$ | | 200 | 250 | μA |
| | UVLO_OFF mode VCC=2.5V | $I_{VCC\_OFF}$ | | 25 | | μA |
| **Detection Reference (DET Pin)** | | | | | | |
| Turn-on voltage | | $V_{DET\_ON}$ | -400 | -300 | -150 | mV |
| Turn-off voltage | (3) | $V_{DET\_OFF}$ | 10 | 15 | 20 | mV |
| Turn-off compensation current | | $I_{DET\_OFF}$ | 85 | 100 | 115 | μA |
| Ring Reject Threshold | | $V_{DET\_R}$ | 1.3 | 1.6 | 1.8 | V |
| Ring Reject Threshold Hysteresis | | $V_{DET\_RHY}$ | | 1.1 | | V |
| Ring Reject Window | | $T_{DET\_WD}$ | 50 | 70 | 100 | ns |
| Leakage current | $V_{DET}$=180V | $I_{DET\_LK}$ | | | 1 | μA |
| Max. Operating Limit | | $F_{SW\_MAX}$ | | 200 | | kHz |

| PARAMETER | CONDITIONS | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Drive (DRV Pin)** | | | | | | |
| Total Turn-on delay time | (2) | $T_{D\_ON}$ | | 130 | | ns |
| Total Turn-off delay time | (2) | $T_{D\_OFF}$ | | 15 | | ns |
| Pseudo dead time | | $T_{PDT}$ | 3.5 | 4.5 | 5.5 | µs |
| Output High Voltage | Io=+10mA | $V_{DRV\_H}$ | 8 | 9 | | V |
| Output Low Voltage | Io=-10mA | $V_{DRV\_L}$ | | | 0.5 | V |
| Turn-off propagation delay | | $T_P$ | | 15 | | ns |
| Turn-on Rising time | (2), drive voltage from 20%(2V) to 80%(8V) | $T_r$ | | 75 | 200 | ns |
| Turn-off Falling time | (2), drive voltage from 80%(8V) to 20%(2V) | $T_f$ | | 13 | 30 | ns |
| Minimum On Time | | $T_{MIN\_ON}$ | 0.8 | 1 | 1.2 | µs |
| Minimum Off Time | | $T_{MIN\_OFF}$ | 0.1 | 0.3 | 0.5 | µs |

**Notes:**

1. Guaranteed by design.
2. Load capacitance=2.2nF.
3. For avoiding SR being too late to turn off in CCM, $R_{DET}$ must be adjusted from 600R down to appropriate value.

## Typical Performance Characteristics

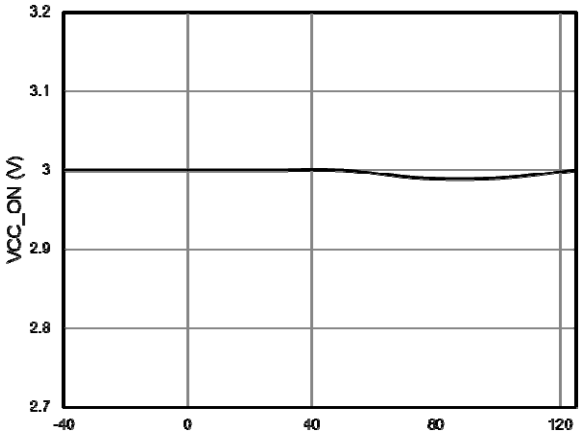



Fig. 3 UVLO ON vs. Temperature

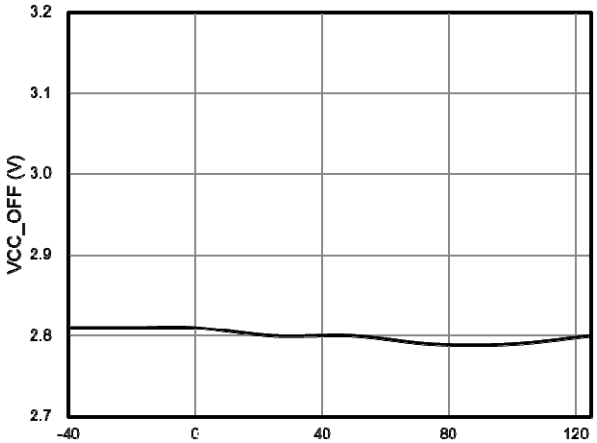



Fig. 4 UVLO OFF vs. Temperature

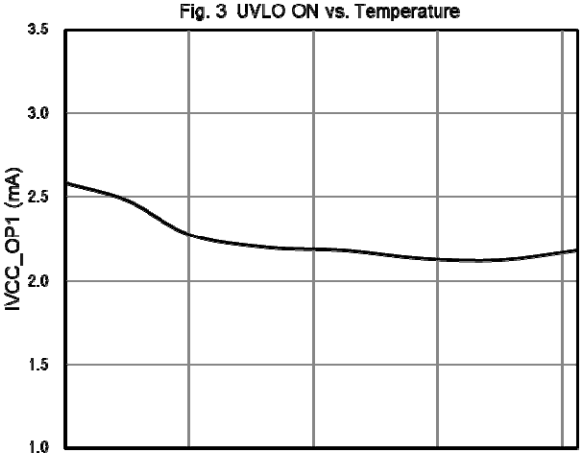



Fig. 5 Operation Current vs. Temperature

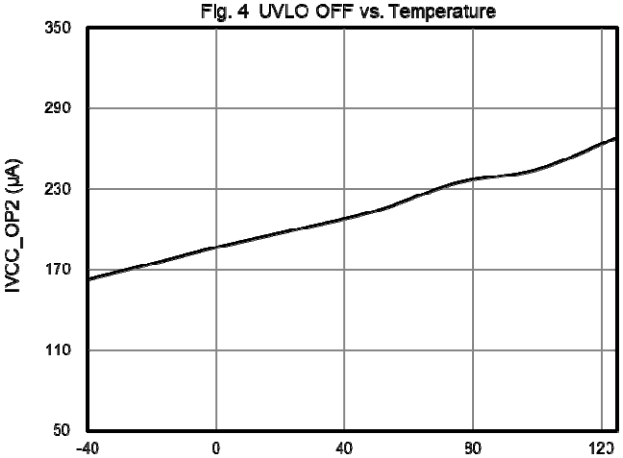



Fig. 6 Green Mode Current vs. Temperature

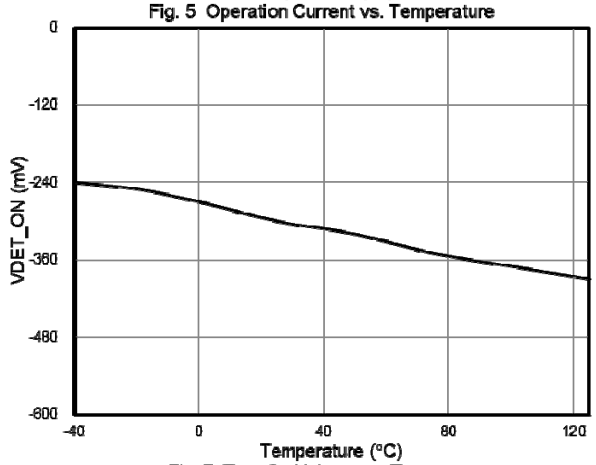



Fig. 7 Turn On Voltage vs. Temperature

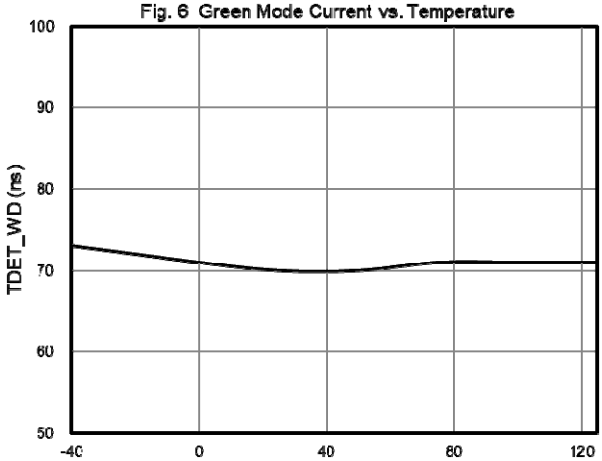



Fig. 8 Ring Reject Window vs. Temperature

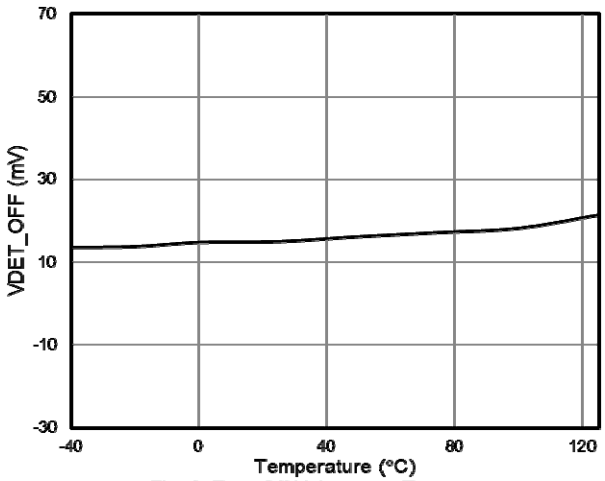



Fig. 9 Turn Off Voltage vs. Temperature

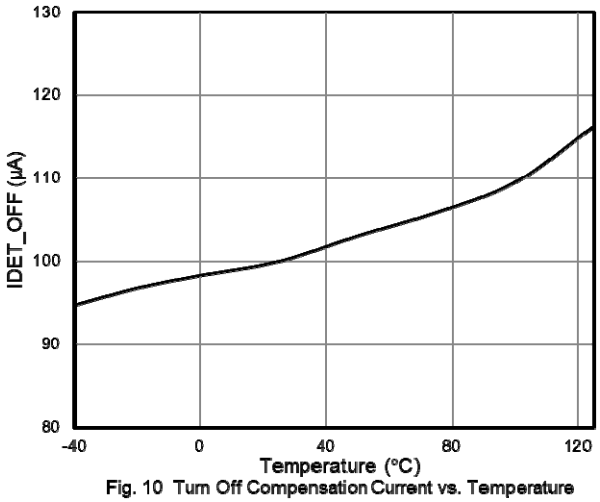



Fig. 10 Turn Off Compensation Current vs. Temperature

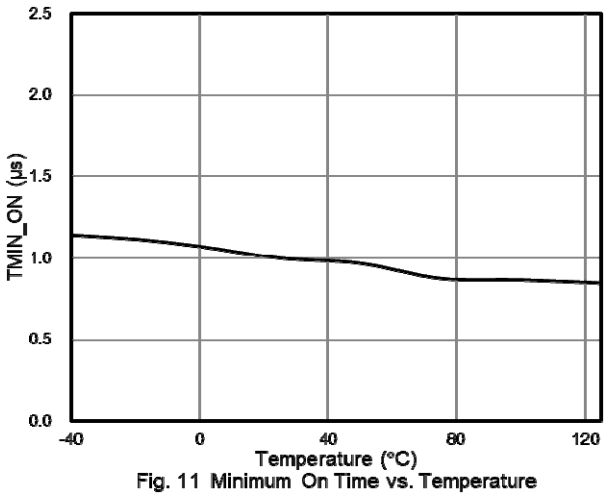



Fig. 11 Minimum On Time vs. Temperature

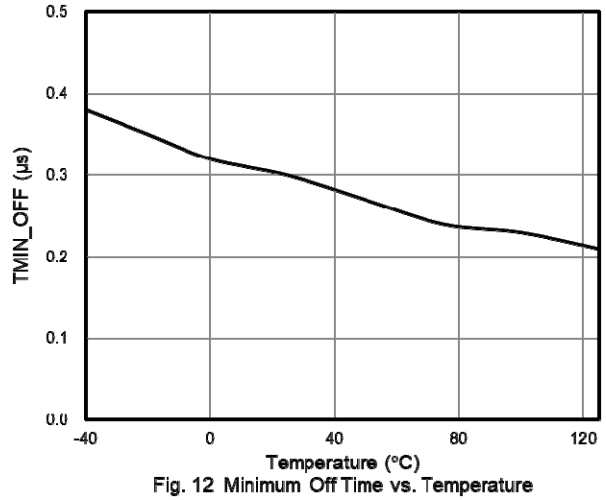



Fig. 12 Minimum Off Time vs. Temperature

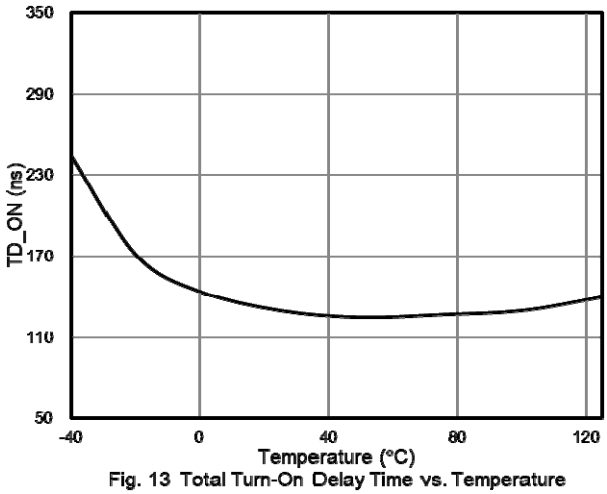



Fig. 13 Total Turn-On Delay Time vs. Temperature

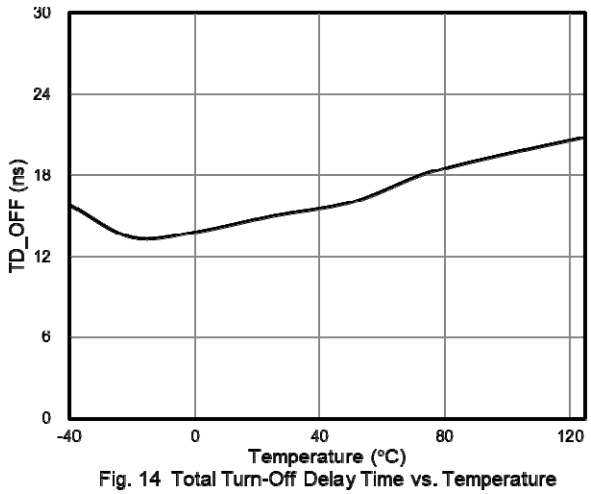



Fig. 14 Total Turn-Off Delay Time vs. Temperature

# Application Information

## Operation Overview

The LD8526U1 is a secondary side synchronous rectification driver IC for CCM and DCM operation. The LD8526U1 not only has excellent dead time control function for safety in load transient, but also only needs very low operation current in green mode. In addition, LD8526U1 can generate its own supply voltage through low output voltage or high side rectification applications to charge battery. Hence, LD8526U1 is suitable for PD application.

## LDO Charge Function

LD8526U1 with a LDO (low drop-out regulator) provides VCC power, and charged by HVR. The LDO charging current can be controlled by connecting a resistor between HVR & MOS drain for the chip temperature optimization. Besides, a capacitor must exist from VCC to GND to store the energy.

## Under Voltage Lockout (UVLO) and Enable Function

An UVLO comparator is implemented in it to detect the voltage on the VCC pin. It will assure the supply voltage enough to turn on the LD8526U1 controllers and further to drive the synchronous rectifier. As shown in Fig. 15, the UVLO(ON) and UVLO(OFF) are 3V and 2.8V respectively.

To enable synchronous rectifier, the following conditions must be met:

1. VCC > UVLO(ON)
2. Exit green mode
3. DET > $V_{DET\_ON}$

With these restrictions, synchronous rectifier always operates in stable condition. Therefore, some unstable transient, which are like turn-on, turn-off, output short, surge, ESD…etc., will not make synchronous rectifier unsafe when it works.

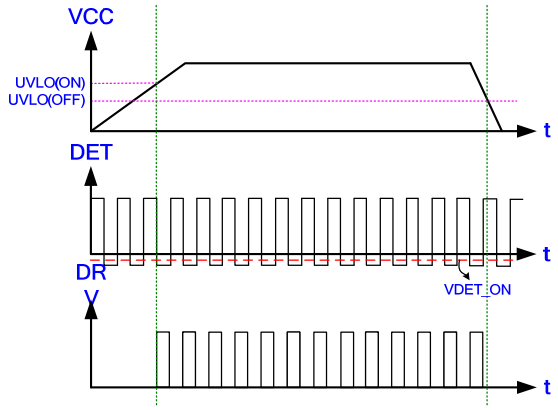



**Fig. 15**

## Green Mode Operation

For improving the efficiency in light load conditions, LD8526U1 stops SR MOSFET driving function to reduce operation current, as shown in Fig. 16.

DET pin detects system behavior, and the internal logic circuit sets DRV to high or low. Hence, LD8526U1 can enter/exit green mode normally, even under dynamic load.

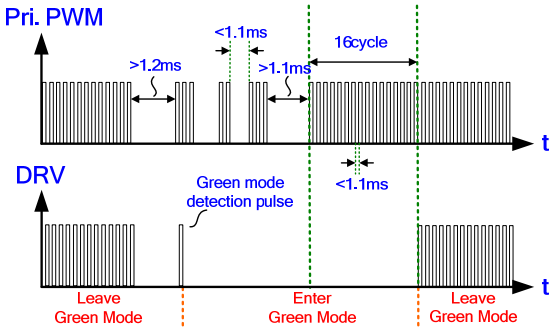



**Fig. 16**

## Turn-on Phase

After a negative voltage (-300 mV typical) is sensed on the DET pin, the driver output voltage (DRV, see block

diagram) is made high and the internal MOSFET is switched on. After switch-on of the SR MOSFET, the input signal on the DET pin is blanked for 1μs. This will eliminate false switch-off due to high frequency ringing at the start of the secondary stroke.

### Turn-off Phase

The DET pin has detection gate on time to do prediction gate pre-drop method ($T_{ON}$ x 0.5 = $T_{PREDICT}$), and the adjusting gate driver voltage is related to MOS parameter.

As soon as the DET voltage is above VDET_OFF, the driver output is pulled to ground. For avoiding SR being too late to turn off in CCM, the following condition must be met, as shown in Fig. 17.

$$V_{DET\_OFF} - I_{DET\_OFF} \times R_{DET} + X = -10mV$$

Where $I_{DET\_OFF}$ = 100μA, $V_{DET\_OFF}$ = +20mV, X= thermal effect and parasitic inductance from trace & electronic components. Hence $R_{DET}$ must be from 600Ω down to find the appropriate turn-off time.

The behavior of DRV in DCM & CCM is shown separately in Fig. 18.

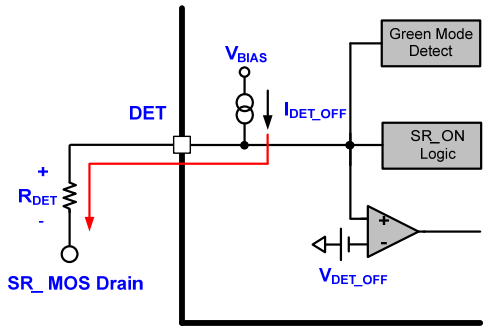



Fig. 17

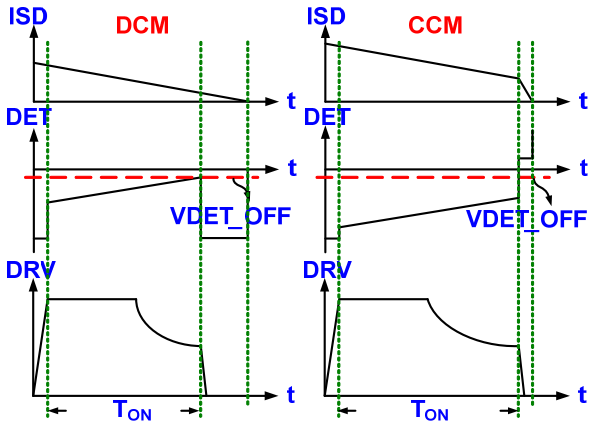



Fig. 18

### Turn-off Phase

The DET pin has detection gate on time to do prediction gate pre-drop method ($T_{ON}$ x 0.5 = $T_{PREDICT}$), and the adjusting gate driver voltage is related to MOS parameter.

As soon as the DET voltage is above VDET_OFF, the driver output is pulled to ground. For avoiding SR being too late to turn off in CCM, the following condition must be met, as shown in Fig. 17.

### Recommended Layout Guide

In order for the system to work properly, layout must pay attention to the following points:

1. Keep the DET and GND loops as small as possible.

2. The power loop needs to be separated from the DET detection loop.

3. Place VCC capacitor as close to IC as possible.

4. Keep the GND of IC and the source pin of MOS as short as possible.

5. To let MOS be turned OFF in time, keep 5nH~20nH inductance of PCB trace as shown in Fig.19 & Fig. 20 in red lines. The suggested trace configurations are listed below:

a. 3.5mm*18mm*2oz

b. 4mm*20mm*2oz

c. 3.5mm*9mm*1oz

d. 4mm*10mm*1oz

e. 6mm*15mm*1oz

In high side application, DET detection point needs to be close to the output capacitor, and in low side application, DET detection point needs to be close to the transformer.

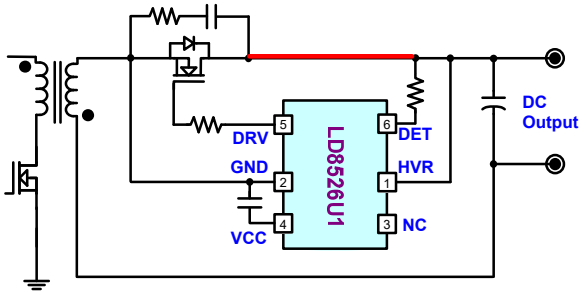



**Fig. 19**

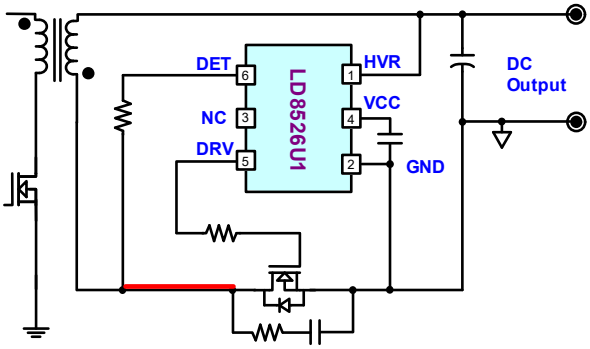
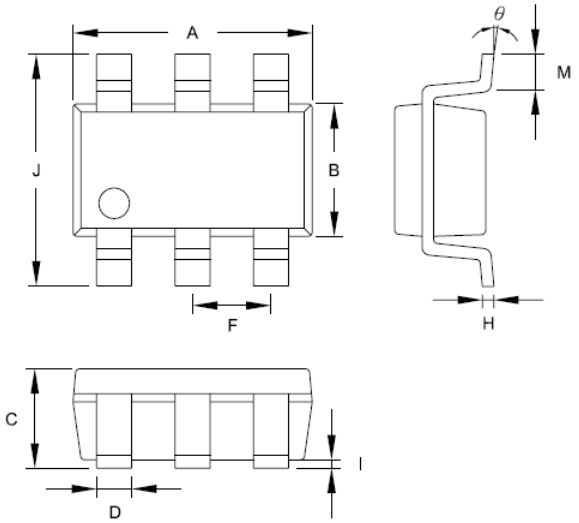



**Fig. 20**

## Package Information

**SOT-26**




| Symbol | Dimension in Millimeters | | Dimensions in Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 2.692 | 3.099 | 0.106 | 0.122 |
| B | 1.397 | 1.803 | 0.055 | 0.071 |
| C | ------- | 1.450 | ------- | 0.057 |
| D | 0.300 | 0.500 | 0.012 | 0.020 |
| F | 0.95 TYP | | 0.037 TYP | |
| H | 0.080 | 0.254 | 0.003 | 0.010 |
| I | 0.050 | 0.150 | 0.002 | 0.006 |
| J | 2.600 | 3.000 | 0.102 | 0.118 |
| M | 0.300 | 0.600 | 0.012 | 0.024 |
| θ | 0° | 10° | 0° | 10° |

## Revision History

| REV. | Date | Change Notice |
|---|---|---|
| 00 | 03/23/2021 | Original Specification |

**Important Notice**

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice.

Customers should verify the datasheets are current and complete before placing order.