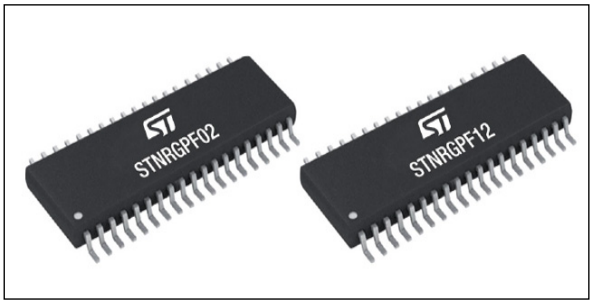
STNRGPF12, STNRGPF02

Two-channel interleaved CCM PFC digital controller

Data brief



Features

- 2 interleaved channels boost PFC
- Fixed frequency CCM average current mode
- Semi digital architecture
- Integrated inrush current limiter function
- Overcurrent and thermal protection
- Soft startup
- Phase-shedding function
- High operating frequency
- Easy integration with other applications
- Flexible design customization to meet specific customer needs
- Firmware
  - Turnkey solution for quick design
  - Graphical User Interface (GUI) for application customization
- Embedded memory data retention 15 years with ECC
- Communication interfaces
  - UART asynchronous protocol for bootloader support
- Operating temperature: -40 °C to 105 °C

Applications

Suitable for PFC applied on welding, industrial motors, UPS, battery chargers, power supplies, air conditioners.

Description

The STNRGPF02 / STNRGPF12 is a digital controller designed specifically for interleaved PFC boost topologies and intended for use in high power applications.

The STNRGPF02 offers traditional inrush current control implemented with mechanical solution based on a relay and limiter resistor.

The STNRGPF12 features a digital inrush current control implemented with a solid state solution based on a silicon controlled rectifier.

The controller is capable of driving up to 2 interleaved channels.

The device works in CCM at fixed frequency with average current mode control, in applications based on a mixed signal (analog/digital) architecture.

The controller can be configured through a dedicated software tool (eDesignSuite) to match a wide range of specific applications. The tool will generate a full schematic which includes a complete list of material and the final binary object code (FW) to be downloaded to the IC.

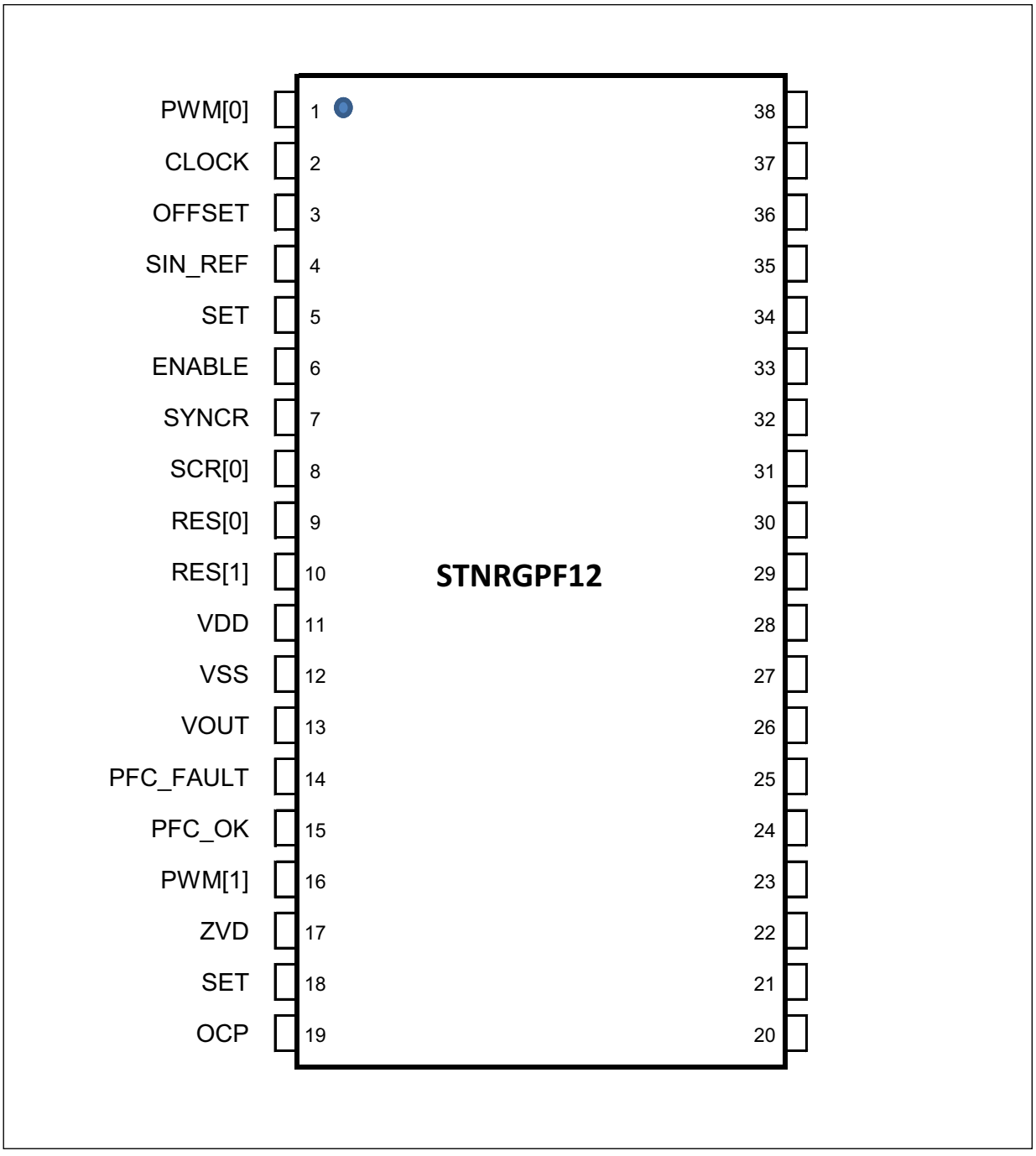
Table 1. Device summary

Order code	Packing
STNRGPF02	Tube
STNRGPF02TR	Tape and reel
STNRGPF12	Tube
STNRGPF12TR	Tape and reel

1 Pinout and pin description

1.1 Pinout

Figure 1. STNRGPF12 pinout



1.2 Pin description

Table 2. Pin description

N°	Type	Name	Pin description
1	OP	PWM[0]	This pin generates the PWM0 for the channel CH0
2	O	CLOCK	This pin generates a PWM signal at selected working frequency having 50% duty cycle. This signal it's used to generate a triangular waveform at switching frequency by means of an external op_amp. The CLOCK signal is also used to realize a protection against undesired commutations
3	O	OFFSET	This pin generated a PWM signal in order to compensate the offset of the external operational amplifier that performs the current loop PI compensator
4	OP	SIN_REF	This pin generates a PWM signal with sinusoidal duty cycle. This PWM signal must be filtered in order to have the current sinusoidal reference that is synchronized with input voltage mains
5	OP	SET_O	This pin generates a pulse in order to trigger ON the CH1 channel with the right out of phase. This pin must be connected to pin 18
6	I	ENABLE	This pin receives the CLOCK signal in order to avoid undesired commutation
7	I	SYNCR[2]	This pin receives the PWM0 signal in order to synchronize the others channels. The falling edge of the PWM0 signal is used to trigger OFF the slave channels CH1 and CH2
8	OP	SCR[0]	This pin generates the PWM in order to drive one of the inrush current limiter switches. Usually an SCR is used to perform this function
9	NC	RES[0]	Reserved
10	NC	RES[1]	Reserved
11	PS	VDD	Supply voltage
12	PS	VSS	Ground
13	PS	VOUT	Supply Voltage of digital section. An external capacitor must be connected to VOUT pin
14	O	PFC_FAULT	During normal operation this pin is high. If a fault condition happens, it is forced low
15	O	PFC_OK	During fault condition this pin is high. When the PFC is ready for load connection it is forced low
16	OP	PWM[1]	This pin generates the PWM for the channel CH1
17	I	ZVD	This pin receive a square wave signal synchronized with input AC voltage. The rising edge of the square wave signal is used by STNRGPF12 to detect the ZVD instant
18	I	SET_I	This pin receives a pulse in order to trigger ON the CH1 channel. This pin must be connected to pin 5

Table 2. Pin description (continued)

N°	Type	Name	Pin description
19	O	OCP	During normal operation this pin is high. If an overcurrent happens it's forced low instantaneously
20	O	FAN	It generates a CMOS/TTL signal that is low until the PFC output power is below a threshold defined during device customization
21	OP	SCR[1]	This pin generates the PWM in order to drive one of the inrush current limiter switches. Usually an SCR is used to perform this function
22	O	PTX	Programming data transmit
23	I	PRX	Programming data receive
24	AI	OUT_PI[3]	Positive input of internal analog comparator 3. It receives the out of analog PI current
25	AI	OUT_PI[2]	Positive input of internal analog comparator 3. It receives the out of analog PI current
26	AI	TRIANG REF	Negative input analog comparators 3 and 2. They receive voltage triangular waveform
27	AI	OCP[0]	Input overcurrent protection
28	AI	OCP[1]	Inductor overcurrent protection
29	PS	VDDA	Analog supply voltage
30	PS	VSSA	Analog ground
31	MI	VIN	This pin is one of the two inputs for the RMS input voltage measurements. A divider resistor is connected to line/neutral input wire
32	MI	TEMP	This pin measures the ambient board temperature. This measurement is realized using the STLM20 device that gives an output voltage proportional to temperature
33	MI	IOUT	This pin measures the PFC output current
34	MI	VOUT	This pin measures the PFC output voltage
35	MI	ICH[0]	This pin measure the RMS current for channel CH[0]
36	MI	ICH[0]	This pin measure the RMS current for channel CH[1]
37	RI		Reserved. This pin must be pulled down by means of a 10k resistor
38	MI	VIN	This pin is one of the two inputs for the RMS input voltage measurements. A divider resistor is connected to line/neutral input wire

2 Revision history

Table 3. Document revision history

Date	Revision	Changes
12-Nov-2018	1	Initial release