Intel® PXA250 and PXA210 Applications Processors

Electrical, Mechanical, and Thermal Specification

Datasheet

Product Features

- High Performance Processor
  - —Intel® XScale™ Microarchitecture
  - —32 KB Instruction Cache
  - —32 KB Data Cache
  - —2 KB “mini” Data Cache
  - —Extensive Data Buffering
- Intel® Media Processing Technology
  - —Enhanced 16-bit Multiply
  - —40-bit Accumulator
- Flexible Clocking
  - —CPU clock from 66 to 300 MHz
  - —Flexible memory clock ratios
  - —Frequency change modes
- Rich Serial Peripheral Set
  - —AC97 Audio Port
  - —I2S Audio Port
  - —USB Client Controller
  - —High Speed UART
  - —Second UART with flow control
  - —FIR and SIR infrared comm ports
- Low Power
  - —Less than 500 mW Typical Internal Dissipation
  - —Supply Voltage may be Reduced to 0.85 V
  - —Low Power/Sleep Modes
- High Performance Memory Controller
  - —Four Banks of SDRAM - up to 100 MHz
  - —Five Static Chip Selects
  - —Support for PCMCIA or Compact Flash
  - —Companion Chip interface
- Additional Peripherals for system connectivity
  - —Multimedia Card Controller (MMC)
  - —SSP Controller
  - —I2C Controller
  - —Two Pulse Width Modulators (PWMs)
  - —All peripheral pins double as GPIOs.
- Hardware debug features
- Hardware Performance Monitoring features

Order Number: 278524-001

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Revision History

Date	Revision	Description
7/6/01	0.5	First Release
2/8/02	-001	First public release of the EMTS

1.0 About this Document

This is the Electrical, Mechanical, and Thermal Specification datasheet for the Intel® PXA250 and PXA210 applications processors. This datasheet contains a functional overview, mechanical data, package signal locations, targeted electrical specifications (simulated), and bus functional waveforms. Detailed functional descriptions other than parametric performance is published in the Intel® PXA250 and PXA210 Applications Processors Developer's Manual. Refer to Table 1, "Related Documentation" for a list of documents that support the PXA250 and PXA210 applications processors.

Table 1. Related Documentation

Document Title	Order / Contact
Intel® PXA250 and PXA210 Applications Processors Developer's Manual	Intel Order # 278522
Intel® XScale™ Microarchitecture for the PXA250 and PXA210 Applications Processors Developer's Manual	Intel Order # 278525
Intel® PXA250 and PXA210 Applications Processors Design Guide	Intel Order # 278523

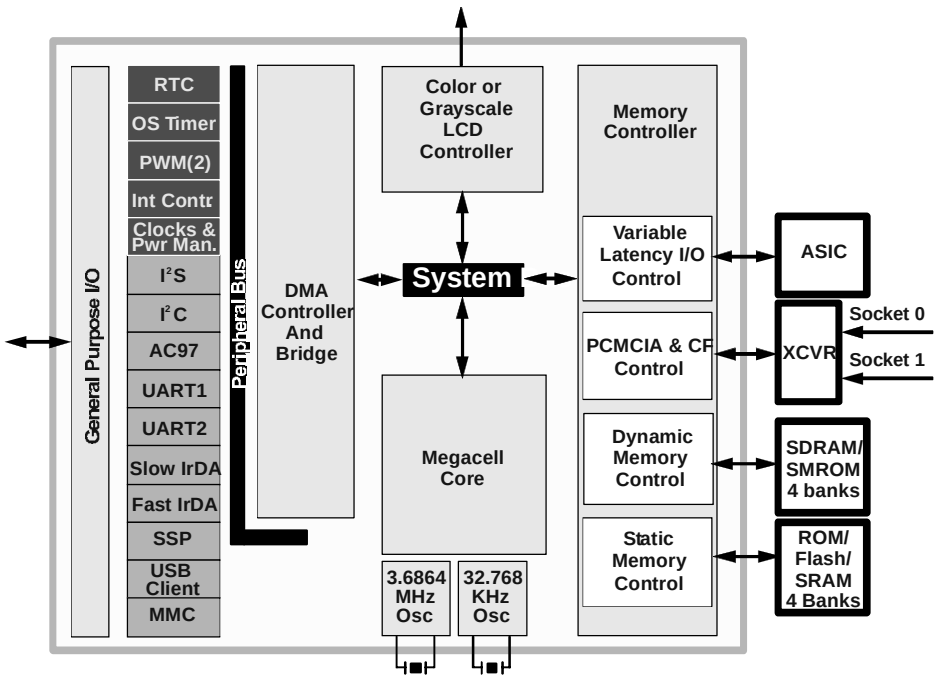
2.0 Functional Overview

The PXA250 and PXA210 applications processors provide high integration, high performance and low power consumption for portable handheld and handset devices. These applications processors incorporate Intel's XScale™ Microarchitecture based on the ARM* V5TE architecture. Refer to the Intel® XScale™ Microarchitecture for the Intel® PXA250 and PXA210 Applications Processors Developer's Manual for implementation details, extensions, and options implemented by Intel's XScale™ Microarchitecture.

The applications processor's memory interface supports a variety of memory types that allow flexibility in design requirements. Hooks for connection to two companion chips permit glueless connection to external devices. An integrated LCD display controller provides support for displays, and permits 1, 2 and 4 bit grayscale and 8 or 16 bit color pixels. A 256-byte palette RAM provides flexibility in color mapping.

A rich set of serial devices as well as general system resources provide enough compute and connectivity capability for many applications. For details on the programming model and theory of operation of each of these units, refer to the Intel® PXA250 and PXA210 Applications Processors Developer's Manual. For the applications processor's block diagram refer to Figure 1, "Applications Processor Block Diagram" on page 8.

Figure 1. Applications Processor Block Diagram



3.0 Package Information

3.1 Package Introduction

The applications processor is offered in two packages;

- The PXA250 applications processor, 256-pin mBGA (refer to Figure 2, “PXA250 Applications Processor” on page 16)
- The PXA210 applications processor, 225-pin TPBGA package (refer to Figure 3, “PXA210 Applications Processor” on page 26)

3.1.1 Functional Signal Definitions

3.1.1.1 PXA250 Signal Pin Descriptions

Signal definitions for the PXA250 applications processor are described in Table 2, "Pin and Signal Descriptions for the PXA250 Applications Processor" on page 9. The physical characteristics of the PXA250 applications processor are shown in Figure 2, "PXA250 Applications Processor" on page 16. The pinout for the PXA250 applications processor is described in Table 3, "PXA250 256-Lead 17x17mm mBGA Pinout — Ballpad Number Order" on page 17.

Table 2. Pin and Signal Descriptions for the PXA250 Applications Processor (Sheet 1 of 7)

Name	Type	Description
Memory Controller Pins		
MA[25:0]	OCZ	Memory address bus. This bus signals the address requested for memory accesses.
MD[15:0]	ICOCZ	Memory data bus. D[15:0] are used for 16-bit data mode.
MD[31:16]	ICOCZ	Memory data bus. D[31:16]: These data bits are used for the PXA250 applications processor 32-bit memories and are not pinned out for the PXA210 applications processor, 16-bit package option.
nOE	OCZ	Memory output enable. This signal should be connected to the output enables of memory devices to control their data bus drivers.
nWE	OCZ	Memory write enable. Connect this signal should to the write enables of memory devices.
nSDCS[3:0]	OCZ	SDRAM CS for banks 0 through 3. Connect these signals to the chip select (CS) pins for SDRAM. nSDCS0 is three-stateable nSDCS1-3 are not
DQM[3:0]	OCZ	SDRAM DQM for data bytes 0 through 3. Connect these signals to the data output mask enables (DQM) for SDRAM.
nSDRAS	OCZ	SDRAM RAS. Connect this signal should to the row address strobe (RAS) pins for all banks of SDRAM.
nSDCAS	OCZ	SDRAM CAS. Connect this signal should to the column address strobe (CAS) pins for all banks of SDRAM.
SDCKE[0]	OC	SDRAM and/or Synchronous Static Memory clock enable. Connect SDCKE[0] to the CKE pins of SMROM and SDRAM-timing Synchronous Flash. The memory controller provides control register bits for deassertion of each SDCKE pin.
SDCKE[1]	OC	SDRAM and/or Synchronous Static Memory clock enable. Connect SDCKE[1] to the SDRAM clock enable pins. It is de-asserted (held low) during sleep. SDCKE[1] is always deasserted upon reset. The memory controller provides control register bits for deassertion of each SDCKE pin.

Table 2. Pin and Signal Descriptions for the PXA250 Applications Processor (Sheet 2 of 7)

Name	Type	Description
SDCLK[2:0]	OCZ	SDRAM and/or Synchronous Static Memory clocks. Connect SDCLK[0] to the clock (CLK) pins of SMROM and SDRAM-timing Synchronous Flash. SDCLK[1] and SDCLK[2] should be connected to the clock pins of SDRAM in bank pairs 0/1 and 2/3, respectively. They are driven by either the internal memory controller clock, or the internal memory controller clock divided by 2. At reset, all clock pins are free running at the divide by 2 clock speed and may be turned off via free running control register bits in the memory controller. The memory controller also provides control register bits for clock division and deassertion of each SDCLK pin. SDCLK[0] control register assertion bit defaults to on if the boot-time static memory bank 0 is configured for SMROM or SDRAM-timing Synchronous Flash. SDCLK[2:1] control register assertion bits are always deasserted upon reset. 0 and 2 are not three-stateable, SDCLK1 is three-stateable
nCS[5]/ GPIO[33]	ICOCZ	Static chip selects. These signals are chip selects for static memory devices such as ROM and Flash. They are individually programmable in the memory configuration registers. nCS[5:3] may be used with variable data latency variable latency I/O devices. See Note [1]
nCS[4]/ GPIO[80]	ICOCZ	Static chip select 4.
nCS[3]/ GPIO[79]	ICOCZ	Static chip select 3.
nCS[2]/ GPIO[78]	ICOCZ	Static chip select 2.
nCS[1]/ GPIO[15]	ICOCZ	Static chip select 1.
nCS[0]	ICOCZ	Static chip select 0. This is the boot memory chip select. nCS[0] is a dedicated pin.
RD/nWR	OCZ	Read/Write for static interface. Intended for use as a steering signal for buffering logic
RDY/ GPIO[18]	ICOCZ	Variable Latency I/O Ready pin (input) See Note [1]
PCMCIA/CF Control Pins		
nPOE/ GPIO[48]	ICOCZ	PCMCIA Output Enable. This PCMCIA signal is an output and performs reads from memory and attribute space. See Note [1]
nPWE/ GPIO[49]	ICOCZ	PCMCIA Write Enable. This signal is an output and performs writes to memory and attribute space. See Note [1]
nPIOW/ GPIO[51]	ICOCZ	PCMCIA I/O Write. This signal is an output and performs write transactions to the PCMCIA I/O space. See Note [1]
nPIOR/ GPIO[50]	ICOCZ	PCMCIA I/O Read. This signal is an output and performs read transactions from the PCMCIA I/O space. See Note [1]
nPCE[2:1]/ GPIO[53, 52]	ICOCZ	PCMCIA Card Enable. These signals are outputs and select a PCMCIA card. Bit one enables the high byte lane and bit zero enables the low byte lane. See Note [1]

Table 2. Pin and Signal Descriptions for the PXA250 Applications Processor (Sheet 3 of 7)

Name	Type	Description
nIOIS16/ GPIO[57]	ICOCZ	I/O Select 16. This signal is an input and is an acknowledge from the PCMCIA card that the current address is a valid 16 bit wide I/O address. See Note [1]
nPWAIT/ GPIO[56]	ICOCZ	PCMCIA Wait. This signal is an input and is driven low by the PCMCIA card to extend the length of the transfers to/from applications processor. See Note [1]
nPSKTSEL/ GPIO[54]	ICOCZ	PCMCIA Socket Select. This signal is an output and is used by external steering logic to route control, address and data signals to one of the two PCMCIA sockets. When PSKTSEL is low, socket zero is selected. When PSKTSEL is high, socket one is selected. This signal has the same timing as an address. See Note [1]
nPREG/ GPIO[55]	ICOCZ	PCMCIA Register Select. This signal is an output and indicates that, on a memory transaction, the target address is attribute space. This signal has the same timing as address. See Note [1]
LCD Controller Pins		
L_DD(15:0)/ GPIO[73:58]	ICOCZ	LCD Controller display data See Note [1]
L_FCLK/ GPIO[74]	ICOCZ	LCD Frame clock See Note [1]
L_LCLK/ GPIO[75]	ICOCZ	LCD Line clock See Note [1]
L_PCLK/ GPIO[76]	ICOCZ	LCD pixel clock See Note [1]
L_BIAS/ GPIO[77]	ICOCZ	AC Bias Drive See Note [1]
Full Function UART Pins		
FFRXD/ GPIO[34]	ICOCZ	Full Function UART Receive pin See Note [1]
FFTXD/ GPIO[39]	ICOCZ	Full Function UART Transmit pin See Note [1]
FFCTS/ GPIO[35]	ICOCZ	Full Function UART Clear-to-Send pin See Note [1]
FFDCD/ GPIO[36]	ICOCZ	Full Function UART Data-Carrier-Detect Pin See Note [1]
FFDSR/ GPIO[37]	ICOCZ	Full Function UART Data-Set-Ready Pin: See Note [1]
FFRI/ GPIO[38]	ICOCZ	Full Function UART Ring Indicator Pin See Note [1]
FFDTR/ GPIO[40]	ICOCZ	Full Function UART Data-Terminal-Ready pin See Note [1]
FFRTS/ GPIO[41]	ICOCZ	Full Function UART Ready-to-Send pin See Note [1]

Table 2. Pin and Signal Descriptions for the PXA250 Applications Processor (Sheet 4 of 7)

Name	Type	Description
Bluetooth UART Pins		
BTRXD/ GPIO[42]	ICOCZ	Bluetooth UART Receive pin See Note [1]
BTTXD/ GPIO[43]	ICOCZ	Bluetooth UART Transmit pin See Note [1]
BTCTS/ GPIO[44]	ICOCZ	Bluetooth UART Clear-to-Send pin See Note [1]
BTRTS/ GPIO[45]	ICOCZ	Bluetooth UART Data-Terminal-Ready pin See Note [1]
MMC Controller Pins		
MMCMD	ICOCZ	Multimedia Card Command pin (I/O)
MMDAT	ICOCZ	Multimedia Card Data Pin (I/O)
SSP Pins		
SSPSCLK/ GPIO[23]	ICOCZ	Synchronous Serial Port Clock (output) See Note [1]
SSPSFRM/ GPIO[24]	ICOCZ	Synchronous serial port Frame Signal (output) See Note [1]
SSPTXD/ GPIO[25]	ICOCZ	Synchronous serial port transmit (output) See Note [1]
SSPRXD/ GPIO[26]	ICOCZ	Synchronous serial port receive (input) See Note [1]
SSPEXTCLK/ GPIO[27]	ICOCZ	Synchronous Serial port external clock (input) See Note [1]
USB Client Pins		
USB_P	IAOA	USB Client port positive Pin of differential pair.
USB_N	IAOA	USB Client port negative Pin of differential pair.
AC97 Controller Pins		
BITCLK/ GPIO[28]	ICOCZ	AC97 Audio Port bit clock (output) See Note [1]
SDATA_IN0/ GPIO[29]	ICOCZ	AC97 Audio Port data in (input) See Note [1]
SDATA_IN1/ GPIO[32]	ICOCZ	AC97 Audio Port data in (input) See Note [1]
SDATA_OUT/ GPIO[30]	ICOCZ	AC97 Audio Port data out (output) See Note [1]
SYNC/ GPIO[31]	ICOCZ	AC97 Audio Port sync signal (output) See Note [1]
nACRESET	OC	AC97 Audio Port reset signal (output) This pin is a dedicated output.

Table 2. Pin and Signal Descriptions for the PXA250 Applications Processor (Sheet 5 of 7)

Name	Type	Description
Standard UART and ICP Pins		
IRRXD/ GPIO[46]	ICOCZ	IrDA Receive signal (input). See Note [1]
IRTXD/ GPIO[47]	ICOCZ	IrDA Transmit signal (output). This pin is the transmit pin for both the SIR and FIR functions. See Note [1]
I2C Controller Pins		
SCL	ICOCZ	I2C clock (Bidirectional) This signal is bidirectional. When it is driving, it functions as an open collector device and requires a pull up resistor. As an input, it expects standard CMOS levels.
SDA	ICOCZ	I2C Data signal (bidirectional). Bidirectional signal. When it is driving, it functions as an open collector device and requires a pull up resistor. As an input, it expects standard CMOS levels.
PWM Pins		
PWM[1:0]/ GPIO[17,16]	ICOCZ	Pulse Width Modulation channels 0 and 1 (outputs) See Note [1]
Dedicated GPIO Pins		
GPIO[1:0]	ICOCZ	General Purpose I/O. These two pins are contained in both the PXA250 and PXA210 Applications Processors. They are preconfigured at a hard reset (nRESET) as wakeup sources for both rising and falling edge detects. These GPIOs do not have alternate functions and are intended to be used as the main external sleep wakeup stimulus.
GPIO[14:2])	ICOCZ	General Purpose I/O: These pins are not included in the PXA210 Applications Processor. See Note [1]
Crystal Pins		
PXTAL	IA	Input connection for 3.6864 Mhz crystal
PEXTAL	OA	Output connection for 3.6846 Mhz crystal Input connection for external oscillator
TXTAL	IA	Input connection for 32.768 Khz crystal
TEXTAL	OA	Output connection for 32.768 Khz crystal Input connection for external oscillator

Table 2. Pin and Signal Descriptions for the PXA250 Applications Processor (Sheet 6 of 7)

Name	Type	Description
Miscellaneous Pins		
BOOT_SEL [2:0]	IC	Boot programming select pins. These pins are sampled to indicate the type of boot device present per the following table; BOOT_SEL[2:0] Description 000 Asynchronous 32-bit ROM 001 Asynchronous 16-bit ROM 010 Reserved 011 Reserved 100 One 32-bit SMROM 101 One 16 bit SMROM 110 Two 16 bit SMROMs (32 bit bus) 111 Reserved
PWR_EN	OCZ	Power Enable. Active high output. PWR_EN enables the external power supply. Negating it signals the power supply that the system is going into sleep mode and that the VDD power supply should be removed.
nBATT_FAUL T	IC	Battery Fault. Active low input. Signals the applications processor that the main power source is going away (battery is low or is removed from the system.) The assertion of nBATT_FAULT causes the applications processor to enter Sleep Mode. The device will not recognize a wakeup event while this signal is asserted.
nVDD_FAULT	IC	VDD Fault. Active low input. Signals the applications processor that the main power source is going out of regulation (i.e. shorted card is inserted). nVDD_FAULT causes the device to enter Sleep Mode. nVDD_FAULT is ignored after a wakeup event until the power supply timer completes (approximately 10 ms).
nRESET	IC	Hard reset. Active low input. nRESET is a level sensitive input which starts the processor from a known address. A LOW level causes the current instruction to terminate abnormally, and all on-chip states to be reset. When nRESET is driven HIGH, the processor re-starts from address 0. nRESET must remain LOW until the power supply is stable and the internal 3.6864 MHz oscillator has come up to speed. While nRESET is LOW the processor performs idle cycles.
nRESET_OUT	OC	Reset Out. Active low output. This signal is asserted when nRESET is asserted and deasserts after nRESET is negated but before the first instruction fetch. nRESET_OUT is also asserted for “soft” reset events (sleep, watchdog reset, GPIO reset)
JTAG Pins		
nTRST	IC	JTAG Test interface reset. If JTAG is used, then you must drive nTRST from low to high either before or at the same time as nRESET If JTAG is not used, then tie nTRST to either nRESET or low.
TDI	IC	JTAG test interface data input. Note this pin has an internal pullup resistor.
TDO	OCZ	JTAG test interface data output. Note this pin does NOT have an internal pullup resistor.
TMS	IC	JTAG test interface mode select. Note this pin has an internal pullup resistor.
TCK	IC	JTAG test interface reference Clock. TCK is the reference clock for all transfers on the JTAG test interface. Note this pin has an internal pulldown resistor.
TEST	IC	Test Mode. You must ground this pin. This pin is for manufacturing purposes only.

Table 2. Pin and Signal Descriptions for the PXA250 Applications Processor (Sheet 7 of 7)

Name	Type	Description
TESTCLK	IC	Test Clock. This pin should be used for test purposes only. An end user should ground this pin.
Power and Ground Pins		
VCC	SUP	Positive supply for the applications processor internal Logic. Connect this supply to the low voltage (.85 - 1.3v) supply on the PCB.
VSS	SUP	Ground supply for the applications processor internal logic. Connect these pins to the common ground plane on the PCB.
PLL_VCC	SUP	Positive supply for the PLLs and Oscillators. It is recommended that you connect this pin to the common low voltage supply.
PLL_VSS	SUP	Ground signal for PLLs.
VCCQ	SUP	Positive supply for all CMOS I/O, except memory bus and PCMCIA pins. Connect these pins to the common 3.3 volt supply on the PCB.
VSSQ	SUP	Ground supply for all CMOS I/O except memory bus and PCMCIA pins. Connect these pins to the common ground plane on the PCB.
VCCN	SUP	Positive supply for memory bus and PCMCIA pins. Connect these pins to the common 3.3 volt supply on the PCB.
VSSN	SUP	Ground supply for memory bus and PCMCIA pins. Connect these pins to the common ground plane on the PCB.
BATT_VCC	SUP	Backup battery connection. Connect this pin to the backup battery supply. If a backup battery is not required, then this pin may be connected to the common 3.3 volt supply on the PCB.

NOTE:
1. *GPIO Reset Operation:* Configured as GPIO inputs by default after any reset. The input buffers for these pins are disabled to prevent current drain.

Figure 2. PXA250 Applications Processor

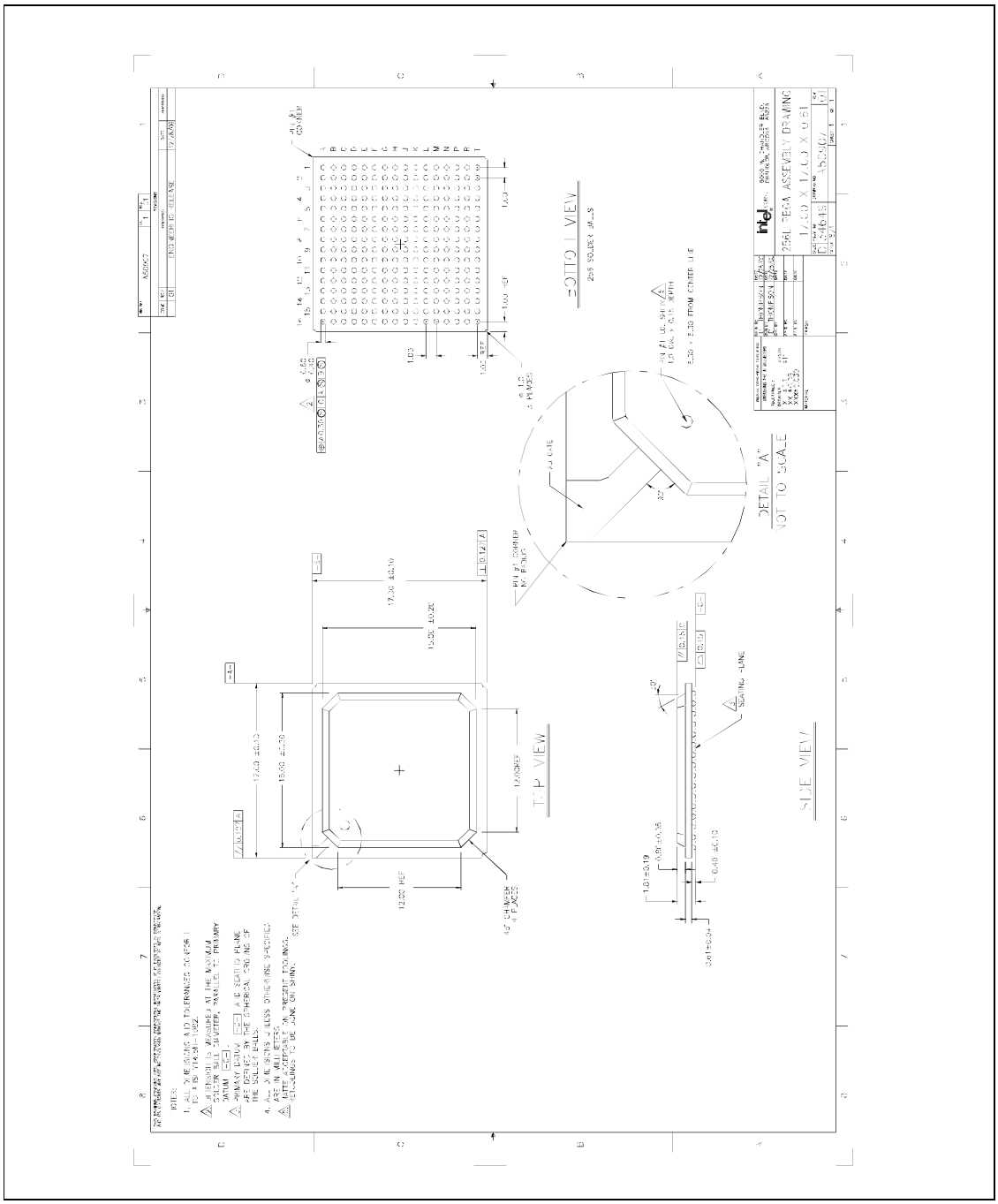


Table 3. PXA250 256-Lead 17x17mm mBGA Pinout — Ballpad Number Order (Sheet 1 of 3)

Ball #	Signal	Ball #	Signal	Ball #	Signal
A1	VCCN	C10	VCCQ	F3	nSDCAS
A2	L_DD[13]/GPIO[71]	C11	VSSQ	F4	VCCN
A3	L_DD[12]/GPIO[70]	C12	USB_P	F5	SDCLK[1]
A4	L_DD[11]/GPIO[69]	C13	VCCQ	F6	VSSQ
A5	L_DD[9]/GPIO[67]	C14	VSSQ	F7	GPIO[10]
A6	L_DD[7]/GPIO[65]	C15	IRTXD/GPIO[47]	F8	FRTS/GPIO[41]
A7	GPIO[11]	C16	VSS	F9	SSPSCLK/GPIO[23]
A8	L_BIAS/GPIO[77]	D1	SDCLK[2]	F10	FFDTR/GPIO[40]
A9	SSPRXD/GPIO[26]	D2	SDCLK[0]	F11	VCC
A10	SDATA_OUT/GPIO[30]	D3	RDnWR	F12	GPIO[9]
A11	SDA	D4	VCCN	F13	BOOT_SEL[2]
A12	FFDCD/GPIO[36]	D5	L_DD[10]/GPIO[68]	F14	GPIO[8]
A13	FFRXD/GPIO[34]	D6	L_DD[5]/GPIO[63]	F15	VSSQ
A14	FFCTS/GPIO[35]	D7	L_DD[1]/GPIO[59]	F16	VSSQ
A15	BTCTS/GPIO[44]	D8	L_LCLK/GPIO[75]	G1	MA[0]
A16	SDATA_IN1/GPIO[32]	D9	SSPTXD/GPIO[25]	G2	VSSN
B1	DQM[1]	D10	nACRESET	G3	nSDCS[2]
B2	DQM[2]	D11	SCL	G4	nWE
B3	L_DD[15]/GPIO[73]	D12	PWM[1]/GPIO[17]	G5	nOE
B4	GPIO[14]	D13	BTTXD/GPIO[43]	G6	nSDCS[1]
B5	GPIO[13]	D14	MMCMD	G7	VCC
B6	GPIO[12]	D15	VCCQ	G8	VSSQ
B7	L_DD[3]/GPIO[61]	D16	VSSQ	G9	VCC
B8	L_PCLK/GPIO[76]	E1	nSDRAS	G10	VSSQ
B9	SSPEXTCLK/GPIO[27]	E2	VSSN	G11	TESTCLK
B10	FFRI/GPIO[38]	E3	SDCKE[1]	G12	TEST
B11	FFDSR/GPIO[37]	E4	SDCKE[0]	G13	BOOT_SEL[1]
B12	USB_N	E5	L_DD[6]/GPIO[64]	G14	VCCQ
B13	BTRXD/GPIO[42]	E6	L_DD[4]/GPIO[62]	G15	GPIO[7]
B14	BTRTS/GPIO[45]	E7	L_DD[[0]/GPIO[58]	G16	BOOT_SEL[0]
B15	IRRXD/GPIO[46]	E8	L_FCLK/GPIO[74]	H1	MA[2]
B16	MMDAT	E9	SSPSFRM/GPIO[24]	H2	MA[1]
C1	RDY/GPIO[18]	E10	SDATA_IN0/GPIO[29]	H3	MD[16]
C2	VSSN	E11	SYNC/GPIO[31]	H4	VCCN
C3	L_DD[14]/GPIO[72]	E12	PWM[0]/GPIO[16]	H5	MD[17]
C4	VSSQ	E13	FFTXD/GPIO[39]	H6	MA[3]
C5	L_DD[8]/GPIO[66]	E14	VCCQ	H7	VSSQ

Table 3. PXA250 256-Lead 17x17mm mBGA Pinout — Ballpad Number Order (Sheet 2 of 3)

Ball #	Signal	Ball #	Signal	Ball #	Signal
C6	VCCQ	E15	VSSQ	H8	VSS
C7	L_DD[2]/GPIO[60]	E16	VSSQ	H9	VSS
C8	VSSQ	F1	nSDCS[0]	H10	VCC
C9	BITCLK/GPIO[28]	F2	nSDCS[3]	H11	nTRST
H12	TCK	L9	VCC	P6	MD[24]
H13	TMS	L10	GPIO[0]	P7	MD26]
H14	GPIO[6]	L11	PWR_EN	P8	MD[27]
H15	TDI	L12	GPIO[1]	P9	nCS[2]/GPIO[78]
H16	TDO	L13	GPIO[2]	P10	MD[29]
J1	MA[7]	L14	VSSQ	P11	MD[12]
J2	VSSN	L15	TEXTAL	P12	MD[31]
J3	MA[6]	L16	TXTAL	P13	nPOE/GPIO[48]
J4	MD[18]	M1	MA[14]	P14	nPCE[1]/GPIO[52]
J5	MA[5]	M2	MD[21]	P15	VSSN
J6	MA[4]	M3	MA[15]	P16	nPSKTSEL/GPIO[54]
J7	VCC	M4	VCCN	R1	MA[18]
J8	VSS	M5	MD[1]	R2	VSSN
J9	VSS	M6	MD[6]	R3	MA[20]
J10	VSSQ	M7	MD[7]	R4	VSSN
J11	GPIO[5]	M8	DQM[0]	R5	MA[22]
J12	GPIO[4]	M9	MD[8]	R6	VSSN
J13	nRESET	M10	MD[15]	R7	MD[25]
J14	VSSQ	M11	BATT_VCC	R8	VSSN
J15	PLL_VCC	M12	GPIO[22]	R9	MD[10]
J16	PLL_VSS	M13	nPREG/GPIO[55]	R10	VSSN
K1	MA[8]	M14	VCCN	R11	MD[30]
K2	MA[9]	M15	VSSN	R12	VSSN
K3	MD[19]	M16	nIOIS16/GPIO[57]	R13	nCS[4]/GPIO[80]
K4	VCCN	N1	MD[22]	R14	VSSN
K5	MA[10]	N2	VSSN	R15	nPIOW/GPIO[51]
K6	MA[11]	N3	MA[16]	R16	nPCE[2]/GPIO[53]
K7	VSSQ	N4	MD[0]	T1	VSS
K8	VCC	N5	VCCN	T2	VCCN
K9	VSSQ	N6	MD[4]	T3	MD[23]
K10	VCC	N7	VCCN	T4	MA[21]
K11	nRESET_OUT	N8	nCS[0]	T5	MA[24]
K12	nBATT_FAULT	N9	VCCN	T6	MD[3]
K13	nVDD_FAULT	N10	MD[13]	T7	MD[5]

Table 3. PXA250 256-Lead 17x17mm mBGA Pinout — Ballpad Number Order (Sheet 3 of 3)

Ball #	Signal	Ball #	Signal	Ball #	Signal
K14	GPIO[3]	N11	VCCN	T8	nCS[1]/GPIO[15]
K15	PXTAL	N12	DREQ[0]/GPIO[20]	T9	nCS[3]/GPIO[79]
K16	PEXTAL	N13	VCCN	T10	MD[9]
L1	MA[12]	N14	DREQ[1]/GPIO[19]	T11	MD[11]
L2	VSSN	N15	GPIO[21]	T12	MD[14]
L3	MA[13]	N16	nPWAIT/GPIO[56]	T13	nCS[5]/GPIO[33]
L4	MD[20]	P1	MA[17]	T14	nPWE/GPIO[49]
L5	MD[2]	P2	MA[19]	T15	nPIOR/GPIO[50]
L6	VCC	P3	VCCN	T16	VCCN
L7	DQM[3]	P4	MA[25]		
L8	MD[28]	P5	MA[23]		

3.1.1.2 PXA210 Signal Pin Descriptions

Signal definitions for the PXA210 applications processor are described in Table 4. The physical characteristics of the PXA210 applications processor are shown in Figure 3, "PXA210 Applications Processor" on page 26. The pinout for the PXA210 applications processor is described in Table 5, "PXA210 225-Lead 13x13mm TPBGA Pinout — Ballpad Number Order" on page 27.

Table 4. Pin and Signal Descriptions for the PXA210 Applications Processor (Sheet 1 of 7)

Pin Name	Type	Signal Descriptions
Memory Controller Pins		
MA[25:0]	OCZ	**Memory address bus.** (output) Signals the address requested for memory accesses.
MD[15:0]	ICOCZ	**Memory data bus.** (input/output) Lower 16 bits of the data bus.
nOE	OCZ	**Memory output enable.** (output) Connect to the output enables of memory devices to control data bus drivers.
nWE	OCZ	**Memory write enable.** (output) Connect to the write enables of memory devices.
nSDCS[1:0]	OCZ	**SDRAM CS for banks 1 and 0.** (output) Connect to the chip select (CS) pins for SDRAM. For the PXA210 applications processor nSDCS0 can be Hi-Z, nSDCS1 cannot.
DQM[1:0]	OCZ	**SDRAM DQM for data bytes 1 and 0.** (output) Connect to the data output mask enables (DQM) for SDRAM.
nSDRAS	OCZ	**SDRAM RAS.** (output) Connect to the row address strobe (RAS) pins for all banks of SDRAM.
nSDCAS	OCZ	**SDRAM CAS.** (output) Connect to the column address strobe (CAS) pins for all banks of SDRAM.
SDCKE[0]	OC	**SDRAM and/or Synchronous Static Memory clock enable.** (output) Connect to the CKE pins of SMROM and SDRAM-timing Synchronous Flash. The memory controller provides control register bits for deassertion.

Table 4. Pin and Signal Descriptions for the PXA210 Applications Processor (Sheet 2 of 7)

Pin Name	Type	Signal Descriptions
SDCKE[1]	OC	**SDRAM and/or Synchronous Static Memory clock enable.** (output) Connect to the clock enable pins of SDRAM. It is deasserted during sleep. SDCKE[1] is always deasserted upon reset. The memory controller provides control register bits for deassertion.
SDCLK[0]	OC	**SDRAM and/or Synchronous Static Memory clocks.** (output) Connect to the clock (CLK) pins of SMROM and SDRAM-timing Synchronous Flash. Connect SDCLK[1] to the clock pins of SDRAM in bank pairs 0/1. It is driven by either the internal memory controller clock or the internal memory controller clock divided by 2. At reset, all clock pins are free running at the divide by 2 clock speed and may be turned off via free running control register bits in the memory controller. The memory controller also provides control register bits for clock division and deassertion of each SDCLK pin. SDCLK[0] control register assertion bit defaults to on if the boot-time static memory bank 0 is configured for SMROM or SDRAM-timing Synchronous Flash. SDCLK[1] control register assertion bit is always deasserted on reset. SDCLK[1] can be Hi-Z, SDCLK[0] cannot.
SDCLK[1]	OCZ	
nCS[5]/ GPIO[33]	ICOCZ	**Static chip selects.** (output) Chip selects to static memory devices such as ROM and Flash. Individually programmable in the memory configuration registers. nCS[5:3] can be used with variable latency I/O devices.
nCS[4]/ GPIO[80]	ICOCZ	
nCS[3]/ GPIO[79]	ICOCZ	
nCS[2]/ GPIO[78]	ICOCZ	
nCS[1]/ GPIO[15]	ICOCZ	
nPWE/ GPIO[49]	ICOCZ	VLIO write enable (output). Used as the write enable signal for Variable Latency I/O.
nCS[0]	ICOCZ	**Static chip select 0.** (output) Chip select for the boot memory. nCS[0] is a dedicated pin.
RD/nWR	OCZ	**Read/Write for static interface.** (output) Signals that the current transaction is a read or write.
RDY/ GPIO[18]	ICOCZ	**Variable Latency I/O Ready pin.** (input) Notifies the memory controller when an external bus device is ready to transfer data.
L_DD[8]/ GPIO[66]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD Controller to the external LCD panel. **Memory Controller alternate bus master request.** (input) Allows an external device to request the system bus from the Memory Controller.
L_DD[15]/ GPIO[73]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD Controller to the external LCD panel. **Memory Controller grant.** (output) Notifies an external device that it has been granted the system bus.
LCD Controller Pins		
L_DD(7:0)/ GPIO[65:58]	ICOCZ	**LCD display data.** (outputs) Transfers pixel information from the LCD Controller to the external LCD panel.
L_DD[8]/ GPIO[66]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD Controller to the external LCD panel. **Memory Controller alternate bus master request.** (input) Allows an external device to request the system bus from the Memory Controller.

Table 4. Pin and Signal Descriptions for the PXA210 Applications Processor (Sheet 3 of 7)

Pin Name	Type	Signal Descriptions
L_DD[9]/ GPIO[67]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD Controller to the external LCD panel. **MMC chip select 0.** (output) Chip select 0 for the MMC Controller.
L_DD[10]/ GPIO[68]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD Controller to the external LCD panel. **MMC chip select 1.** (output) Chip select 1 for the MMC Controller.
L_DD[11]/ GPIO[69]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD Controller to the external LCD panel. **MMC clock.** (output) Clock for the MMC Controller.
L_DD[12]/ GPIO[70]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD Controller to the external LCD panel. **RTC clock.** (output) Real time clock 1 Hz tick.
L_DD[13]/ GPIO[71]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD Controller to the external LCD panel. **3.6864 MHz clock.** (output) Output from 3.6864 MHz oscillator.
L_DD[14]/ GPIO[72]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD Controller to the external LCD panel. **32 kHz clock.** (output) Output from the 32 kHz oscillator.
L_DD[15]/ GPIO[73]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD Controller to the external LCD panel. **Memory Controller grant.** (output) Notifies an external device it has been granted the system bus.
L_FCLK/ GPIO[74]	ICOCZ	**LCD frame clock.** (output) Indicates the start of a new frame. Also referred to as Vsync.
L_LCLK/ GPIO[75]	ICOCZ	**LCD line clock.** (output) Indicates the start of a new line. Also referred to as Hsync.
L_PCLK/ GPIO[76]	ICOCZ	**LCD pixel clock.** (output) Clocks valid pixel data into the LCD's line shift buffer.
L_BIAS/ GPIO[77]	ICOCZ	**AC bias drive.** (output) Notifies the panel to change the polarity for some passive LCD panel. For TFT panels, this signal indicates valid pixel data.
Full Function UART Pins		
FFRXD/ GPIO[34]	ICOCZ	**Full Function UART Receive.** (input) **MMC chip select 0.** (output) Chip select 0 for the MMC Controller.
FFTXD/ GPIO[39]	ICOCZ	**Full Function UART Transmit.** (output) **MMC chip select 1.** (output) Chip select 1 for the MMC Controller.
Bluetooth UART Pins		
BTRXD/ GPIO[42]	ICOCZ	**Bluetooth UART Receive.** (input)
BTTXD/ GPIO[43]	ICOCZ	**Bluetooth UART Transmit.** (output)
BTCTS/ GPIO[44]	ICOCZ	**Bluetooth UART Clear-to-Send.** (input)
BTRTS/ GPIO[45]	ICOCZ	**Bluetooth UART Data-Terminal-Ready.** (output)

Table 4. Pin and Signal Descriptions for the PXA210 Applications Processor (Sheet 4 of 7)

Pin Name	Type	Signal Descriptions
Standard UART and ICP Pins		
IRRXD/ GPIO[46]	ICOCZ	**IrDA receive signal.** (input) Receive pin for the FIR function. **Standard UART receive.** (input)
IRTXD/ GPIO[47]	ICOCZ	**IrDA transmit signal.** (output) Transmit pin for the Standard UART, SIR and FIR functions. **Standard UART transmit.** (output)
MMC Controller Pins		
MMCMD	ICOCZ	**Multimedia Card Command.** (bidirectional)
MMDAT	ICOCZ	**Multimedia Card Data.** (bidirectional)
GPIO[53]	ICOCZ	**MMC clock.** (output) Clock signal for the MMC Controller.
L_DD[9]/ GPIO[67]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD Controller to the external LCD panel. **MMC chip select 0.** (output) Chip select 0 for the MMC Controller.
L_DD[10]/ GPIO[68]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD Controller to the external LCD panel. **MMC chip select 1.** (output) Chip select 1 for the MMC Controller.
L_DD[11]/ GPIO[69]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD Controller to the external LCD panel. **MMC clock.** (output) Clock for the MMC Controller.
FFRXD/ GPIO[34]	ICOCZ	**Full Function UART Receive.** (input) **MMC chip select 0.** (output) Chip select 0 for the MMC Controller.
FFTXD/ GPIO[39]	ICOCZ	**Full Function UART Transmit.** (output) **MMC chip select 1.** (output) Chip select 1 for the MMC Controller.
SSP Pins		
SSPSCLK/ GPIO[23]	ICOCZ	**Synchronous Serial Port Clock.** (output)
SSPSFRM/ GPIO[24]	ICOCZ	**Synchronous Serial Port Frame.** (output)
SSPTXD/ GPIO[25]	ICOCZ	**Synchronous Serial Port Transmit.** (output)
SSPRXD/ GPIO[26]	ICOCZ	**Synchronous Serial Port Receive.** (input)
SSPEXTCLK/ GPIO[27]	ICOCZ	**Synchronous Serial Port External Clock.** (input)
USB Client Pins		
USB_P	IAOAZ	**USB Client Positive.** (bidirectional)
USB_N	IAOAZ	**USB Client Negative pin.** (bidirectional)

Table 4. Pin and Signal Descriptions for the PXA210 Applications Processor (Sheet 5 of 7)

Pin Name	Type	Signal Descriptions
AC97 Controller and I^2S Controller Pins		
BITCLK/ GPIO[28]	ICOCZ	**AC97 Audio Port bit clock.** (input) AC97 clock is generated by Codec 0 and fed into the PXA210 applications processor and Codec 1. **AC97 Audio Port bit clock.** (output) AC97 clock is generated by the PXA210 applications processor. **I^2S bit clock.** (input) I^2S clock is generated externally and fed into PXA210 applications processor. **I^2S bit clock.** (output) I^2S clock is generated by the PXA210 applications processor.
SDATA_IN0/ GPIO[29]	ICOCZ	**AC97 Audio Port data in.** (input) Input line for Codec 0. **I^2S data in.** (input) Input line for the I^2S Controller.
SDATA_IN1/ GPIO[32]	ICOCZ	**AC97 Audio Port data in.** (input) Input line for Codec 1. **I^2S system clock.** (output) System clock from I^2S Controller.
SDATA_OUT/ GPIO[30]	ICOCZ	**AC97 Audio Port data out.** (output) Output from the PXA210 to Codecs 0 and 1. **I^2S data out.** (output) Output line for the I^2S Controller.
SYNC/ GPIO[31]	ICOCZ	**AC97 Audio Port sync signal.** (output) Frame sync signal for the AC97 Controller. **I^2S sync.** (output) Frame sync signal for the I^2S Controller.
nACRESET	OC	**AC97 Audio Port reset signal.** (output)
I^2C Controller Pins		
SCL	ICOCZ	**I^2C clock.** (bidirectional)
SDA	ICOCZ	**I^2C data.** (bidirectional).
PWM Pins		
PWM[1:0]/ GPIO[17:16]	ICOCZ	**Pulse Width Modulation channels 0 and 1.** (outputs)
GPIO Pins		
GPIO[1:0]	ICOCZ	**General Purpose I/O.** Wakeup sources on both rising and falling edges on nRESET.
GPIO[57:48]	ICOCZ	**General Purpose I/O.** Wakeup sources on both rising and falling edges on nRESET.
Crystal and Clock Pins		
PXTAL	IA	**3.6864 Mhz crystal input.**
PEXTAL	OA	**3.6864 Mhz crystal output.**
TXTAL	IA	**32.768 khz crystal input.**
TEXTAL	OA	**32.768 khz crystal output.**
L_DD[12]/ GPIO[70]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD Controller to the external LCD panel. **RTC clock.** (output) Real time clock 1 Hz tick.
L_DD[13]/ GPIO[71]	ICOCZ	**LCD display data.** (output) Transfers the pixel information from the LCD Controller to the external LCD panel. **3.6864 MHz clock.** (output) Output from 3.6864 MHz oscillator.
L_DD[14]/ GPIO[72]	ICOCZ	**LCD display data.** (output) Transfers pixel information from the LCD Controller to the external LCD panel. **32 kHz clock.** (output) Output from the 32 kHz oscillator.

Table 4. Pin and Signal Descriptions for the PXA210 Applications Processor (Sheet 6 of 7)

Pin Name	Type	Signal Descriptions
Miscellaneous Pins		
BOOT_SEL [2:0]	IC	**Boot select pins.** (input) Indicates type of boot device.
PWR_EN	OC	**Power Enable for the power supply.** (output) When negated, it signals the power supply to remove power because the system is entering Sleep Mode.
nBATT_FAULT	IC	**Main Battery Fault.** (input) Signals that main battery is low or removed. Assertion causes the PXA210 applications processor to enter Sleep Mode or force an Imprecise Data Exception, which cannot be masked. The PXA210 applications processor will not recognize a wakeup event while this signal is asserted.
nVDD_FAULT	IC	**VDD Fault.** (input) Signals that the main power source is going out of regulation. nVDD_FAULT causes the PXA210 applications processor to enter Sleep Mode or force an Imprecise Data Exception, which cannot be masked. nVDD_FAULT is ignored after a wakeup event until the power supply timer completes (approximately 10 ms).
nRESET	IC	**Hard reset.** (input) Level sensitive input used to start the processor from a known address. Assertion causes the current instruction to terminate abnormally and causes a reset. When nRESET is driven high, the processor starts execution from address 0. nRESET must remain low until the power supply is stable and the internal 3.6864 MHz oscillator has stabilized.
nRESET_OUT	OC	**Reset Out.** (output) Asserted when nRESET is asserted and deasserts after nRESET is deasserted but before the first instruction fetch. nRESET_OUT is also asserted for “soft” reset events: sleep, watchdog reset, or GPIO reset.
JTAG and Test Pins		
nTRST	IC	JTAG Test Interface Reset. Resets the JTAG/Debug port. If JTAG/Debug is used, drive nTRST from low to high either before or at the same time as nRESET. If JTAG is not used, nTRST must be either tied to nRESET or tied low. Intel recommends that a JTAG/Debug port be added to all systems for debug and download. See Chapter 9 in the “Intel® PXA250 and PXA210 Applications Processor Design Guide” for details.
TDI	IC	**JTAG test data input.** (input) Data from the JTAG controller is sent to the PXA210 using this pin. This pin has an internal pull-up resistor.
TDO	OCZ	**JTAG test data output.** (output) Data from the PXA210 applications processor is returned to the JTAG controller using this pin.
TMS	IC	**JTAG test mode select.** (input) Selects the test mode required from the JTAG controller. This pin has an internal pull-up resistor.
TCK	IC	**JTAG test clock.** (input) Clock for all transfers on the JTAG test interface.
TEST	IC	**Test Mode.** (input) Reserved. Must be grounded.
TESTCLK	IC	**Test Clock.** (input) Reserved. Must be grounded.
Power and Ground Pins		
VCC	SUP	**Positive supply for internal logic.** Must be connected to the low voltage (.85 - 1.3v) supply on the PCB.
VSS	SUP	**Ground supply for internal logic.** Must be connected to the common ground plane on the PCB.
PLL_VCC	SUP	**Positive supply for PLLs and oscillators.** Must be connected to a separate quiet supply plane on the PCB but may be connected to the common low voltage supply.
PLL_VSS	SUP	**Ground signal for PLLs.**
VCCQ	SUP	**Positive supply for all CMOS I/O except memory bus.** Must be connected to the common 3.3 V supply on the PCB.

Table 4. Pin and Signal Descriptions for the PXA210 Applications Processor (Sheet 7 of 7)

Pin Name	Type	Signal Descriptions
VSSQ	SUP	**Ground supply for all CMOS I/O except memory bus.** Must be connected to the common ground plane on the PCB.
VCCN	SUP	**Positive supply for memory bus.** Must be connected to the common 3.3 V or 2.5 V supply on the PCB.
VSSN	SUP	**Ground supply for memory bus and some GPIO pins.** Must be connected to the common ground plane on the PCB.
BATT_VCC	SUP	**Backup battery supply.** Connect to the backup battery supply. If a backup battery is not required then this pin may be connected to the common 3.3 V supply on the PCB.

Figure 3. PXA210 Applications Processor

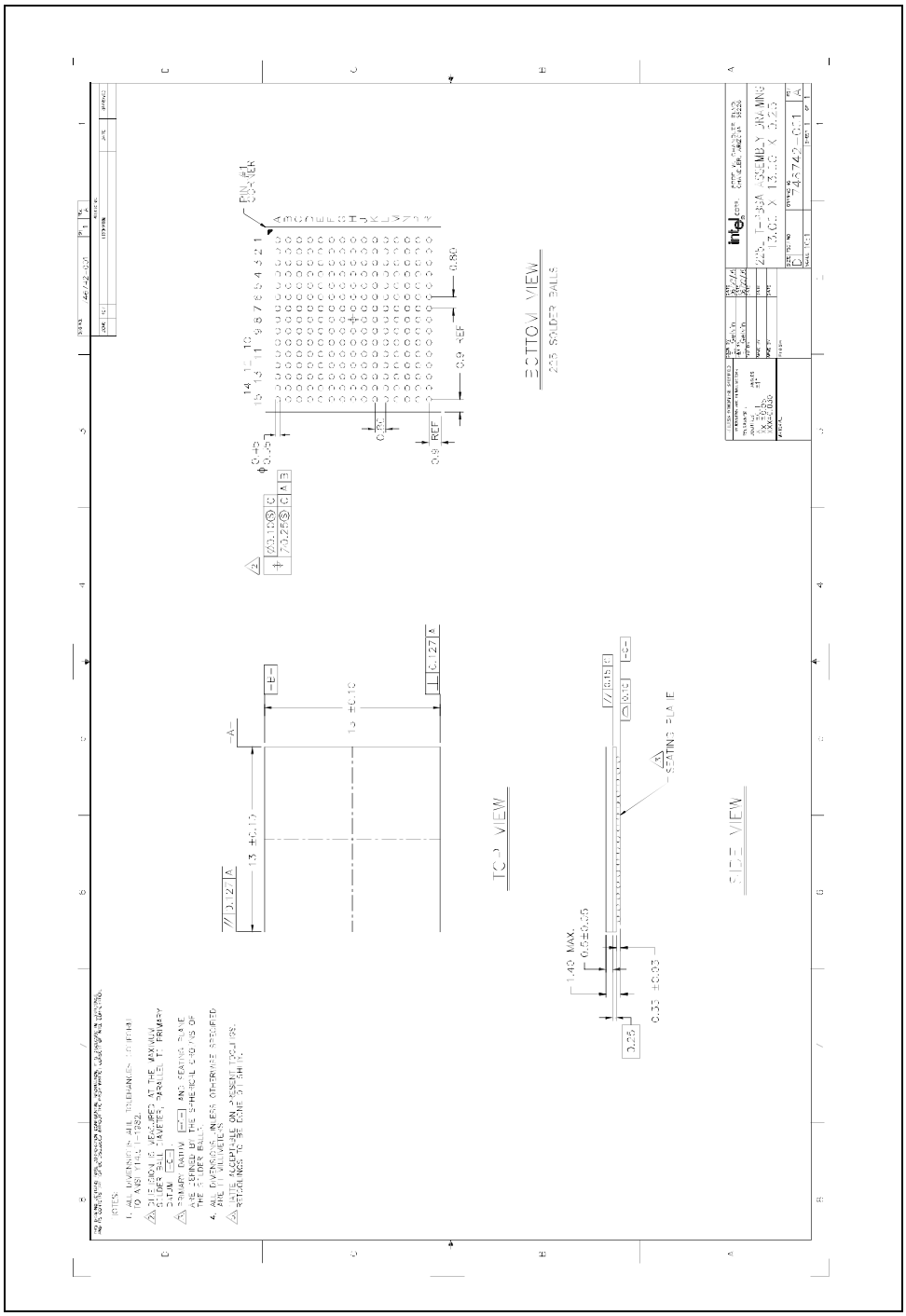


Table 5. PXA210 225-Lead 13x13mm TPBGA Pinout — Ballpad Number Order (Sheet 1 of 3)

Ball #	Signal	Ball #	Signal	Ball #	Signal
A1	DQM[1]	C12	BTTXD/GPIO[43]	F8	SSPRXD/GPIO[26]
A2	L_DD[14]/GPIO[72]	C13	VSSQ	F9	VCC
A3	L_DD[10]/GPIO[68]	C14	VSS	F10	FFTXD/GPIO[39]
A4	VSSQ	C15	VCCQ	F11	VCC
A5	L_DD[6]/GPIO[64]	D1	VCC	F12	VSSQ
A6	L_DD[2]/GPIO[60]	D2	VSSQ	F13	TESTCLK
A7	L_LCLK/GPIO[75]	D3	SDCLK[1]	F14	BOOT_SEL[0]
A8	SSPSCLK/GPIO[23]	D4	L_DD[15]/GPIO[73]	F15	TEST
A9	SSPEXTCLK/GPIO[27]	D5	VCC	G1	MA[0]
A10	nACRESET	D6	L_DD[5]/GPIO[63]	G2	nOE
A11	PWM[1]/GPIO[17]	D7	L_DD[0]/GPIO[58]	G3	nWE
A12	VSSQ	D8	SSPSFRM/GPIO[24]	G4	VCCN
A13	FFRXD/GPIO[34]	D9	SDATA_OUT/GPIO[30]	G5	VSSN
A14	BTCTS/GPIO[44]	D10	SCL	G6	RDnWR
A15	IRRXD/GPIO[46]	D11	SDATA_IN1/GPIO[32]	G7	VSS
B1	RDY/GPIO[18]	D12	BOOT_SEL[1]	G8	VSS
B2	VSSN	D13	VSSQ	G9	VSS
B3	L_DD[13]/GPIO[71]	D14	VSSQ	G10	BTRXD/GPIO[42]
B4	L_DD[9]/GPIO[67]	D15	VSSQ	G11	nTRST
B5	VSSQ	E1	nSDCAS	G12	TDI
B6	L_DD[3]/GPIO[61]	E2	VCCN	G13	TCK
B7	L_PCLK/GPIO[76]	E3	VSSN	G14	TMS
B8	VSSQ	E4	SDCLK[0]	G15	TDO
B9	BITCLK/GPIO[28]	E5	L_DD[11]/GPIO[69]	H1	VCCN
B10	SDA	E6	L_DD[7]/GPIO[65]	H2	VSSN
B11	VSSQ	E7	L_DD[1]/GPIO[59]	H3	MA[2]
B12	USB_N	E8	SSPTXD/GPIO[25]	H4	MA[1]
B13	BTRTS/GPIO[45]	E9	SYNC/GPIO[31]	H5	VCC
B14	IRTXD/GPIO[47]	E10	VCCQ	H6	VSSQ
B15	MMDAT	E11	MMCMD	H7	VSS
C1	SDCKE[1]	E12	VCCQ	H8	VSS
C2	SDCKE[0]	E13	VSSQ	H9	VSS
C3	VCCN	E14	VSSQ	H10	VSSQ
C4	L_DD[12]/GPIO[70]	E15	BOOT_SEL[2]	H11	VCC
C5	VCCQ	F1	VSSN	H12	VSSQ
C6	L_DD[4]/GPIO[62]	F2	NSDCS[0]	H13	VCC
C7	L_BIAS/GPIO[77]	F3	NSDRAS	H14	PLL_VCC

Table 5. PXA210 225-Lead 13x13mm TPBGA Pinout — Ballpad Number Order (Sheet 2 of 3)

Ball #	Signal	Ball #	Signal	Ball #	Signal
C8	VCCQ	F4	NSDCS[1]	H15	PLL_VSS
C9	SDATA_IN0/GPIO[29]	F5	VCC	J1	MA[5]
C10	PWM[0]/GPIO[16]	F6	L_DD[8]/GPIO[66]	J2	MA[6]
C11	USB_P	F7	L_FCLK/GPIO[74]	J3	VSSN
J4	MA[4]	L15	GPIO[0]	P11	VCCN
J5	MA[3]	M1	MA[14]	P12	MD[15]
J6	VSSQ	M2	MA[15]	P13	VCCN
J7	VSS	M3	VCCN	P14	GPIO[50]
J8	VSS	M4	MA[16]	P15	VSSQ
J9	VSS	M5	VCCN	R1	MA[19]
J10	VSSQ	M6	VSSN	R2	MA[20]
J11	nRESET	M7	MD[3]	R3	MA[21]
J12	nRESET_OUT	M8	MD[7]	R4	MA[25]
J13	PWR_EN	M9	nCS[1]/GPIO[15]	R5	MD[1]
J14	nVDD_FAULT	M10	MD[10]	R6	VCCN
J15	nBATT_FAULT	M11	MD[13]	R7	MD[5]
K1	MA[8]	M12	GPIO[48]	R8	nCS[0]
K2	MA[9]	M13	GPIO[52]	R9	nCS[3]/GPIO[79]
K3	MA[10]	M14	VSSN	R10	MD[9]
K4	MA[7]	M15	GPIO[56]	R11	VSSN
K5	VCCN	N1	VSSN	R12	MD[14]
K6	VCC	N2	MA[18]	R13	nCS[4]/GPIO[80]
K7	VSSQ	N3	VSS	R14	nPWE/GPIO[49]
K8	VCC	N4	MA[22]	R15	GPIO[51]
K9	VSSQ	N5	MA[24]		
K10	VCC	N6	VCCN		
K11	GPIO[1]	N7	VCC		
K12	TEXTAL	N8	VSSN		
K13	TXTAL	N9	DQM[0]		
K14	PEXTAL	N10	VCCN		
K15	PXTAL	N11	MD[12]		
L1	VSSN	N12	VSSN		
L2	VCCN	N13	nCS[5]/GPIO[33]		
L3	MA[12]	N14	GPIO[53]		
L4	MA[13]	N15	VCCN		
L5	MA[11]	P1	MA[17]		
L6	VSSQ	P2	VSSN		
L7	MD[2]	P3	VCCN		

Table 5. PXA210 225-Lead 13x13mm TPBGA Pinout — Ballpad Number Order (Sheet 3 of 3)

Ball #	Signal	Ball #	Signal	Ball #	Signal
L8	MD[6]	P4	MA[23]		
L9	VSSN	P5	MD[0]		
L10	MD[11]	P6	VSSN		
L11	BATT_VCC	P7	MD[4]		
L12	GPIO[54]	P8	VCCN		
L13	GPIO[55]	P9	nCS[2]/GPIO[78]		
L14	GPIO[57]	P10	MD[8]		

3.2 Package Power Ratings

Table 6. θ_{JA} and Maximum Power Ratings

Processor	θ_{JA}	Max Power
PXA250	33 C^{O}/w	1.4W
PXA210	44 C^{O}/w	888W

4.0 Electrical Specifications

4.1 Absolute Maximum Ratings

This section provide the Absolute Maximum ratings for the applications processors. Do not exceed these parameters. If you do the part may be permanently damaged. Operation at Absolute Maximum Ratings is not guaranteed.

Table 7. Absolute Maximum Ratings (Sheet 1 of 2)

Symbol	Description	Min	Max	Units
TS	Storage Temperature	-40	125	deg C
VSS_O	Offset Voltage between any two VSS pins (VSS, VSSQ, VSSN)	-0.3	0.3	V
VCC_O	Offset Voltage between any of the following pins: VCCQ and VCCN	-0.3	0.3	V
VCC_HV	Voltage Applied to High Voltage Supplies (VCCQ, VCCN, BATT_VCC)	VSS-0.3	VSS+4.0	V
VCC_LV	Voltage Applied to Low Voltage Supplies (VCC, PLL_VCC)	VSS-0.3	VSS+1.65	V
VIP	Voltage Applied to non-Supply pins except XTAL pins	VSS-0.3	max of VCCQ+0.3, VSS+4.0	V

Table 7. Absolute Maximum Ratings (Sheet 2 of 2)

Symbol	Description	Min	Max	Units
VIP_X	Voltage Applied to XTAL pins (PXTAL, PEXTAL, TXTAL, TEXTAL)	VSS-0.3	max of VCC+0.3, VSS+1.65	V
VESD	Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.		2000	V
IEOS	Maximum DC Input Current (Electrical Overstress) for any non-supply pin		5	mA

4.2 Operating Conditions

This section shows voltage, frequency, and temperature specifications for the applications processor for four different ranges (shown in Table 8, “Voltage, Temperature, and Frequency Electrical Specifications”.) The temperature specification for each range is constant; the frequency range is dependent on the operation voltage.

Note: The parameters in Table 8 are preliminary and subject to change.

Table 8. Voltage, Temperature, and Frequency Electrical Specifications (Sheet 1 of 2)

Symbol	Description	Min	Typical	Max	Units
tA	Ambient Temperature - Extended Temp	-40	-	85	°C
tA	Ambient Temperature - Nominal Temp	0	-	70	°C
VVSS	VSS, VSSN, VSSQ Voltage	-0.3	0	0.3	V
VVCCQ	VCCQ Voltage	3.0	3.3	3.6	V
VVCCN	VCCN Voltage	2.375	2.5/3.3	3.6	V
VBATT	BATT_VCC Voltage	2.2	3.0	3.8	V
Low Voltage Range (PXA250 and PXA210)					
VVCC_L	VCC, PLL_VCC Voltage, Low Range	0.765	0.85	0.935	V
fTURBO_L	Turbo Mode Frequency, Low Range	99.5		132.7	MHz
fSDRAM_L	External Synchronous Memory Frequency, Low Range	50		99.5	MHz
Medium Voltage Range (PXA250 and PXA210)					
VVCC_M	VCC, PLL_VCC Voltage, Mid Range	0.90	1.00	1.10	V
fTURBO_M	Turbo Mode Frequency, Mid Range	99.5		199.1	MHz
fSDRAM_M	External Synchronous Memory Frequency, Mid Range	50		99.5	MHz
High Voltage Range (PXA250)					
VVCC_H	VCC, PLL_VCC Voltage, High Range	0.99	1.10	1.21	V
fTURBO_H	Turbo Mode Frequency, High Range	99.5		298.7	MHz
fSDRAM_H	External Synchronous Memory Frequency, High Range	50		99.5	MHz

Table 8. Voltage, Temperature, and Frequency Electrical Specifications (Sheet 2 of 2)

Symbol	Description	Min	Typical	Max	Units
Peak Voltage Range (PXA250)					
VVCC_P	VCC, PLL_VCC Voltage, Peak Range	1.17	1.30	1.43	V
fTURBO_P	Turbo Mode Frequency, Peak Range	99.5		398.2	MHz
fSDRAM_P	External Synchronous Memory Frequency, Peak Range	50		99.5	MHz

4.3 Targeted DC Specifications

The DC Characteristics for each pin include input sense levels and output drive levels and currents. These parameters can be used to determine maximum DC loading, and also to determine maximum transition times for a given load. The DC Operating Conditions for the High- and Low-Strength Input, Output, and I/O pins are shown in Table 9, “Standard Input, Output, and I/O Pin DC Operating Conditions”. All DC specification values are valid for the entire temperature range of the device.

Table 9. Standard Input, Output, and I/O Pin DC Operating Conditions

Symbol	Description	Min	Typical	Max	Units
Input DC Operating Conditions					
VIH	Input High Voltage, all standard input and I/O pins	0.8*VCCQ		VCCQ	V
VIL	Input Low Voltage, all standard input and I/O pins	VSS		0.2*VCCQ	V
IIN	Input Leakage, all standard input and IO pins			10	µA
Output DC Operating Conditions					
VOH	Output High Voltage, all standard output and I/O pins	VCCQ-0.6		VCCQ	V
VOL	Output Low Voltage, all standard output and I/O pins	VSS		VSS+0.4	V
IOH_H	Output High Current, all standard, high-strength output and I/O pins (VO=VOH)	-10			mA
IOH_L	Output High Current, all standard, low-strength output and I/O pins (VO=VOH)	-3			mA
IOL_H	Output Low Current, all standard, high-strength output and I/O pins (VO=VOH)	10			mA
IOL_L	Output Low Current, all standard, low-strength output and I/O pins (VO=VOH)	3			mA

4.4 Targeted AC Specifications

All the non-analog input, output, and I/O pins on the applications processor can be divided into one of two categories:

1. High Strength Input, Output, and I/O pins:
   - nCS[5:1] (GP 33, 80, 79, 78, 15 respectively), nCS[0]
   - MD[31:0], MA[25:0]
   - DQM[3:0]
   - nOE, nWE, nSDRAS, nSDCAS, nSDCS[3:0]
   - SDCLK[2:0], SDCKE[1:0]
   - RDnWR, RDY (GP[18])
   - nPWE, nPOE pins (GP[49:48])
   - MMCLK (GP[53]), MMCMD, MMDAT
   - TDO
   - nACRESET
2. Low Strength Input, Output, and I/O pins - all remaining non-supply pins

A pin's AC Characteristics include input and output capacitance. These determine loading for external drivers or other load analysis. The AC Characteristics also include a de-rating factor, which indicates how much faster or slower the AC timings get with different loads. The AC Operating Conditions for the high- and low-strength input, output, and I/O pins are shown in Table 10, "Standard Input, Output, and I/O Pin AC Operating Conditions". All AC specification values are valid for entire temperature range of the device.

Table 10. Standard Input, Output, and I/O Pin AC Operating Conditions

Symbol	Description	Min	Typical	Max	Units
CIN	Input Capacitance, all standard input and IO pins			10	pF
COUT_H	Output Capacitance, all standard high-strength output and IO pins	251		501	pF
tdF_H	Output de-rating, falling edge on all standard, high-strength output and I/O pins, from 50pF load.				ns/pF
tdR_H	Output de-rating, rising edge on all standard, high-strength output and I/O pins, from 50pF load.				ns/pF

NOTE: AC Specifications guaranteed for loads in this range. All testing is done at 50pF

4.5 Oscillator Electrical Specifications

The applications processor contains two oscillators: a 32.768 kHz oscillator and a 3.6864 MHz oscillator. Each is for a specific crystal. When choosing a crystal, match the crystal parameters as closely as possible.

4.5.1 32.768 kHz Oscillator Specifications

The 32.768 kHz Oscillator is connected between the TXTAL (amplifier input) and TEXTAL (amplified output). The 32.768 kHz specifications are shown in Table 11, “32.768 kHz Oscillator Specifications”.

Table 11. 32.768 kHz Oscillator Specifications

Symbol	Description	Min	Typical	Max	Units
Crystal Specifications - Typical is FOX NC38					
FXT	Crystal Frequency, TXTAL/TEXTAL		32.768		kHz
LMT	Motional Inductance, TXTAL/TEXTAL		6827.81		H
CMT	Motional Capacitance, TXTAL/TEXTAL		3.455		fF
RMT	Motional Resistance, TXTAL/TEXTAL	6	16	35	kΩ
COT	Shunt Capacitance TXTAL to TEXTAL		1.6		pF
CLT	Load Capacitance TXTAL/TEXTAL		12.5		pF
Amplifier Specifications					
VIH_X	Input High Voltage, TXTAL	0.8*VCC		VCC	V
VIL_X	Input Low Voltage, TXTAL	VSS		0.2*VCC	V
IIN_XT	Input Leakage, TXTAL			1	µA
CIN_XT	Input Capacitance, TXTAL/TEXTAL		18	25	pF
tS_XT	Stabilization Time	2	-	10	s
Board Specifications					
RP_XT	Parasitic Resistance, TXTAL/TEXTAL to any node	20			MΩ
CP_XT	Parasitic Capacitance, TXTAL/TEXTAL, total			5	pF
COP_XT	Parasitic Shunt Capacitance, TXTAL to TEXTAL			0.4	pF

To drive the 32.768 kHz crystal pins from an external source:

- Drive the TEXTAL pin with a digital signal that has a low level near 0 volts and a high level near VCC. Do not exceed VCC or go below VSS by more than 100 mV. The minimum slew rate is 1 volt per 1 µs. The maximum current sourced by the external clock source when the clock is at its maximum positive voltage should be approximately 1 mA.
- Float the TXTAL pin or drive it complementary to the TEXTAL pin, with the same voltage level, slew rate, and input current restrictions.

4.5.2 3.6864 MHz Oscillator Specifications

The 3.6864 MHz Oscillator is connected between the PXTAL (amplifier input) and PEXTAL (amplified output). The 3.6864 MHz specifications are shown in Table 12, “3.6864 MHz Oscillator Specifications”.

Table 12. 3.6864 MHz Oscillator Specifications

Symbol	Description	Min	Typical	Max	Units
Crystal Specifications - Typical is FOX HC49S					
FXP	Crystal Frequency, PXTAL/PEXTAL		3.6864		MHz
LMP	Motional Inductance, PXTAL/PEXTAL		0.50593		H
CMP	Motional Capacitance, PXTAL/PEXTAL		3.68488		fF
RMP	Motional Resistance, PXTAL/PEXTAL	50	99.3	200	W
COP	Shunt Capacitance PXTAL to PEXTAL		1.7		pF
CLP	Load Capacitance PXTAL/PEXTAL		20		pF
Amplifier Specifications					
VIH_X	Input High Voltage, PXTAL	0.8*VCC		VCC	V
VIL_X	Input Low Voltage, PXTAL	VSS		0.2*VCC	V
IIN_XP	Input Leakage, PXTAL			10	µA
CIN_XP	Input Capacitance, PXTAL/PEXTAL		40	50	pF
tS_XP	Stabilization Time	17.8		67.8	ms
Board Specifications					
RP_XP	Parasitic Resistance, PXTAL/PEXTAL to any node	20			MΩ
CP_XP	Parasitic Capacitance, PXTAL/PEXTAL, total			5	pF
COP_XP	Parasitic Shunt Capacitance, PXTAL to PEXTAL			0.4	pF

To drive the 3.6864 MHz crystal pins from an external source:

- Drive the PEXTAL pin with a digital signal with a low level near 0 volts and a high level near VCC. Do not exceed VCC or go below VSS by more than 100 mV. The minimum slew rate is 1 volt / 100 ns. The maximum current sourced by the external clock source when the clock is at its maximum positive voltage should be approximately 1 mA.
- Float the PXTAL pin or drive it complementary to the PXTAL pin, with the same voltage level, slew rate, and input current restrictions. If floated, some degree of noise susceptibility will be introduced in the system, and it is therefore not recommended.

4.6 Reset and Power AC Timing Specifications

The applications processor asserts the nRESET_OUT pin in one of several different modes:

- Power On
- Hardware Reset
- Watchdog Reset
- GPIO Reset
- Sleep Mode

The following sections give the timing and specifications for the entry and exit of these modes.

4.6.1 Power On Timing

The External Voltage Regulator and other power-on devices must provide the applications processor with a specific sequence of power and resets to ensure proper operation. This sequence is shown in Figure 4, “Power-On Reset Timing” on page 36, and detailed in Table 13, “Power-On Timing Specifications” on page 36.

On the applications processor, it is important that the power supplies be powered-up in a certain order to avoid high current situations. The required order is:

1. BATT_VCC
2. VCCQ
3. VCCN
4. VCC and PLL_VCC

The supply in step 3 may be powered at the same time as those in step 2, however, VCCN should not be powered before VCCQ.

Note: If Hardware Reset is entered during Sleep Mode, follow the proper power-supply stabilization times and nRESET timing requirements indicated in Table 13.

Figure 4. Power-On Reset Timing

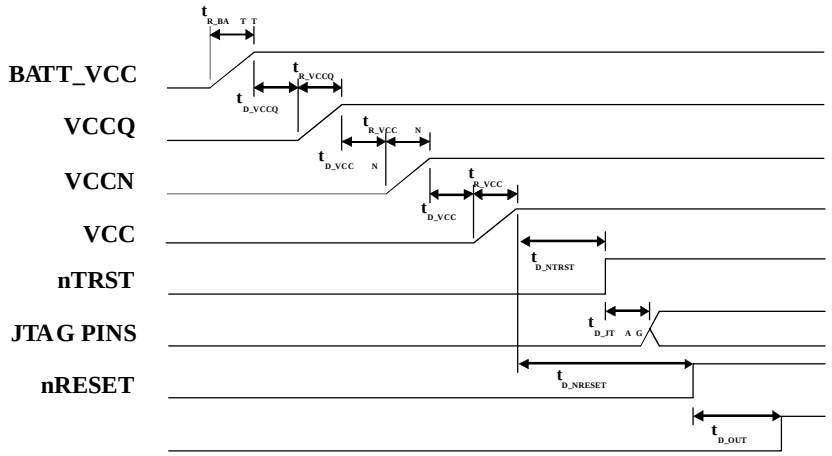


Table 13. Power-On Timing Specifications

Symbol	Description	Min	Typical	Max	Units
tR_BATT	BATT_VCC Rise / Stabilization time	0.01		100	ms
tR_VCCQ	VCCQ, VCCN Rise / Stabilization time	0.01		100	ms
tR_VCC	VCC, PLL_VCC Rise / Stabilization time	0.01		10	ms
tD_VCCQ	Delay between BATT_VCC at voltage and before VCCQ and VCCN applied	0			ms
tD_VCC	Delay from VCCQ, VCCN at voltage and before VCC, PLL_VCC applied	0	—		ms
tD_NTRST	Delay between VCC, PLL_VCC stable and nTRST deasserted	50			ms
tD_JTAG	Delay between nTRST deasserted and JTAG pins active, with nRESET asserted	0.03			ms
tD_NRESET	Delay between VCC, PLL_VCC stable and nRESET deasserted	50			ms
tD_OUT	Delay between nRESET deasserted and nRESET_OUT deasserted	18.1		18.2	ms

4.6.2 Hardware Reset Timing

The timing sequences shown in Hardware Reset Timing for hardware reset assumes stable power supplies at the assertion of nRESET. If the power supplies are unstable, follow the timings indicated in Section 4.6.1, “Power On Timing” on page 35.

Figure 5. Hardware Reset Timing

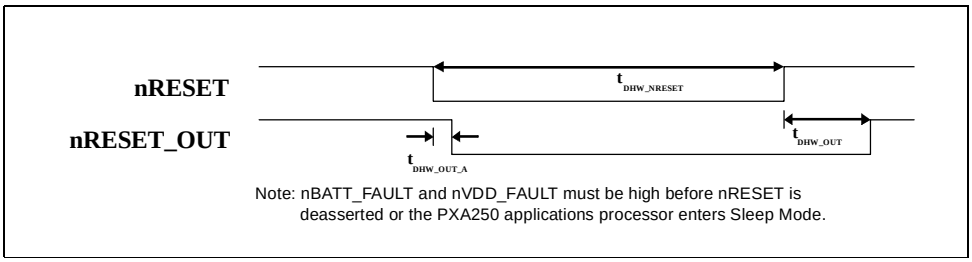


Table 14. Hardware Reset Timing Specifications

Symbol	Description	Min	Typical	Max	Units
tDHW_NRESET	Minimum assertion time of nRESET	0.001			ms
tDHW_OUT_A	Delay between nRESET Asserted and nRESET_OUT Asserted	0		0.001	ms
tDHW_OUT	Delay between nRESET deasserted and nRESET_OUT deasserted	18.1		18.2	ms

4.6.3 Watchdog Reset Timing

Watchdog Reset is an internally generated reset and therefore has no external pin dependencies. The nRESETOUT pin is the only indicator of Watchdog Reset, and it stays asserted for t_{DHW_OUT}. Refer to Figure 5, “Hardware Reset Timing” on page 37.

4.6.4 GPIO Reset Timing

GPIO Reset is generated externally, and the source is reconfigured as a standard GPIO as soon as the reset propagates internally. The clocks module is not reset by GPIO Reset, so the timing varies based on the frequency of clock selected and if the Clocks and Power Manager is in the Frequency Change Sequence when GPIO Reset is asserted (see Section 4.5.1, “32.768 kHz Oscillator Specifications” on page 33.) Figure 6, “GPIO Reset Timing” on page 37 shows the possible timing of GPIO Reset.

Figure 6. GPIO Reset Timing

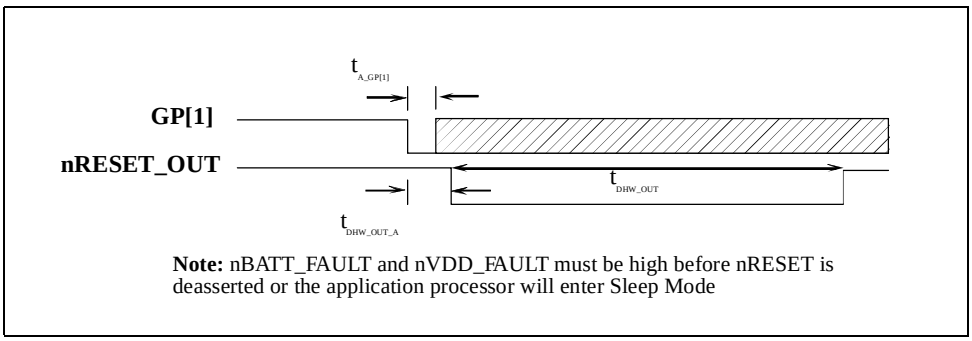


Table 15. GPIO Reset Timing Specifications

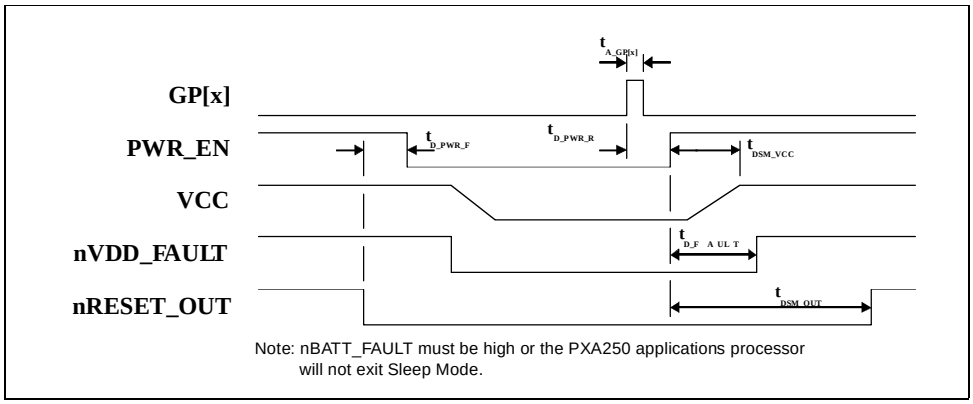
Symbol	Description	Min	Typical	Max	Units
tA_GP[1]	Minimum assert time of GP[1]1 in 3.6864MHz input clock cycles	4		-	cycles
tDHW_OUT_A	Delay between GP[1] Asserted and nRESET_OUT Asserted in 3.6864MHz input clock cycles	6		8	cycles
tDHW_OUT	Delay between nRESET_OUT asserted and nRESET_OUT deasserted, Run or Turbo Mode2	5		28	µs
tDHW_OUT_F	Delay between nRESET_OUT asserted and nRESET_OUT deasserted, during Frequency Change Sequence3	5		380	µs

NOTES:
1. GP[1] is not recognized as a reset source again until configured to do so in software. Software should check the state of GP[1] before configuring as a Reset to ensure no spurious reset is generated.
2. Time is 512*N Processor Clock Cycles plus up to 4 cycles of the 3.6864MHz input clock.
3. Time during the Frequency Change Sequence depends on the state of the PLL Lock Detector at the assertion of GPIO Reset. The Lock Detector has a maximum time of 350µs plus synchronization.

4.6.5 Sleep Mode Timing

Sleep Mode is internally asserted, it and asserts the nRESET_OUT and PWR_EN signals. The sequence indicated in Figure 7, “Sleep Mode Timing” on page 38 and detailed in Figure 16, “Sleep Mode Timing Specifications” on page 39 is the required timing parameters for Sleep Mode.

Figure 7. Sleep Mode Timing



Note: nBATT_FAULT must be high or the PXA250 applications processor will not exit Sleep Mode.

Table 16. Sleep Mode Timing Specifications

Symbol	Description	Min	Typical	Max	Units
tA_GP[x}	Assert Time of GPIO Wake up Source (x=[15:0])	91.6			µs
tD_PWR_F	Delay from nRESET_OUT asserted to PWR_EN deasserted	61		91.6	µs
tD_PWR_R	Delay between GP[x] asserted to PWR_EN asserted	30.5		122.1	µs
tDSM_VCC	Delay between PWR_EN asserted and VCC stable			10	ms
tD_FAULT	Delay between PWR_EN asserted and nVDD_FAULT deasserted			10	ms
tDSM_OUT	Delay between PWR_EN asserted and nRESET_OUT deasserted, OPDE Set	28.0		80	ms
tDSM_OUT_O	Delay between PWR_EN asserted and nRESET_OUT deasserted, OPDE Clear	10.35		10.5	ms

4.7 Memory Bus and PCMCIA AC Specifications

This section gives the timing information for these types of memory:

- SRAM / ROM / Flash / Synchronous Fast Flash Asynchronous writes (Table 17, “SRAM / ROM / Flash / Synchronous Fast Flash AC Specifications” on page 39)
- Variable Latency I/O (Table 18, “Variable Latency I/O Interface AC Specifications” on page 40)
- Card Interface (PCMCIA or Compact Flash) (Table 19, “Card Interface (PCMCIA or Compact Flash) AC Specifications” on page 41)
- Synchronous Memories (Table 20, “Synchronous Memory Interface AC Specifications[1]” on page 42)

Table 17. SRAM / ROM / Flash / Synchronous Fast Flash AC Specifications (Sheet 1 of 2)

Symbol	Description	MEMCLK Frequency (MHz)					Units, Notes
		99.5	118.0	132.7	147.5	165.9	
tromAS	MA(25:0) setup to nCS, nOE, nSDCAS (as nADV) asserted	10	8.5	7.5	6.8	6	ns, 1
tromAH	MA(25:0) hold after nCS, nOE, nSDCAS (as nADV) deasserted	10	8.5	7.5	6.8	6	ns, 1
tromASW	MA(25:0) setup to nWE asserted	30	25.5	22.5	20.4	18	ns, 3
tromAHW	MA(25:0) hold after nWE deasserted	10	8.5	7.5	6.8	6	ns, 1
tromCES	nCS setup to nWE asserted	20	17	15	13.6	12	ns, 2
tromCEH	nCS hold after nWE deasserted	10	8.5	7.5	6.8	6	ns, 1
tromDS	MD(31:0), DQM(3:0) write data setup to nWE asserted	10	8.5	7.5	6.8	6	ns, 1

Table 17. SRAM / ROM / Flash / Synchronous Fast Flash AC Specifications (Sheet 2 of 2)

Symbol	Description	MEMCLK Frequency (MHz)					Units, Notes
		99.5	118.0	132.7	147.5	165.9	
tromDSWH	MD(31:0), DQM(3:0) write data setup to nWE deasserted	20	17	15	13.6	12	ns, 2
tromDH	MD(31:0), DQM(3:0) write data hold after nWE deasserted	10	8.5	7.5	6.8	6	ns, 1
tromNWE	nWE high time between beats of write data	20	17	15	13.6	12	ns, 2

NOTES:
1. This number represents 1 MEMCLK period
2. This number represents 2 MEMCLK periods
3. This number represents 3 MEMCLK periods

Table 18. Variable Latency I/O Interface AC Specifications

Symbol	Description	MEMCLK Frequency (MHz)					Units, Notes
		99.5	118.0	132.7	147.5	165.9	
tvlioAS	MA(25:0) setup to nCS asserted	10	8.5	7.5	6.8	6	ns, 1
tvlioASRW	MA(25:0) setup to nOE or nPWE asserted	10	8.5	7.5	6.8	6	ns, 1
tvlioAH	MA(25:0) hold after nOE or nPWE deasserted	10	8.5	7.5	6.8	6	ns, 1
tvlioCES	nCS setup to nOE or nPWE asserted	20	17	15	13.6	12	ns, 2
tvlioCEH	nCS hold after nOE or nPWE deasserted	10	8.5	7.5	6.8	6	ns, 1
tvlioDSW	MD(31:0), DQM(3:0) write data setup to nPWE asserted	10	8.5	7.5	6.8	6	ns, 1
tvlioDSWH	MD(31:0), DQM(3:0) write data setup to nPWE deasserted	20	17	15	13.6	12	ns, 2
tvlioDHW	MD(31:0), DQM(3:0) hold after nPWE deasserted	10	8.5	7.5	6.8	6	ns, 1
tvlioDHR	MD(31:0) read data hold after nOE deasserted	0	0	0	0	0	ns
tvlioRDYH	RDY hold after nOE, nPWE deasserted	0	0	0	0	0	ns
tvlioNPWE	nPWE, nOE high time between beats of write or read data	20	17	15	13.6	12	ns, 2

NOTES:
1. This number represents 1 MEMCLK period
2. This number represents 2 MEMCLK periods

Table 19. Card Interface (PCMCIA or Compact Flash) AC Specifications

Symbol	Description	MEMCLK Frequency (MHz)					Units, Notes
		99.5	118.0	132.7	147.5	165.9	
tcardAS	MA(25:0), nPREG, PSKTSEL, nPCE setup to nPWE, nPOE, nPIOW, or nPIOR asserted	20	17	15	13.6	12	ns, 1
tcardAH	MA(25:0), nPREG, PSKTSEL, nPCE hold after nPWE, nPOE, nPIOW, or nPIOR deasserted	10	8.5	7.5	6.8	6	ns, 1
tcardDS	MD(31:0) setup to nPWE, nPOE, nPIOW, or nPIOR asserted	10	8.5	7.5	6.8	6	ns, 1
tcardDH	MD(31:0) hold after nPWE, nPOE, nPIOW, or nPIOR deasserted	10	8.5	7.5	6.8	6	ns, 1
tcardCMD	nPWE, nPOE, nPIOW, or nPIOR command assertion	30	25.5	22.5	20.4	18	ns, 1

NOTE: These numbers are minimums. They can be much longer based on the programmable Card Interface timing registers.

Table 20. Synchronous Memory Interface AC Specifications[1]

Symbol	Description	MIN	MAX	Units, Notes
SDRAM / SMROM / SDRAM-Timing Synchronous Flash (Synchronous)				
tsynCLK	SDCLK period	10	20	ns, 2
tsynCMD	nSDCAS, nSDRAS, nWE, nSDCS assert time	1		sdclk
tsynRCD	nSDRAS to nSDCAS assert time	1		sdclk
tsynCAS	nSDCAS to nSDCAS assert time	2		sdclk
tsynSDOS	MA(25:0), MD(31:0), DQM(3:0), nSDCS(3:0), nSDRAS, nSDCAS, nWE, nOE, SDCKE(1:0), RDnWR output setup time to SDCLK(2:0) rise	3.8		ns, 3
tsynSDOH	MA(25:0), MD(31:0), DQM(3:0), nSDCS(3:0), nSDRAS, nSDCAS, nWE, nOE, SDCKE(1:0), RDnWR output hold time from SDCLK(2:0) rise	3.6		ns, 3
tsynSDIS	MD(31:0) read data input setup time from SDCLK(2:0) rise	0.5		ns
tsynDIH	MD(31:0) read data input hold time from SDCLK(2:0) rise	1.5		ns
Fast Flash (Synchronous READS only)				
tffCLK	SDCLK period	15	20	ns, 4
tffAS	MA(25:0) setup to nSDCAS (as nADV) asserted	0.5		sdclk
tffCES	nCS setup to nSDCAS (as nADV) asserted	0.5		sdclk
tffADV	nSDCAS (as nADV) pulse width	1		sdclk
tffOS	nSDCAS (as nADV) deassertion to nOE assertion	3		sdclk
tffCEH	nOE deassertion to nCS deassertion	4		sdclk

NOTES:
1. These numbers are for a maximum 99.5 MHz MEMCLK and 99.5 MHz output SDCLK.
2. SDCLK for SDRAM, SMROM, and SDRAM-timing Synchronous Flash can be at the slowest, divide-by-2 of the 99.5 MHz MEMCLK. It can be 99.5MHz at the fastest.
3. This number represents 1/2 SDCLK period.
4. SDCLK for Fast Flash can be at the slowest, divide-by-2 of the 99.5 MHz MEMCLK. It can be divide-by-2 of the 132.7 MHz MEMCLK at its fastest.

4.8 Peripheral Module AC Specifications

This section describes the AC Specifications for these peripheral units:

- LCD
- SSP

4.8.1 LCD Module AC Timing

Figure 8 describes the LCD timing parameters. The LCD pin timing specifications are referenced to the pixel clock (L_PCLK). Values for the parameters are given in Table 21.

Figure 8. LCD AC Timing Definitions

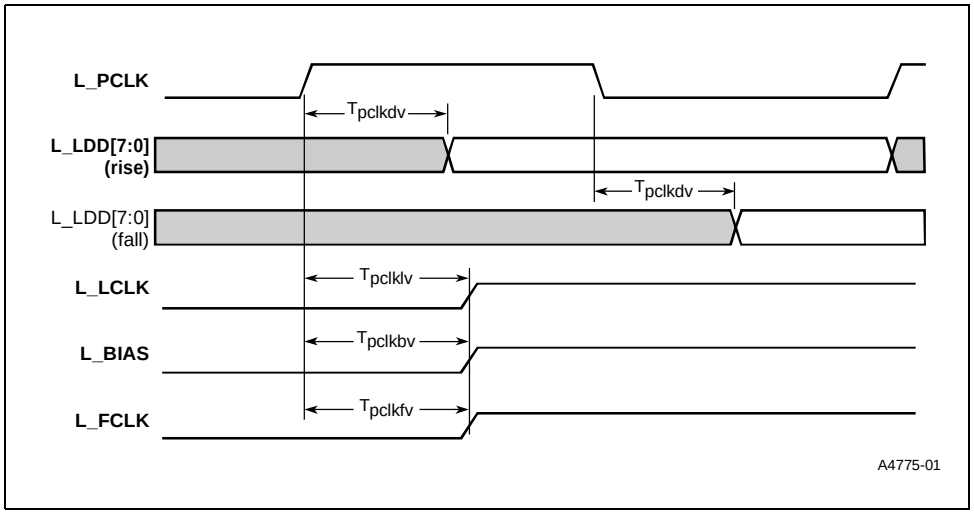


Table 21. LCD AC Timing Specifications

Symbol	Description	Min	Max	Units	Notes
Tpclkdv	L_PCLK rise/fall to L_LDD<7:0> driven valid		14	ns	1
Tpclklv	L_PCLK fall to L_LCLK driven valid		14	ns	2
Tpclkfv	L_PCLK fall to L_LFCLK driven valid		14	ns	2
Tpclkbv	L_PCLK rise to L_BIAS driven valid		14	ns	2

NOTES:
1. You can program the LCD data pins to be driven on either the rising or falling edge of the pixel clock (L_PCLK).
2. These LCD signals can, at times, transition when L_PCLK is not clocking (between frames). At this time, they are clocked with the internal version of the pixel clock before it is driven out onto the L_PCLK pin.

4.8.2 SSP Module AC Timing

Figure 9, “SSP AC Timing Definitions” on page 44 describes the SSP timing parameters. The SSP pin timing specifications are referenced to SCLK_C. Values for the parameters are given in Table 22, “SSP AC Timing Specifications” on page 44.

Figure 9. SSP AC Timing Definitions

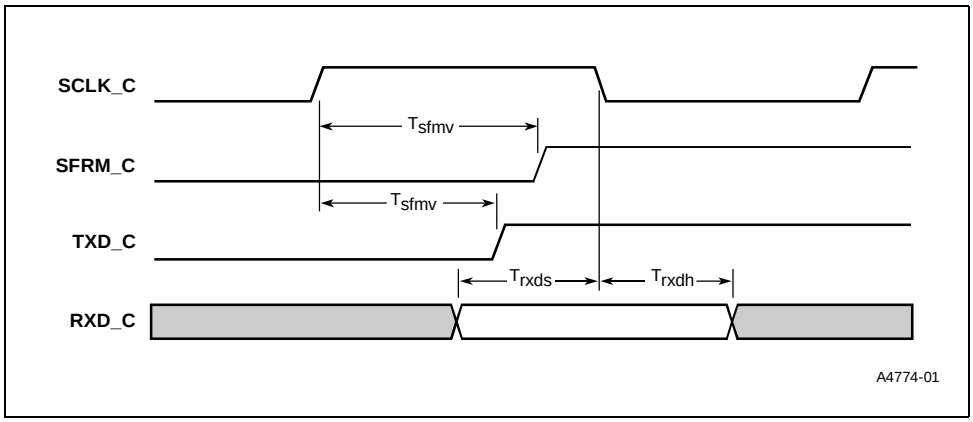


Table 22. SSP AC Timing Specifications

Symbol	Description	Min	Max	Units	Notes
Tsfmv	SCLK_C rise to SFRM_C driven valid		21	ns	
Trxds	RXD_C valid to SCLK_C fall (input setup)	11		ns	
Trxdh	SCLK_C fall to RXD_C invalid (input hold)	0		ns	
Tsfmv	SCLK_C rise to TXD_C valid		22	ns	

4.8.3 Boundary Scan Test Signal Timings

Boundary scan test signal timing is shown in Table 23, “Boundary Scan Test Signal Timing”.

Table 23. Boundary Scan Test Signal Timing (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Units	Notes
TBSF	TCK Frequency	0.0	33.33	MHz	
TBSCH	TCK High Time	15.0		ns	Measured at 1.5 V
TBSCL	TCK Low Time	15.0		ns	Measured at 1.5 V
TBSCR	TCK Rise Time		5.0	ns	0.8 V to 2.0 V
TBSCF	TCK Fall Time		5.0	ns	2.0 V to 0.8 V
TBSIS1	Input Setup to TCK TDI, TMS	4.0		ns	
TBSIH1	Input Hold from TCK TDI, TMS	6.0		ns	
TBSIS2	Input Setup to TCK nTRST	25.0		ns	
TBSIH2	Input Hold from TCK nTRST	3.0		ns	
TBSOV1	TDO Valid Delay	1.5	6.9	ns	Relative to falling edge of TCK
TOF1	TDO Float Delay	1.1	5.4	ns	Relative to falling edge of TCK
TOV12	All Outputs (Non-Test) Valid Delay	1.5	6.9	ns	Relative to falling edge of TCK

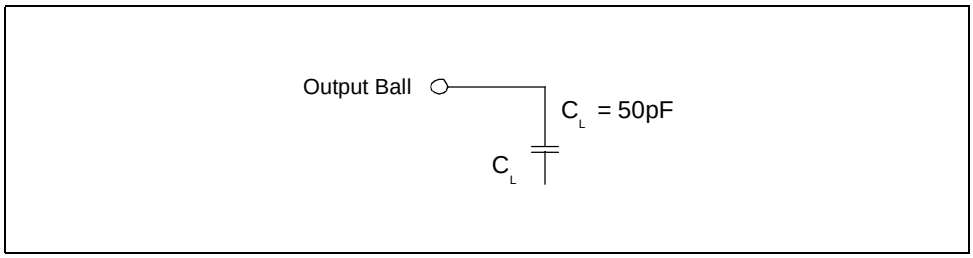
Table 23. Boundary Scan Test Signal Timing (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Units	Notes
TOF2	All Outputs (Non-Test) Float Delay	1.1	5.4	ns	Relative to falling edge of TCK
TIS10	Input Setup to TCK All Inputs (Non-Test)	4.0		ns	
TIH8	Input Hold from TCK All Inputs (Non-Test)	6.0		ns	

4.9 AC Test Conditions

The AC specifications in Section 4.4, “Targeted AC Specifications” on page 32 are tested with a 50 pF load indicated in Figure 10.

Figure 10. AC Test Load

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