Remote 8-bit I/O expander for Fm+ I²C-bus with interrupt

Features

- Operation power supply voltage from 2.3V to 5.5V
- 8-bit remote I/O pins that default to inputs at power-up
- 1 MHz I²C-bus interface
- Compliant with the I²C-bus Fast and Standard modes
- 5.5V tolerant I/Os
- SDA with 30 mA sink capability for 4000 pF buses
- Latched outputs with 25 mA sink capability for directly driving LEDs
- Total package sink capability of 200 mA
- Active LOW open-drain interrupt output
- Low standby current
- 64 programmable slave addresses using 3 address pins
- ESD protection (4KV HBM and 1KV CDM)
- Latch-up tested (exceeds 100mA)
- Offered in three different packages: SOIC-16,TSSOP-16 and TQFN 3x3-16

Description

The PI4IOE5V9674 provides general purpose remote I/O expansion for most microcontroller families via the two-line bidirectional bus (I²C-bus) and is a part of the Fast-mode Plus family.

The PI4IOE5V9674 provides higher Fast-mode Plus (Fm+) I²C-bus speeds (1 MHz versus 400 kHz) so that the output can support PWM dimming of LEDs, high I²C-bus drive (30 mA) so that many more devices can be on the bus without the need for bus buffers, high total package sink capacity (200 mA) that supports having all 25 mA LEDs on at the same time and more device addresses (64) are available to allow many more devices on the bus without address conflicts.

The device consists of a 8-bit quasi-bidirectional port and an I²C-bus interface. The PI4IOE5V9674 has a low current consumption and includes latched outputs with high current drive capability for directly driving LEDs.

It also possesses an interrupt line ($\overline{INT}$) which can be connected to the interrupt logic of the microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C-bus. The internal Power-On Reset (POR) or software reset sequence initializes the I/Os as inputs.

Pin Configuration

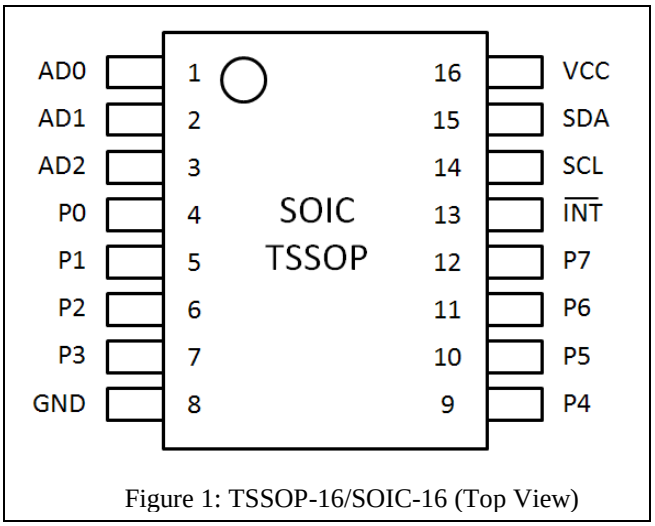


Figure 1: TSSOP-16/SOIC-16 (Top View)

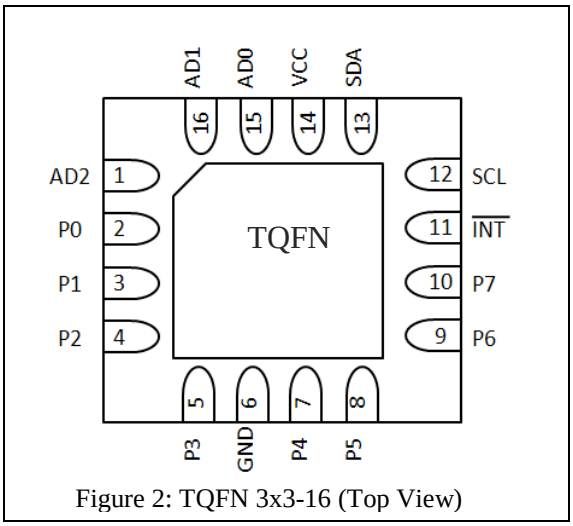


Figure 2: TQFN 3x3-16 (Top View)

Pin Description

Table 1: Pin Description

Pin		Name	Type	Description
SO24 TSSOP24	TQFN24			
1	15	AD0	I	Address input 0
2	16	AD1	I	Address input 1
3	1	AD2	I	Address input 2
4	2	P0	I/O	Port 0 input/output 0
5	3	P1	I/O	Port 0 input/output 1
6	4	P2	I/O	Port 0 input/output 2
7	5	P3	I/O	Port 0 input/output 3
8	6	GND	G	Ground
9	7	P4	I/O	Port 0 input/output 4
10	8	P5	I/O	Port 0 input/output 5
11	9	P6	I/O	Port 0 input/output 6
12	10	P7	I/O	Port 0 input/output 7
13	11	$\overline{INT}$	O	Interrupt input (open-drain)
14	12	SCL	I	Serial clock line input
15	13	SDA	I	Serial data line open-drain
16	14	VCC	P	Supply voltage

* I = Input; O = Output; P = Power; G = Ground

Maximum Ratings

Power supply	-0.5V to +6.0V
Voltage on an I/O pin	GND-0.5V to +6.0V
Input current	±20mA
Output current on an I/O pin	±50mA
Supply current	±160mA
Ground supply current	400mA
Total power dissipation	400mW
Operation temperature	-40~85℃
Storage temperature	-65~150℃
Maximum Junction temperature ,T j(max)	125℃

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Static characteristics

VCC = 2.3 V to 5.5 V; GND = 0 V; Tamb= -40 ℃ to +85 ℃; unless otherwise specified.

Table 2: Static characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power supply						
VCC	Supply voltage		2.3	-	5.5	V
I_{DD}	Supply current	Operating mode; no load; VI = VCC or GND; fSCL = 1 MHz; AD0, AD1, AD2 = static H or L	-	200	500	μA
I_{stb}	Standby current	Standby mode; VCC = 5.5 V; no load; VI = VCC; fSCL= 0 kHz; I/O = inputs	-	4.5	10	uA
V_{POR}	Power-on reset voltage[1]		-	1.16	1.41	V
Input SCL, input/output SDA						
V_{IL}	Low level input voltage		-0.5	-	+0.3VCC	V
V_{IH}	High level input voltage		0.7VCC	-	5.5	V
I_{OL}	Low level output current	V_{OL} = 0.4 V; V_{CC} = 2.3 V	20	35	-	mA
		V_{OL} = 0.4 V; V_{CC} = 3.0 V	25	44		
		V_{OL} = 0.4 V; V_{CC} = 4.5 V	30	57		
I_L	Leakage current	V_I=VCC=GND	-1	-	1	μA
C_i	Input capacitance	V_I =GND	-	5	10	pF

Continued

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I/Os						
VIL	LOW-level input voltage		-0.5		$0.3V_{CC}$	V
VIH	HIGH-level input voltage		$0.7V_{CC}$		5.5	V
I_{OL}	Low level output current	VCC = 2.3 V; V_{OL} = 0.5 V[2]	12	26		mA
		VCC =3.0V; V_{OL} = 0.5 V[2]	17	33		mA
		VCC =4.5V; V_{OL} = 0.5 V[2]	25	40		mA
I_{OL}(tot)	total LOW-level output current	VOL=0.5V;VCC=4.5V			200	mA
I_{OH}	HIGH-level output current	VOH = GND	-30	-359	-480	uA
Itrt(pu)	transient boosted pull-up current	VOH= GND	-0.5	-1.0		mA
C_i	Input capacitance	[3]	-	2.1	10	pF
C_o	Output capacitance	[3]	-	2.1	10	pF
Interrupt $\overline{INT}$						
I_{OL}	Low level output current	V_{OL}=0.4V	3.0	-	-	mA
C_o	Output capacitance			3	10	pF
Select inputs AD0,AD1,AD2						
V_{IL}	Low level input voltage		-0.5	-	+0.3VCC	V
V_{IH}	High level input voltage		0.7VCC	-	5.5	V
I_L	Input leakage current		-1		1	μA
Ci	input capacitance			3.5	10	pF

Note:
[1]: VCC must be lowered to 0.2 V for at least 20 us in order to reset part.
[2]: Each I/O must be externally limited to a maximum of 25 mA and the total package limited to 200 mA due to internal busing limits.
[3]: The value is not tested, but verified on sampling basis.

Dynamic Characteristics

Table 3: Dynamic characteristics

Symbol	Parameter	Standard mode I²C		Fast mode I²C		Fast mode Plus I²C		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	kHz
t_{BUF}	bus free time between a STOP and START condition	4.7	-	1.3	-	0.5		µs
$t_{HD;STA}$	hold time (repeated) START condition	4.0	-	0.6	-	0.26		µs
$t_{SU;STA}$	set-up time for a repeated START condition	4.7	-	0.6	-	0.26		µs
$t_{SU;STO}$	set-up time for STOP condition	4.0	-	0.6	-	0.26		µs
$t_{VD;ACK}$[1]	data valid acknowledge time	-	3.45	-	0.9	-	0.45	µs
$t_{HD;DAT}$[2]	data hold time	0	-	0	-	0		ns
$t_{VD;DAT}$	data valid time	-	3.45	-	0.9	-	0.45	ns
$t_{SU;DAT}$	data set-up time	250	-	100	-	50		ns
t_{LOW}	LOW period of the SCL clock	4.7	-	1.3	-	0.5		µs
t_{HIGH}	HIGH period of the SCL clock	4.0	-	0.6	-	0.26		µs
t_f	fall time of both SDA and SCL signals	-	300	-	300		120	ns
t_r	rise time of both SDA and SCL signals	-	1000	-	300		120	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter	-	50	-	50		50	ns
Port timing C_L≤100pF								
$t_{v(Q)}$	Data output valid time[3]		4		4		4	ns
$t_{su(D)}$	Data input set-up time	0		0		0		ns
$t_{h(D)}$	Data input hold time	4		4		4		µs
Interrupt timing C_L≤100pF								
$t_{v(INT)}$	Valid time on pin $\overline{INT}$	-	4	-	4		4	µs
$t_{rst(INT)}$	Reset time on pin $\overline{INT}$	-	4	-	4		4	µs

Note:
[1]: $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA (out) LOW.
[2]: $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.
[3]: $t_{v(Q)}$measured from 0.7VCC on SCL to 50% I/O output.

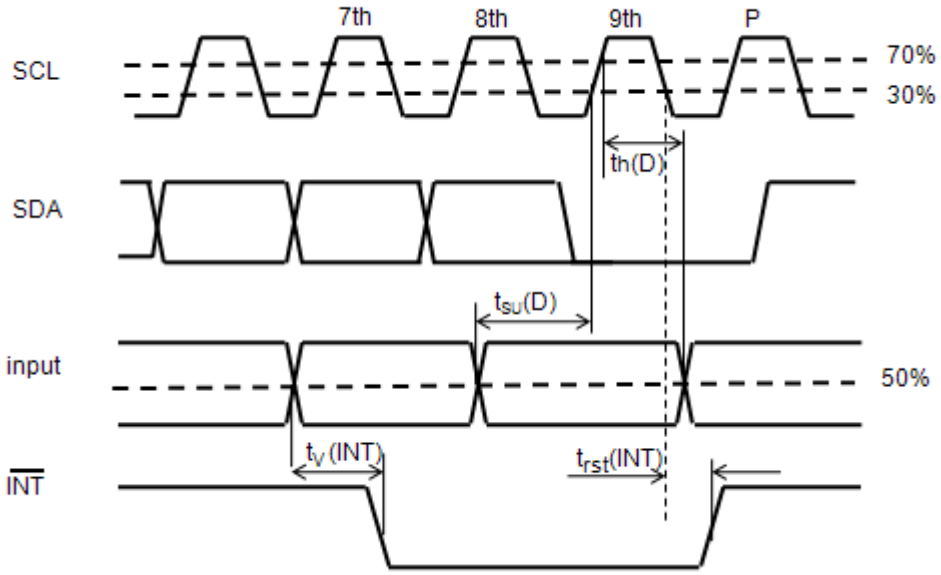
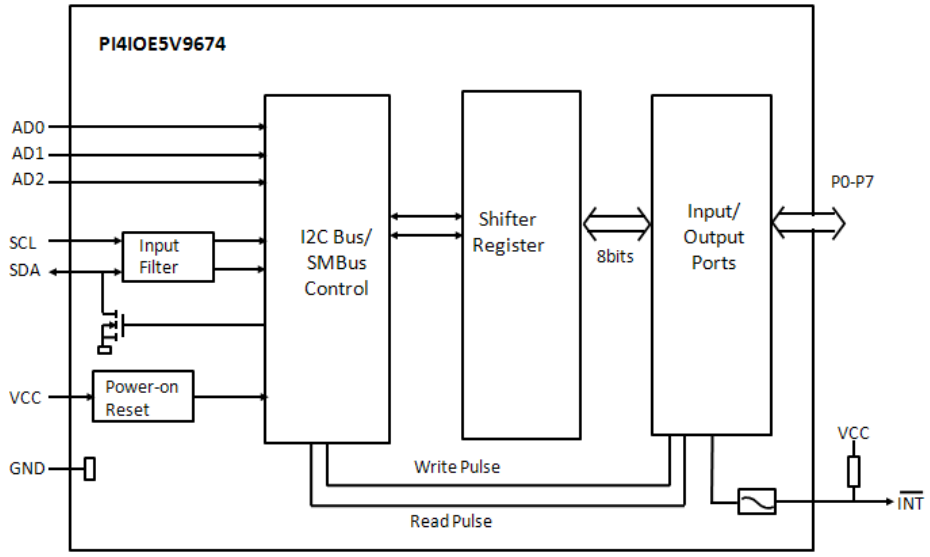


Figure 3: timing parameters for INT signal

PI4IOE5V9674 Block Diagram

Figure 4: Block diagram



Note: All I/Os are set to inputs at reset.

Details Description

a. Device address

Following a START condition, the bus master must send the address of the slave it is accessing and the operation it wants to perform (read or write). The address of the PI4IOE5V9674 is shown in bellow. Slave address pins AD2, AD1, and AD0 choose 1 of 64 slave addresses. To conserve power, no internal pull-up resistors are incorporated on AD2, AD1, and AD0. Address values depending on AD2, AD1, and AD0 can be found in Table "PI4IOE5V9674 address map".

Remark: The General Call address (0000 0000b) and the Device ID address (1111 100Xb) are reserved and cannot be used as device address. Failure to follow this requirement will cause the PI4IOE5V9674 not to acknowledge.

Remark: Reserved I²C-bus addresses must be used with caution since they can interfere with:

- "reserved for future use" I²C-bus addresses (0000 011, 1111 101, 1111 110, 1111 111)
- slave devices that use the 10-bit addressing scheme (1111 0xx)
- High speed mode (Hs-mode) master code (0000 1xx)

PI4IOE5V9674 address

	b7(MSB)	b6	b5	b4	b3	b2	b1	b0
Address Byte	A6	A5	A4	A3	A2	A1	A0	R/W

The last bit of the first byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

PI4IOE5V9674 Address maps

AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	Address (Write)	Address (Read)
GND	SCL	GND	0	0	1	0	0	0	0	20h	21h
GND	SCL	VCC	0	0	1	0	0	0	1	22h	23h
GND	SDA	GND	0	0	1	0	0	1	0	24h	25h
GND	SDA	VCC	0	0	1	0	0	1	1	26h	27h
VCC	SCL	GND	0	0	1	0	1	0	0	28h	29h
VCC	SCL	VCC	0	0	1	0	1	0	1	2Ah	2Bh
VCC	SDA	GND	0	0	1	0	1	1	0	2Ch	2Dh
VCC	SDA	VCC	0	0	1	0	1	1	1	2Eh	2Fh
GND	SCL	SCL	0	0	1	1	0	0	0	30h	31h
GND	SCL	SDA	0	0	1	1	0	0	1	32h	33h
GND	SDA	SCL	0	0	1	1	0	1	0	34h	35h
GND	SDA	SDA	0	0	1	1	0	1	1	36h	37h
VCC	SCL	SCL	0	0	1	1	1	0	0	38h	39h
VCC	SCL	SDA	0	0	1	1	1	0	1	3Ah	3Bh
VCC	SDA	SCL	0	0	1	1	1	1	0	3Ch	3Dh
VCC	SDA	SDA	0	0	1	1	1	1	1	3Eh	3Fh
GND	GND	GND	0	1	0	0	0	0	0	40h	41h
GND	GND	VCC	0	1	0	0	0	0	1	42h	43h
GND	VCC	GND	0	1	0	0	0	1	0	44h	45h
GND	VCC	VCC	0	1	0	0	0	1	1	46h	47h
VCC	GND	GND	0	1	0	0	1	0	0	48h	49h
VCC	GND	VCC	0	1	0	0	1	0	1	4Ah	4Bh
VCC	VCC	GND	0	1	0	0	1	1	0	4Ch	4Dh
VCC	VCC	VCC	0	1	0	0	1	1	1	4Eh	4Fh
GND	GND	SCL	0	1	0	1	0	0	0	50h	51h
GND	GND	SDA	0	1	0	1	0	0	1	52h	53h
GND	VCC	SCL	0	1	0	1	0	1	0	54h	55h
GND	VCC	SDA	0	1	0	1	0	1	1	56h	57h
VCC	GND	SCL	0	1	0	1	1	0	0	58h	59h
VCC	GND	SDA	0	1	0	1	1	0	1	5Ah	5Bh
VCC	VCC	SCL	0	1	0	1	1	1	0	5Ch	5Dh
VCC	VCC	SDA	0	1	0	1	1	1	1	5Eh	5Fh

PI4IOE5V9674 Address maps

AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	Address (Write)	Address (Read)
SCL	SCL	GND	1	0	1	0	0	0	0	A0h	A1h
SCL	SCL	VCC	1	0	1	0	0	0	1	A2h	A3h
SCL	SDA	GND	1	0	1	0	0	1	0	A4h	A5h
SCL	SDA	VCC	1	0	1	0	0	1	1	A6h	A7h
SDA	SCL	GND	1	0	1	0	1	0	0	A8h	A9h
SDA	SCL	VCC	1	0	1	0	1	0	1	AAh	ABh
SDA	SDA	GND	1	0	1	0	1	1	0	ACh	ADh
SDA	SDA	VCC	1	0	1	0	1	1	1	AEh	AFh
SCL	SCL	SCL	1	0	1	1	0	0	0	B0h	B1h
SCL	SCL	SDA	1	0	1	1	0	0	1	B2h	B3h
SCL	SDA	SCL	1	0	1	1	0	1	0	B4h	B5h
SCL	SDA	SDA	1	0	1	1	0	1	1	B6h	B7h
SDA	SCL	SCL	1	0	1	1	1	0	0	B8h	B9h
SDA	SCL	SDA	1	0	1	1	1	0	1	BAh	BBh
SDA	SDA	SCL	1	0	1	1	1	1	0	BCh	BDh
SDA	SDA	SDA	1	0	1	1	1	1	1	BEh	BFh
SCL	GND	GND	1	1	0	0	0	0	0	C0h	C1h
SCL	GND	VCC	1	1	0	0	0	0	1	C2h	C3h
SCL	VCC	GND	1	1	0	0	0	1	0	C4h	C5h
SCL	VCC	VCC	1	1	0	0	0	1	1	C6h	C7h
SDA	GND	GND	1	1	0	0	1	0	0	C8h	C9h
SDA	GND	VCC	1	1	0	0	1	0	1	CAh	CBh
SDA	VCC	GND	1	1	0	0	1	1	0	CCh	CDh
SDA	VCC	VCC	1	1	0	0	1	1	1	CEh	CFh
SCL	GND	SCL	1	1	1	0	0	0	0	E0h	E1h
SCL	GND	SDA	1	1	1	0	0	0	1	E2h	E3h
SCL	VCC	SCL	1	1	1	0	0	1	0	E4h	E5h
SCL	VCC	SDA	1	1	1	0	0	1	1	E6h	E7h
SDA	GND	SCL	1	1	1	0	1	0	0	E8h	E9h
SDA	GND	SDA	1	1	1	0	1	0	1	EAh	EBh
SDA	VCC	SCL	1	1	1	0	1	1	0	ECh	EDh
SDA	VCC	SDA	1	1	1	0	1	1	1	EEh	EFh

Software Reset call addresses

- General Call address: allows to reset the PI4IOE5V9675 through the I²C-bus upon reception of the right I²C-bus sequence.

	b7(MSB)	b6	b5	b4	b3	b2	b1	b0
General Call Address	0	1	0	0	1	0	0	R/W

Software Reset

The Software Reset Call allows all the devices in the I²C-bus to be reset to the power-up state value through a specific formatted I²C-bus command. To be performed correctly, it implies that the I²C-bus is functional and that there is no device hanging the bus.

The Software Reset sequence is defined as following:

1. A START command is sent by the I²C-bus master.
2. The reserved General Call I²C-bus address '0000 000' with the R/W bit set to 0 (write) is sent by the I²C-bus master.
3. The device acknowledges after seeing the General Call address '0000 0000' (00h) only. If the R/W bit is set to 1 (read), no acknowledge is returned to the I2C-bus master.
4. Once the General Call address has been sent and acknowledged, the master sends 1 byte. The value of the byte must be equal to 06h.
   a. The device acknowledges this value only. If the byte is not equal to 06h, the device does not acknowledge it.
   b. If more than 1 byte of data is sent, the device does not acknowledge any more.
5. Once the right byte has been sent and correctly acknowledged, the master sends a STOP command to end the Software Reset sequence: the device then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time. If the master sends a Repeated START instead, no reset is performed.

The I²C-bus master must interpret a non-acknowledge from the device (at any time) as a 'Software Reset Abort'. The device does not initiate a reset of its registers.

The unique sequence that initiates a Software Reset is described in Figure 5.

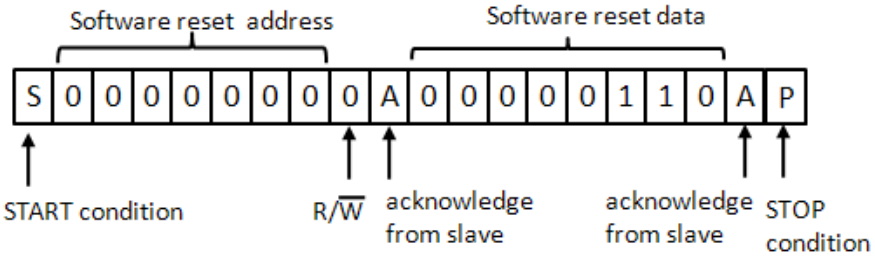


Figure 5: Software Reset sequence

Quasi-bidirectional I/O architecture

A quasi-bidirectional I/O is an input or output port without using a direction control register. Whenever the master reads the register, the value returned to master depends on the actual voltage or status of the pin. At power-on, all the ports are HIGH with a weak 100 uA internal pull-up to VCC, but can be driven LOW by an internal transistor, or an external signal. The I/O ports are entirely independent of each other, but each I/O octal is controlled by the same read or write data byte.

Advantages of the quasi-bidirectional I/O over totem pole I/O include:

- Better for driving LEDs since the p-channel (transistor to VCC) is small, which saves die size and therefore cost. LED drive only requires an internal transistor to ground, while the LED is connected to VCC through a current-limiting resistor. Totem pole I/O have both n-channel and p-channel transistors, which allow solid HIGH and LOW output levels without a pull-up resistor —

good for logic levels.

• Simpler architecture — only a single register and the I/O can be both input and output at the same time. Totem pole I/O have a direction register that specifies the port pin direction and it is always in that configuration unless the direction is explicitly changed.

• Does not require a command byte. The simplicity of one register (no need for the pointer register or, technically, the command byte) is an advantage in some embedded systems where every byte counts because of memory or bandwidth limitations.

There is only one register to control four possibilities of the port pin: Input HIGH, input LOW, output HIGH, or output LOW.

Input HIGH: The master needs to write 1 to the register to set the port as an input mode if the device is not in the default power-on condition. The master reads the register to check the input status. If the external source pulls the port pin up to VCC or drives logic 1, then the master will read the value of 1.

Input LOW: The master needs to write 1 to the register to set the port to input mode if the device is not in the default power-on condition. The master reads the register to check the input status. If the external source pulls the port pin down to GND or drives logic 0, which sinks the weak 100 uA current source, then the master will read the value of 0.

Output HIGH: The master writes 1 to the register. There is an additional 'accelerator' or strong pull-up current when the master sets the port HIGH. The additional strong pull-up is only active during the HIGH time of the acknowledge clock cycle. This accelerator current helps the port's 100 uA current source make a faster rising edge into a heavily loaded output, but only at the start of the acknowledge clock cycle to avoid bus contention if an external signal is pulling the port LOW to GND/driving the port with logic 0 at the same time. After the half clock cycle there is only the 100uA current source to hold the port HIGH.

Output LOW: The master writes 0 to the register. There is a strong current sink transistor that holds the port pin LOW. A large current may flow into the port, which could potentially damage the part if the master writes a 0 to the register and an external source is pulling the port HIGH at the same time.

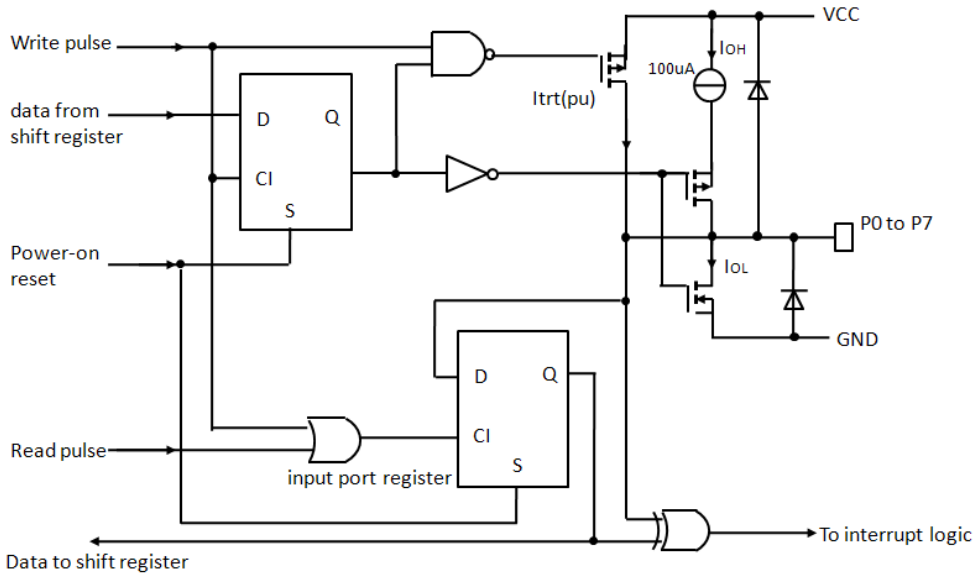


Figure 6.Simplified schematic diagram of P0 to P7

Writing to the port (Output mode)

The master (microcontroller) sends the START condition and slave address setting the last bit of the address byte to logic 0 for the write mode. The PI4IOE5V9674 acknowledges and the master then sends the data byte for P7 to P0 to the port register. As the clock line goes HIGH, the 8-bit data is presented on the port lines after it has been acknowledged by the PI4IOE5V9674. If a LOW is written, the strong pull-down turns on and stays on. If a HIGH is written, the strong pull-up turns on for 1⁄2 of the clock cycle, then the line is held HIGH by the weak current source. The master can then send a STOP or ReSTART condition or continue sending data. The number of data bytes that can be sent successively is not limited and the previous data is overwritten every time a data byte has been sent and acknowledged. Ensure a logic 1 is written for any port that is being used as an input to ensure the strong external pull-down is turned off.

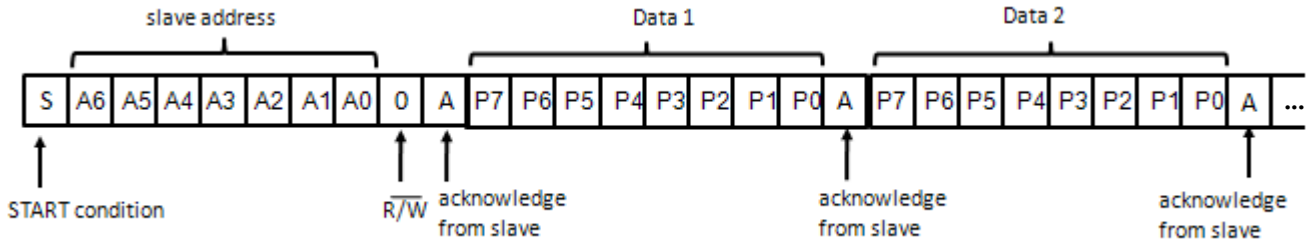


Figure 7. Write Mode

Reading from a port (Input mode)

The port must have been previously written to logic 1, which is the condition after power-on reset or software reset. To enter the Read mode the master (microcontroller) addresses the slave device and sets the last bit of the address byte to logic 1 (address byte read). The slave will acknowledge and then send the data byte to the master. The master will NACK and then send the STOP condition or ACK and read the input register again.

The read of any pin being used as an output will indicate HIGH or LOW depending on the actual state of the pin. If the data on the input port changes faster than the master can read, this data may be lost.

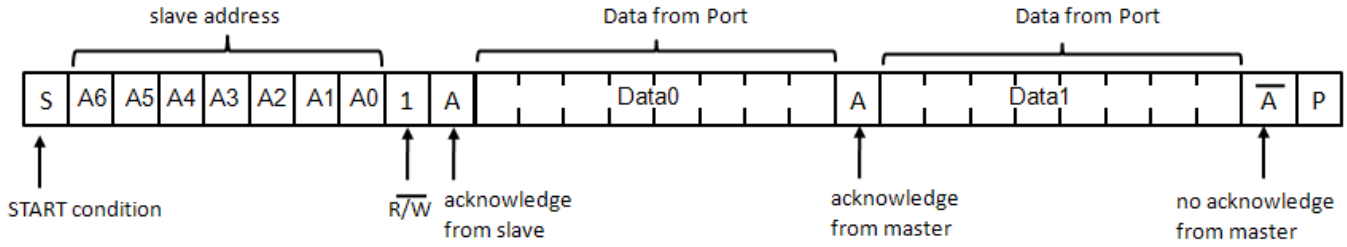


Figure 8.Read input port register

Power-on reset

When power is applied to VCC, an internal Power-On Reset (POR) holds the PI4IOE5V9674 in a reset condition until VCC has reached VPOR. At that point, the reset condition is released and the PI4IOE5V9674 registers and I²C-bus/SMBus state machine will initialize to their default states of all I/O inputs with weak current source to VCC. Thereafter VCC must be lowered below VPOR and back up to the operation voltage for power-on reset cycle.

Interrupt output ($\overline{INT}$)

The PI4IOE5V9674 provides an open-drain interrupt ($\overline{INT}$) which can be fed to a corresponding input of the microcontroller. This gives these chips a kind of master function which can initiate an action elsewhere in the system.

An interrupt is generated by any rising or falling edge of the port inputs. After time $t_{(V)D}$ the signal $\overline{INT}$ is valid.

The interrupt disappears when data on the port is changed to the original setting or data is read from or written to the device which has generated the interrupt.

In the write mode, the interrupt may become deactivated (HIGH) on the rising edge of the write to port pulse. On the falling edge of the write to port pulse the interrupt is definitely deactivated (HIGH).

The interrupt is reset in the read mode on the rising edge of the read from port pulse.

During the resetting of the interrupt itself, any changes on the I/Os may not generate an interrupt. After the interrupt is reset any change in I/Os will be detected and transmitted as an $\overline{INT}$.

At power-on reset all ports are in Input mode and the initial state of the ports is HIGH, therefore, for any port pin that is pulled LOW or driven LOW by external source, the interrupt output will be active (output LOW).

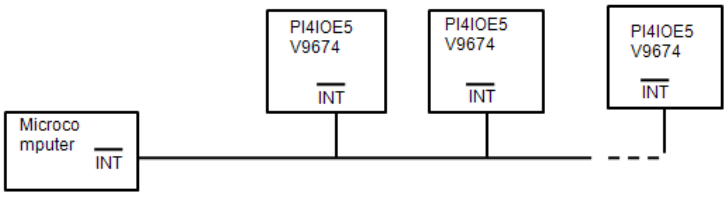


Figure 9. Application of multiple PI4IOE5V9674s with interrupt

Bidirectional I/O expander applications

In the 8-bit I/O expander application shown in Figure 10, P0 and P1 are inputs, and P2 to P7 are outputs. When used in this configuration, during a write, the input (P0 and P1) must be written as HIGH so the external devices fully control the input ports.

The desired HIGH or LOW logic levels may be written to the ports used as outputs (P2 to P7). If 10 uA internal output HIGH is not enough current source, the port needs external pull-up resistor. During a read, the logic levels of the external devices driving the input ports (P0 and P1) and the previous written logic level to the output ports (P2 to P7) will be read.

The GPIO also has an interrupt line ($\overline{INT}$) that can be connected to the interrupt logic of the microcontroller. By sending an interrupt signal on this line, the remote I/O informs the microprocessor that there has been a change of data on its ports without having to communicate via the I²C-bus.

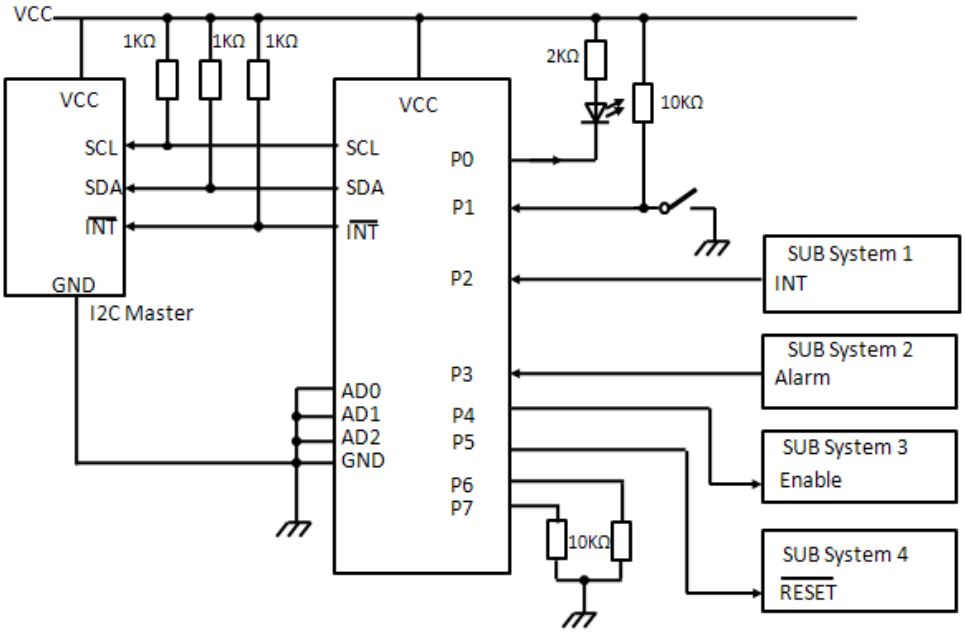


Figure 10. Bidirectional I/O expander application

High current-drive load applications

The GPIO has a maximum sinking current of 25 mA per bit. In applications requiring additional drive, two port pins in the same octal may be connected together to sink up to 50 mA current. Both bits must then always be turned on or off together. Up to 8 pins (one octal) can be connected together to drive 200 mA.

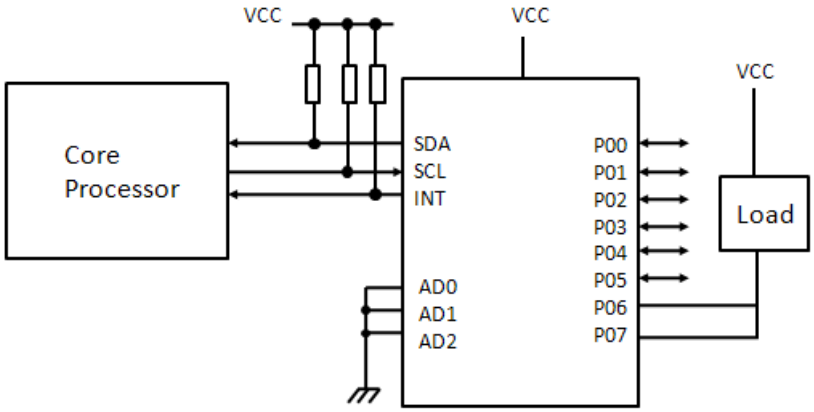
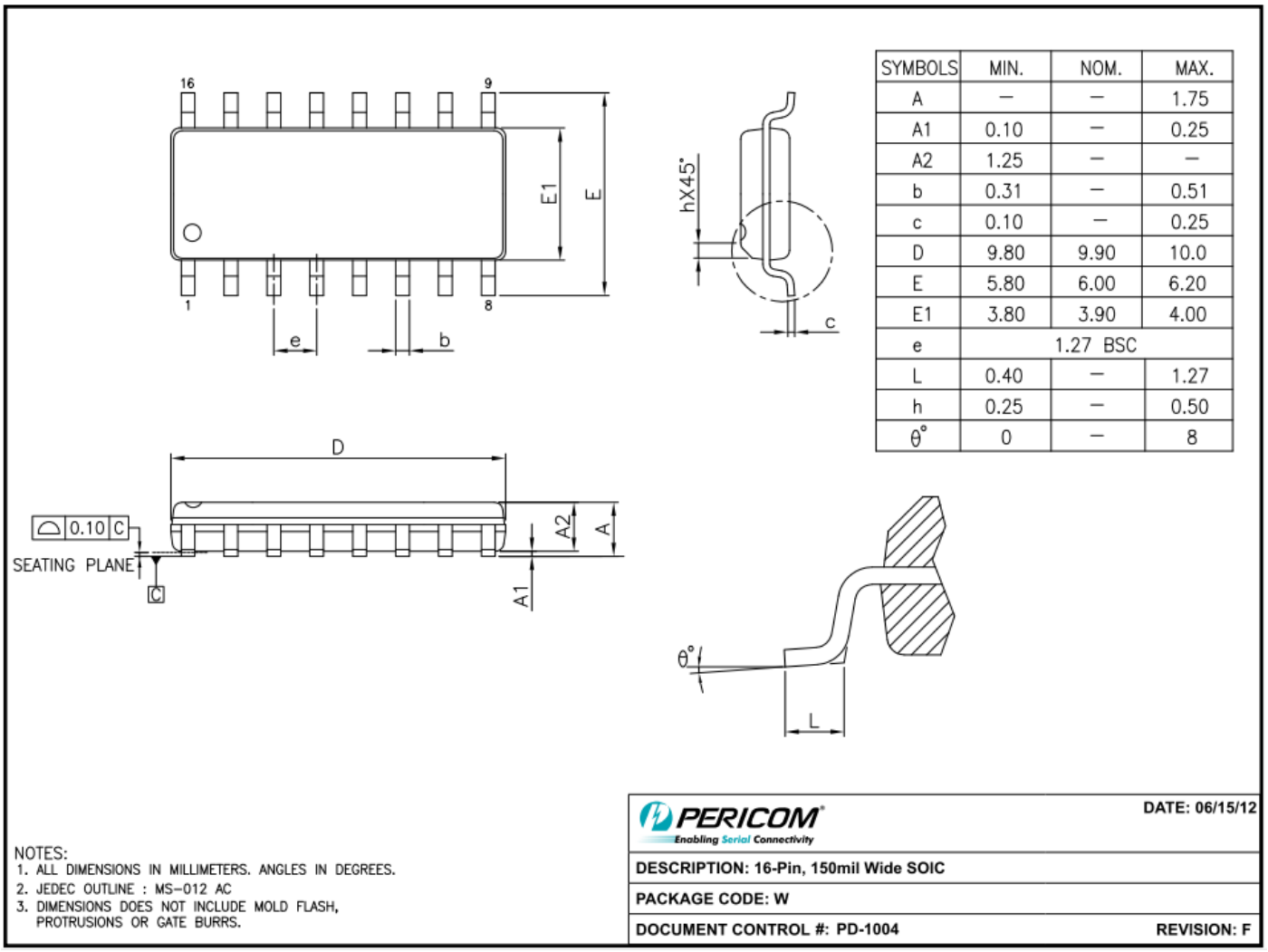


Figure 11. High current-drive load application

Mechanical Information

SOIC-16(W)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	9.80	9.90	10.0
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27 BSC	
L	0.40	–	1.27
h	0.25	–	0.50
θ°	0	–	8

NOTES:
1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.
2. JEDEC OUTLINE : MS-012 AC
3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

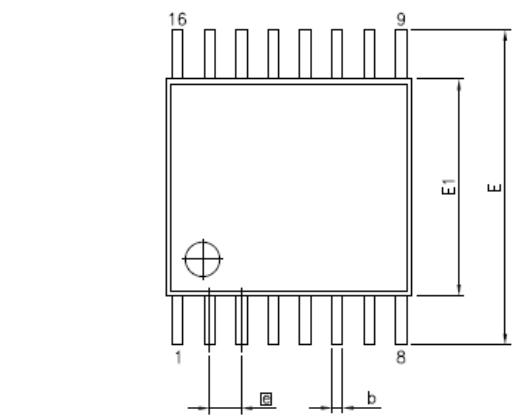
PERICOM Enabling Serial Connectivity — DATE: 06/15/12

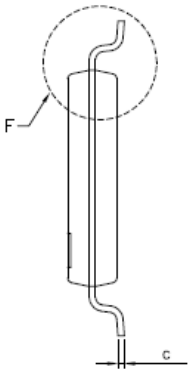
DESCRIPTION: 16-Pin, 150mil Wide SOIC

PACKAGE CODE: W

DOCUMENT CONTROL #: PD-1004 — REVISION: F

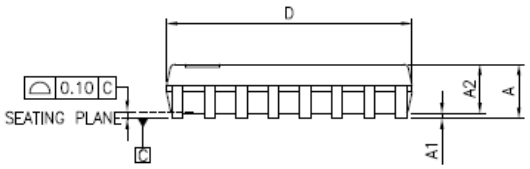
TSSOP-16(L)

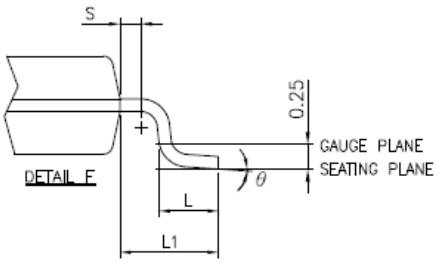




VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	–	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°





Notes:
1. Refer JEDEC MO-153F/AB
2. Controlling dimensions in millimeters
3. Package outline exclusive of mold flash and metal burr

PERICOM Enabling Serial Connectivity

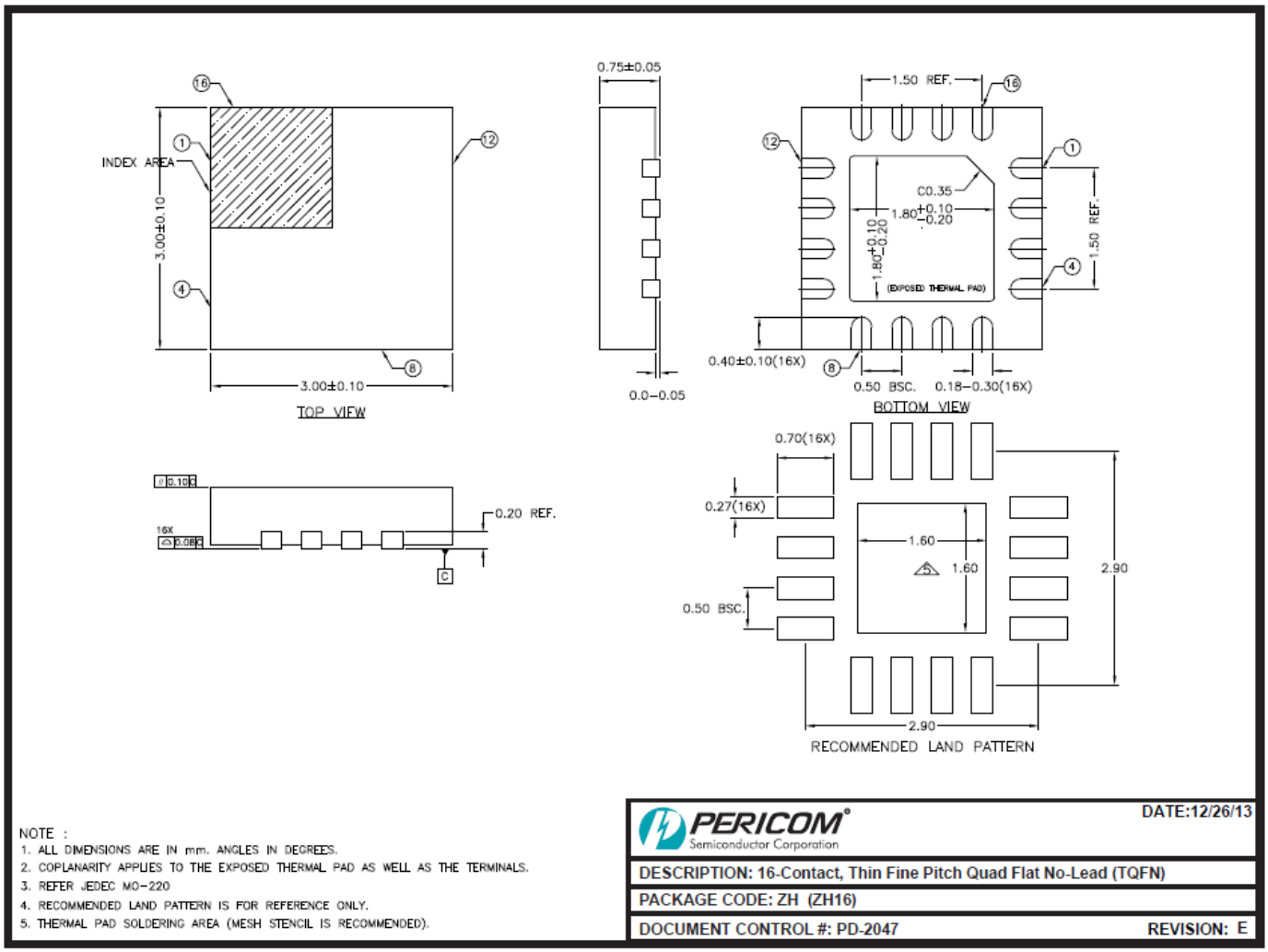
DATE: 05/03/12

DESCRIPTION: 16-Pin, 173mil Wide TSSOP

PACKAGE CODE: L

DOCUMENT CONTROL #: PD-1310 REVISION: F

TQFN 3x3-16(ZH)



Ordering Information

Part No.	Package Code	Package
PI4IOE5V9674WE	W	16-Pin,150 mil Wide SOIC
PI4IOE5V9674WEX	W	16-Pin,150 mil Wide SOIC, Tape & Reel
PI4IOE5V9674LE	L	16-Pin,173 mil Wide TSSOP
PI4IOE5V9674LEX	L	16-Pin,173 mil Wide TSSOP, Tape & Reel
PI4IOE5V9674ZHEX	ZH	16-Pin,TQFN,3.0x3.0, Tape & Reel

Note:

- E = Pb-free and Green
- Adding X Suffix= Tape/Reel