PD- 95666

International
IOR Rectifier

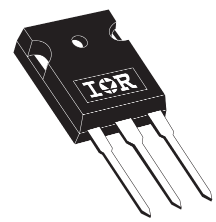
SMPS MOSFET IRFPC50APbF

HEXFET® Power MOSFET

V_{DSS}	Rds(on) max	I_D
600V	**0.58Ω**	**11A**

Applications
- Switch Mode Power Supply (SMPS)
- Uninterruptable Power Supply
- High speed power switching
- Lead-Free

Benefits
- Low Gate Charge Qg results in Simple Drive Requirement
- Improved Gate, Avalanche and dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective Coss specified (See AN 1001)



TO-247AC G D S

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	11	
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	7.0	A
I_{DM}	Pulsed Drain Current ①	44	
P_D @T_C = 25°C	Power Dissipation	180	W
	Linear Derating Factor	1.4	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	4.9	V/ns
T_J	Operating Junction and	-55 to + 150	
T_{STG}	Storage Temperature Range		°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torqe, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Typical SMPS Topology:

- PFC Boost

Notes ① through ⑤ are on page 8

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	600	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.65	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	0.58	Ω	V_{GS} = 10V, I_D = 6.0A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{DSS}	Drain-to-Source Leakage Current	——	——	25	μA	V_{DS} = 600V, V_{GS} = 0V
		——	——	250		V_{DS} = 480V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -30V

Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	7.7	——	——	S	V_{DS} = 50V, I_D = 6.0A
Q_g	Total Gate Charge	——	——	70	nC	I_D = 11A
Q_{gs}	Gate-to-Source Charge	——	——	19		V_{DS} = 480V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	——	28		V_{GS} = 10V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	——	15	——	ns	V_{DD} = 300V
t_r	Rise Time	——	40	——		I_D = 11A
$t_{d(off)}$	Turn-Off Delay Time	——	33	——		R_G = 6.2Ω
t_f	Fall Time	——	29	——		R_D = 30Ω,See Fig. 10 ④
C_{iss}	Input Capacitance	——	2100	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	270	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	9.7	——		ƒ = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	——	2830	——		V_{GS} = 0V, V_{DS} = 1.0V, ƒ = 1.0MHz
C_{oss}	Output Capacitance	——	74	——		V_{GS} = 0V, V_{DS} = 480V, ƒ = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	——	81	——		V_{GS} = 0V, V_{DS} = 0V to 480V ⑤

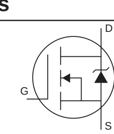
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	——	920	mJ
I_{AR}	Avalanche Current①	——	11	A
E_{AR}	Repetitive Avalanche Energy①	——	18	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.65	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	——	
$R_{\theta JA}$	Junction-to-Ambient	——	40	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	11	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	44		
V_{SD}	Diode Forward Voltage	——	——	1.4	V	T_J = 25°C, I_S = 11A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	500	740	ns	T_J = 25°C, I_F = 11A
Q_{rr}	Reverse RecoveryCharge	——	4.0	6.0	μC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

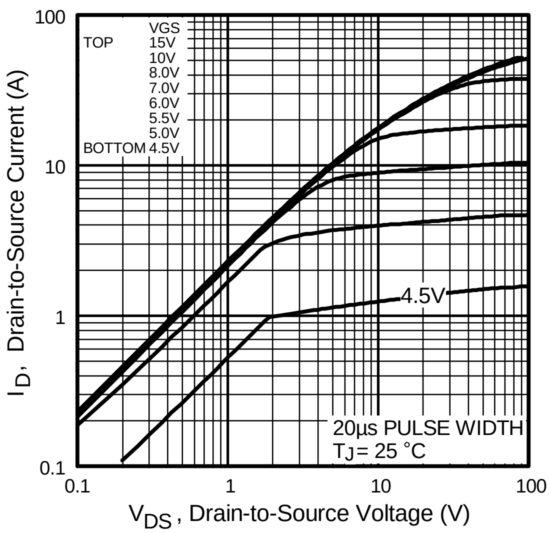


Fig 1. Typical Output Characteristics

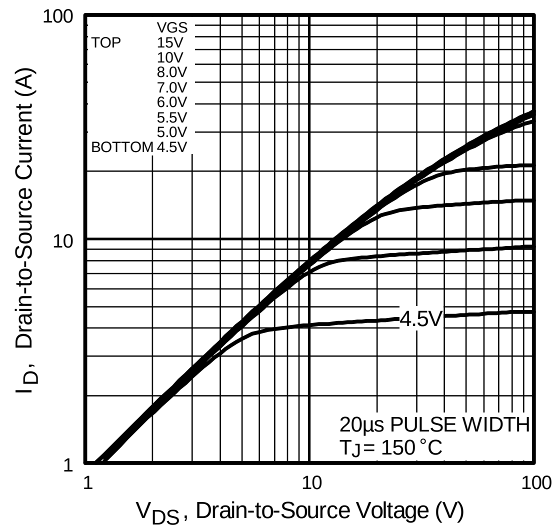


Fig 2. Typical Output Characteristics

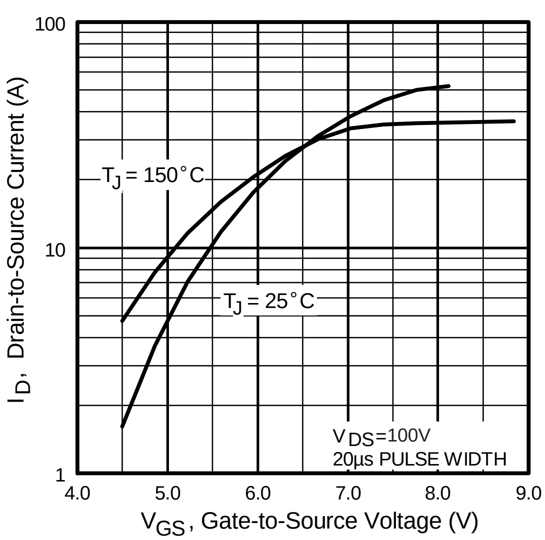


Fig 3. Typical Transfer Characteristics

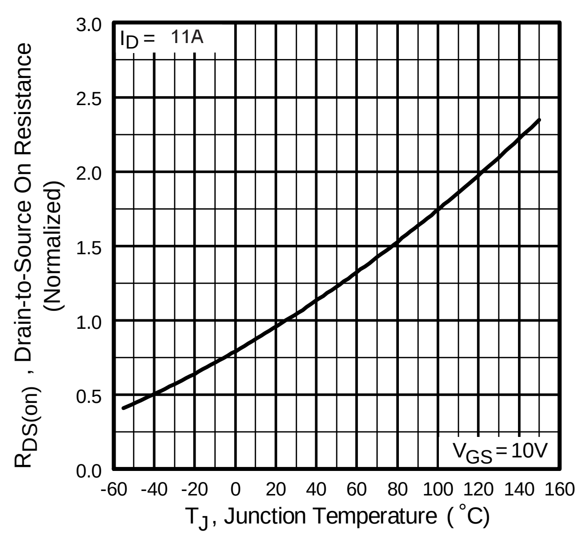


Fig 4. Normalized On-Resistance Vs. Temperature

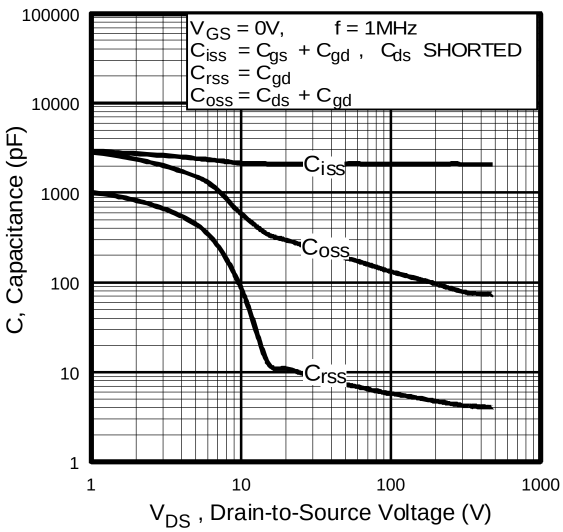


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

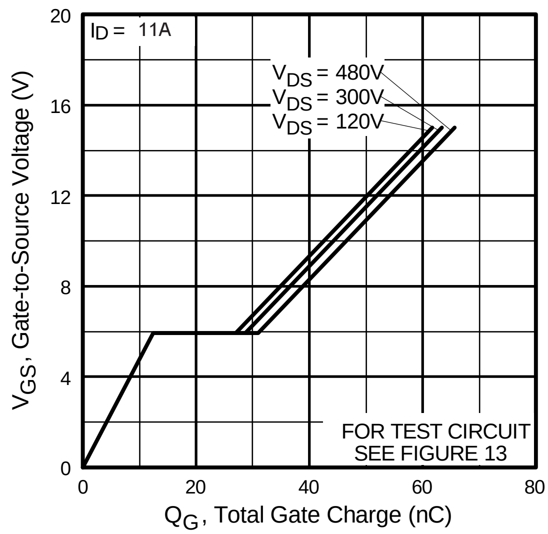


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

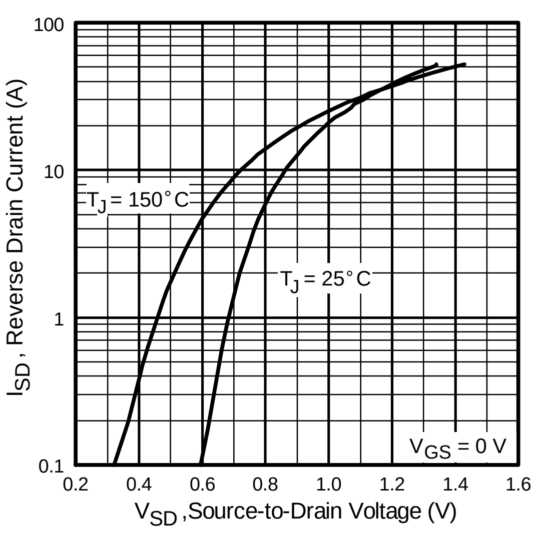


Fig 7. Typical Source-Drain Diode Forward Voltage

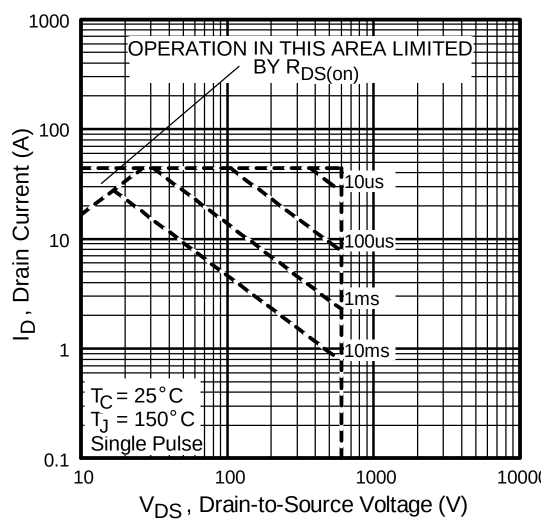


Fig 8. Maximum Safe Operating Area

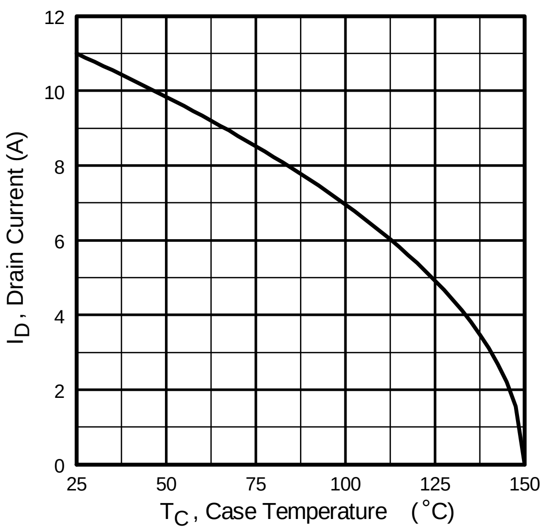


Fig 9. Maximum Drain Current Vs. Case Temperature

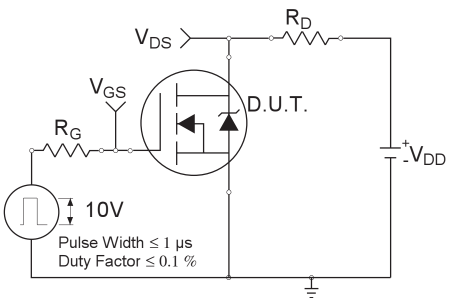


Fig 10a. Switching Time Test Circuit

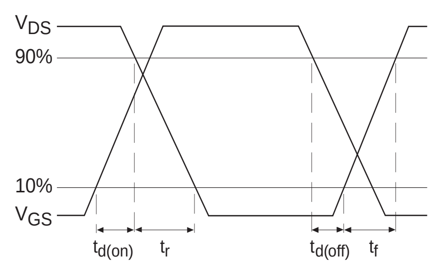


Fig 10b. Switching Time Waveforms

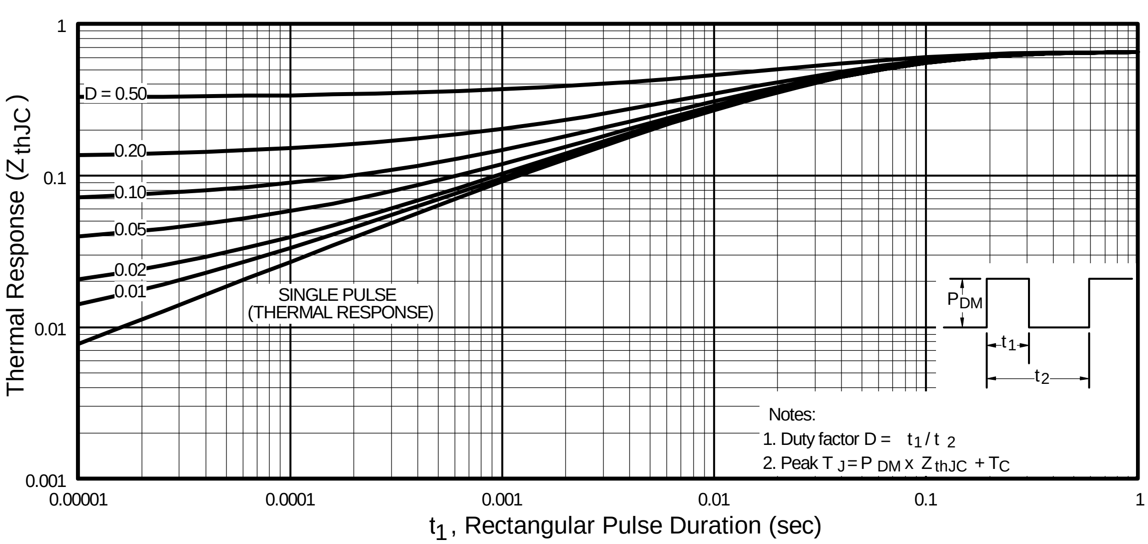


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

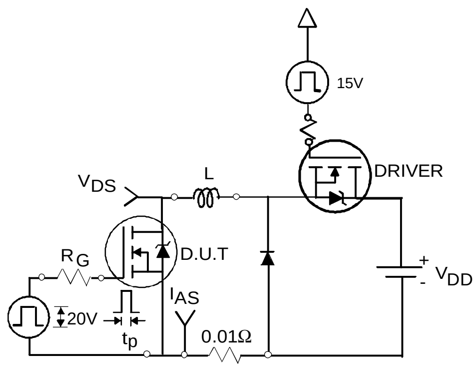


Fig 12a. Unclamped Inductive Test Circuit

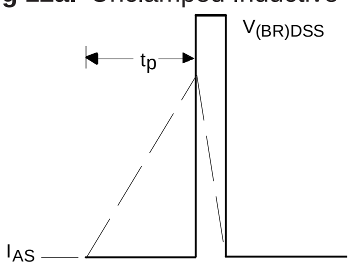


Fig 12b. Unclamped Inductive Waveforms

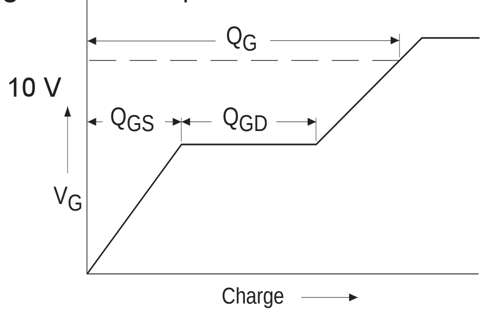


Fig 13a. Basic Gate Charge Waveform

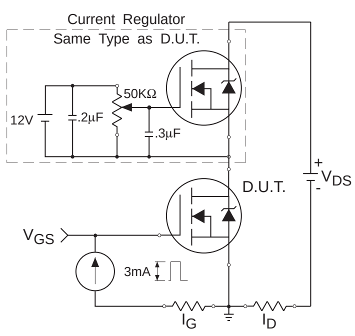


Fig 13b. Gate Charge Test Circuit

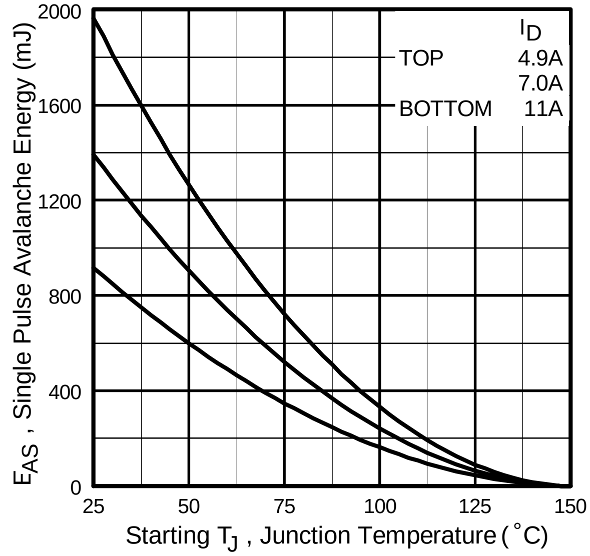


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

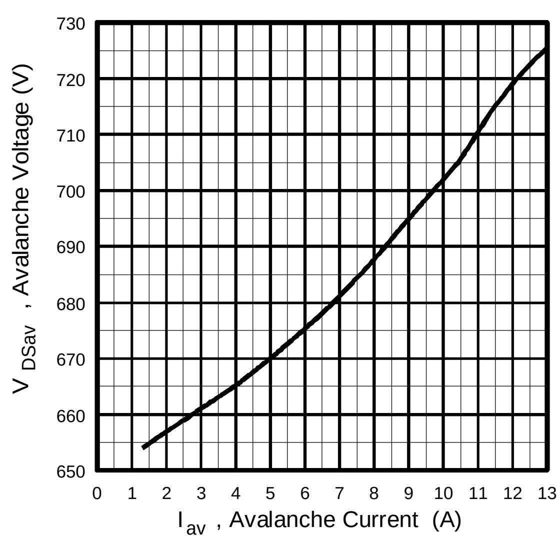
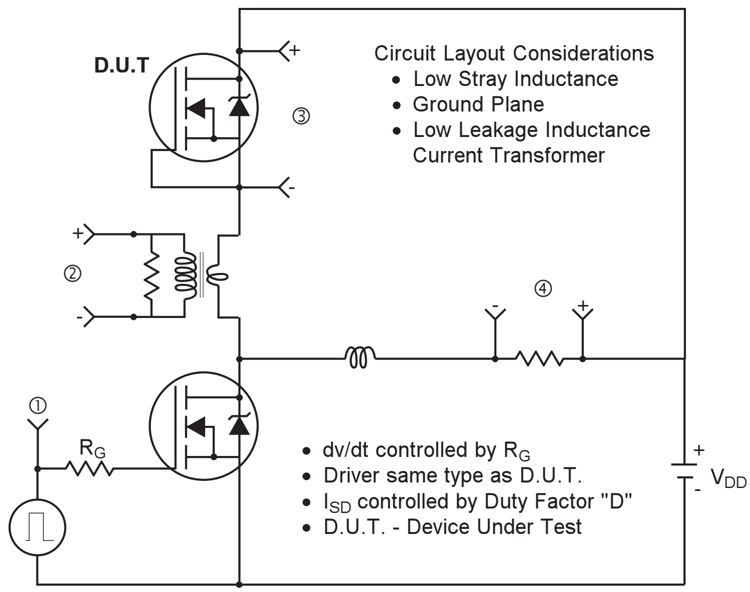
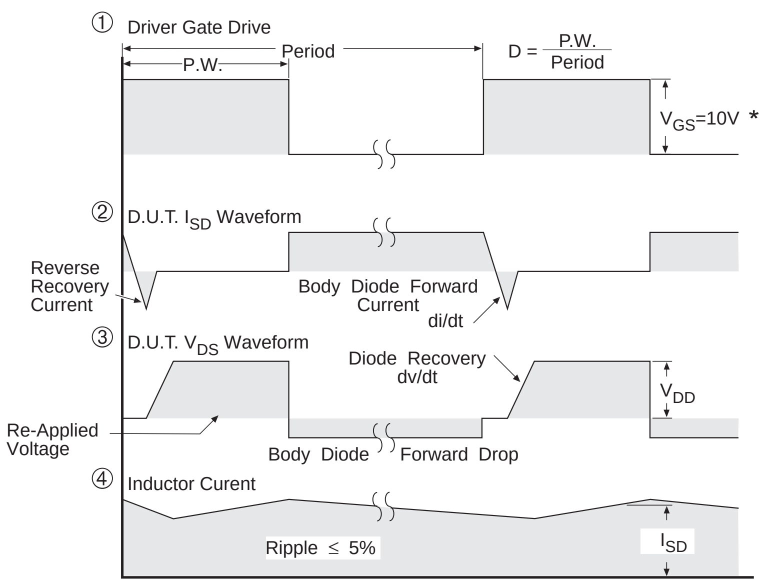


Fig 12d. Typical Drain-to-Source Voltage Vs. Avalanche Current

Peak Diode Recovery dv/dt Test Circuit

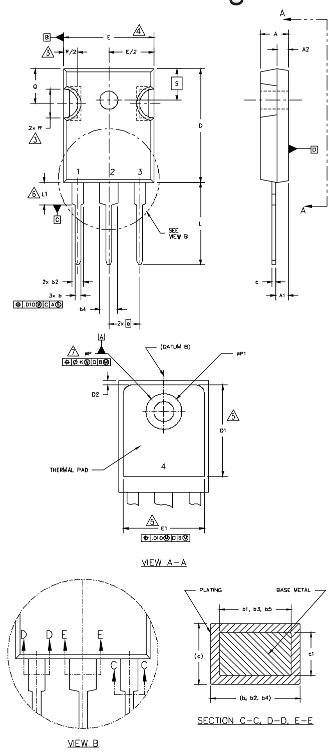




* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFETS

TO-247AC Package Outline Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
3. (△) CONTOUR OF SLOT OPTIONAL.
4. (△) DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. (△) THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENISONS D1 & E1.
6. (△) LEAD FINISH UNCONTROLLED IN L1.
7. (△) øP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154" [3.91].
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247 WITH THE EXCEPTION OF DIMENSION c.

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.37	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.034	0.38	0.86	
c1	.015	.030	0.38	0.76	
D	.776	.815	19.71	20.70	4
D1	.515	–	13.08	–	5
D2	.020	.030	0.51	0.76	
E	.602	.625	15.29	15.87	4
E1	.540	–	15.72	–	
e	.215 BSC		5.46 BSC		
øk	.010		2.54		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
N	3		7.62 BSC		
øP	.140	.144	3.56	3.66	
øP1	–	.275	–	6.98	
Q	.209	.224	5.31	5.69	
R	.178	.216	4.52	5.49	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

IGBTs, CoPACK

1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

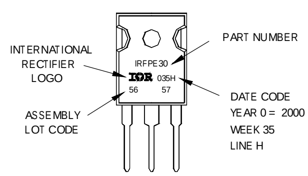
DIODES

1.– ANODE/OPEN
2.– CATHODE
3.– ANODE

TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2000
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position indicates "Lead-Free"



Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting $T_J = 25°C$, L = 15mH $R_G = 25\Omega$, $I_{AS} = 11A$. (See Figure 12)

③ $I_{SD} \leq 11A$, $di/dt \leq 126A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150°C$

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

Data and specifications subject to change without notice.

International
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