DESCRIPTION

The PT2482 is a brushed-DC motor driver for printers, home appliances, industrial equipment, and other small machines. Dual pin logic inputs controls the H-bridge driver output current flows to maniple the motor rotation in forward or reverse direction. With sufficient heat dissipation PCB area or add-on heatsinking, the peak output current may up to 3.6 Amps.

The PT2482 has built-in PWM current regulation circuits; it's a very useful function to limiting average current draws from power supply during motor rotates starts up and stalled. The PWM current regulation level is determinates by an external resistor connects on ISEN pin. And FALTN pin can be uses as fault indication for microcontroller during output is over current (OCP), thermal shutdown (TSD) or VM under voltage lockout (UVLO) is active.

The PT2482 is protected from many fault conditions, including under voltage (UVLO), over current protection (OCP) and over temperature shut down (TSD). The drive will disable the H-bridge output during fault condition is met, and device will automatically recovery when fault phenomena is removed.

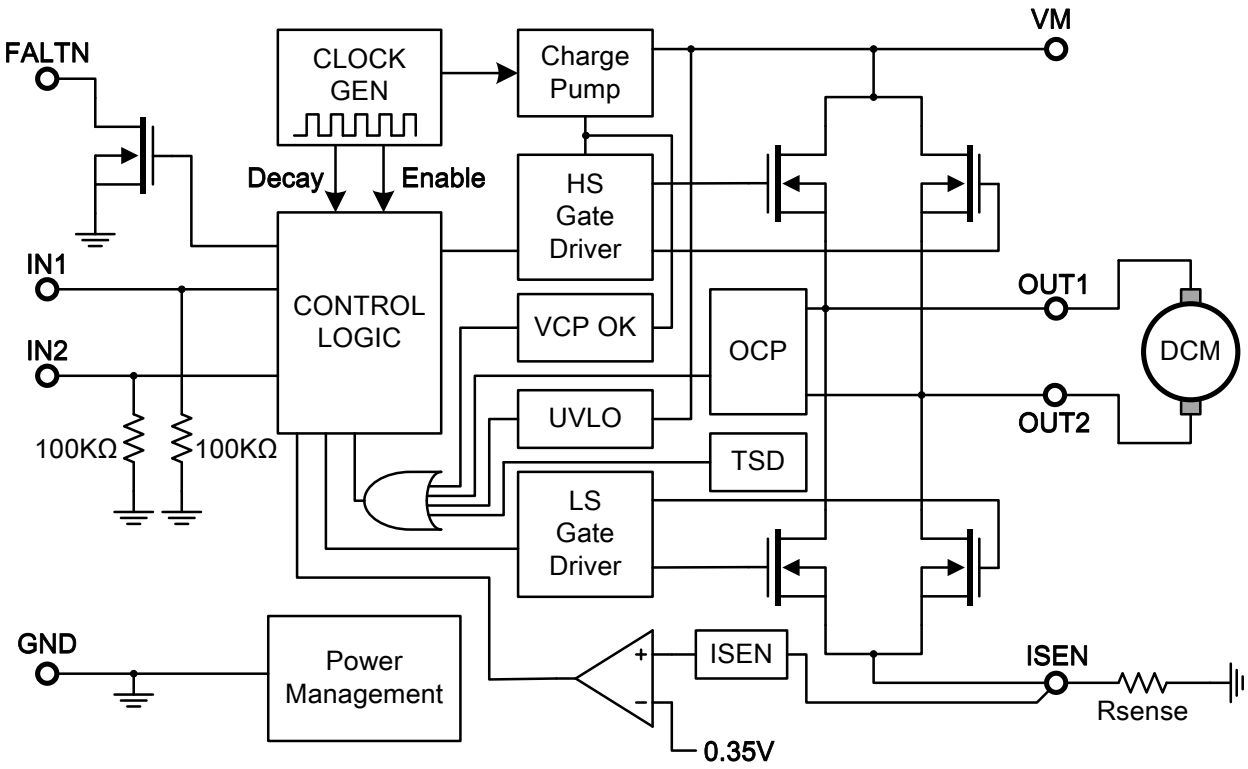
FEATURES

- H-Bridge Motor Driver for:
  – Single brushed DC Motor,
  – Single Winding of a Bipolar Stepping Motor
  – Solenoid High Side Driver
- Wide Operating Voltage : 6.5V to 45V
- Low Switches $R_{DS(on)}$ (HS+LS) : 500mΩ(typ)
- Peak Current Output : 3.6 Amps
- H-bridge Control Interface
- PWM Current Regulation
- Low-Power Sleep Mode
- Fault Indication Output
- Small Package and Footprint
  – 8-Pin HSOP With Thermal PAD
- **Protection Features**
  – VM Under voltage Lockout (UVLO)
  – Over Current Protection (OCP)
  – Over Thermal Shutdown (TSD)
  – Automatic Fault Recovery

APPLICATIONS

- Printers
- Home Appliances
- Industrial Equipment

BLOCK DIAGRAM



APPLICATION CIRCUIT

Drives brushed DC motor with PWM current regulation function.

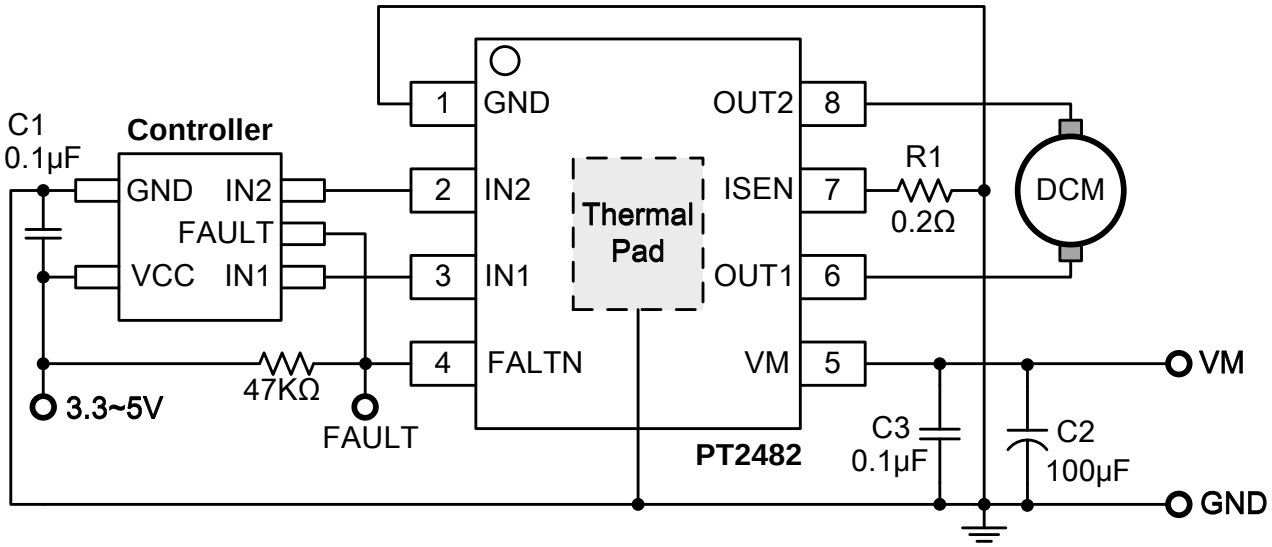


Figure 1. Typical Application Circuit

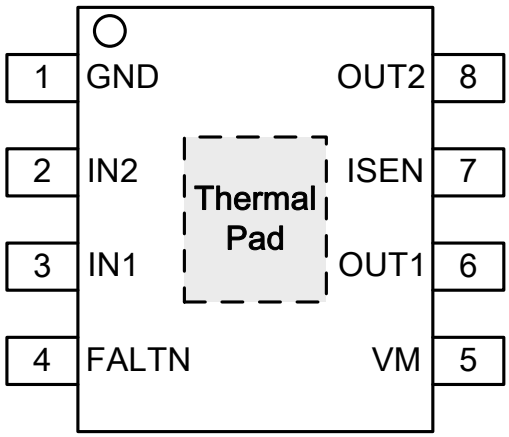
note(1) : The recommended value of R1 is from 0.1Ω to 0.5Ω, power dissipation from 0.5 to 1W.
note(2) : Connects ISEN pin to power ground directly if PWM current regulation function is not necessary.
note(3) : FAULT pin should be connects a pull up resistor to the VCC of microcontroller.

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT2482-HS	8 Pins, HSOP	PT2482-HS

PIN CONFIGURATION

Top View



PIN DESCRIPTION

Pin Name	Type	Description	Pin No.
GND	POWER	Ground for internal circuits, connects to power ground.	1
IN2	I	Control logic input 2, with 100KΩ internal pulldown.	2
IN1	I	Control logic input 1, with 100KΩ internal pulldown.	3
FALTN	O	Fault indication output.	4
VM	POWER	Main power supply input for the IC.	5
OUT1	O	H-bridge output 1.	6
ISEN	O	H-bridge low side MOSFETs ground current path, refer to the application circuit for the recommends of sense resistor connection.	7
OUT2	O	H-bridge output 2.	8
THERMAL PAD	-	Thermal pad; must be soldered to the PCB ground plane. For improves thermal dissipation, a broad, multiple layer ground planes with multiple via connection is recommended.	-

FUNCTION DESCRIPTION

H-BRIDGE OUTPUT CONFIGURATION

The motor winding current direction is determinate by H-bridge output configuration, and it is maniples by control logic interface. Please refer to Table 1 for corresponds between input and output.

IN1	IN2	OUT1	OUT2	DESCRIPTION
0	0	HiZ	HiZ	Coast mode. The H-bridge is disabled and whole chip entering sleep mode after Tslp time (~1mS).
0	1	L	H	Reverse mode (Output current from OUT2 to OUT1)
1	0	H	L	Forward mode (Output current from OUT1 to OUT2)
1	1	L	L	Brake mode; motor winding current flowing in between both low side MOSFETs.(slow decay)

Table 1. H-Bridge Output Operation

SLEEP MODE

If both control logic input pin sets to low state(or float connection) from forward/reverse mode, the H-bride will disabled immediately, after a short delay time (Tslp, approximately 1mS) the internal circuit also disabled and whole chip will entering sleep mode, the current consumption will drops to Islp level and outputs remains in HiZ.

The internal circuit needs an enable time (Tena, approximately 50μS) to wakes up the H-bridge from sleep mode or UVLO released. During sleep mode actives, whatever the IN1 or IN2 pin are pull-high for at least 5μS, the chip will quit from sleep mode and H-bridge will operates after Tena time.

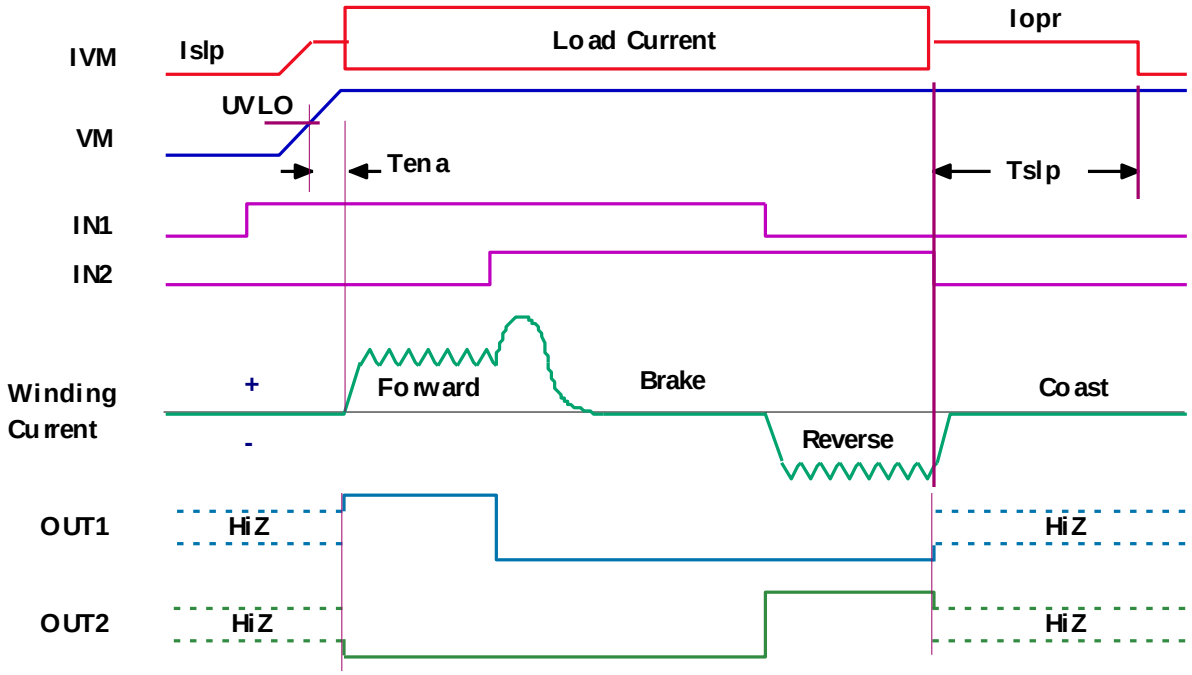


Figure 1. H-Bridge Output Mode and Control Logic Timing

PWM CURRENT REGULATION

The output current of H-bridge is based on the reference input, VREF, and the resistance of current sensing resistor placed on the ISEN pin, the current setting according to Equation 1:

$$I_{TRIP}\ (A) = \frac{V_{TRIP}\ (V)}{R_{ISEN}\ (\Omega)} = \frac{0.35\ (V)}{R_{ISEN}\ (\Omega)} \quad \text{(Eq.1)}$$

For example, if R_{ISEN} = 0.2Ω, the internal reference V_{TRIP} = 0.35V fixed, the PWM current regulation mechanism will limits motor winding or inductor current not exceeds 1.75 Amps no matter how much load is applied. When I_{TRIP} is reached, the H-bridge enforces the inductor current into slow decay path by enabling both low-side FETs, and it does this for a fixed off time, T_{OFF} (typically 25 μs).

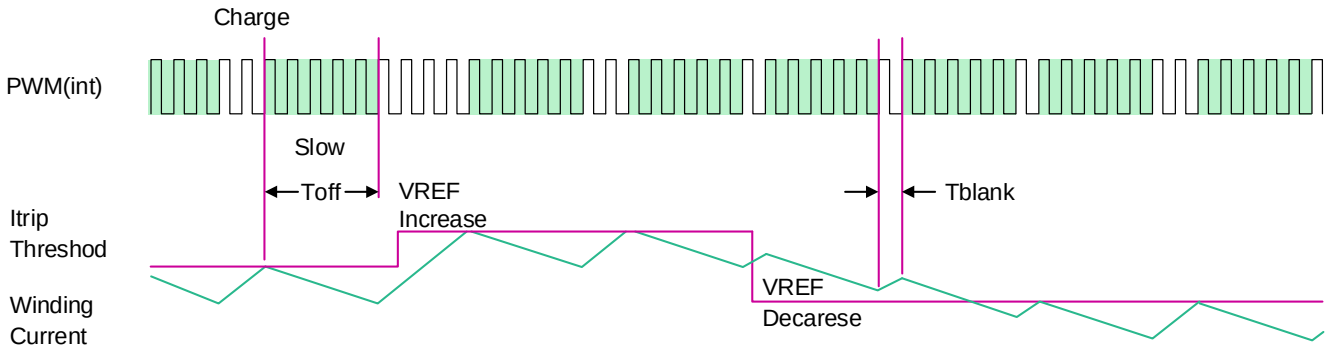


Figure 2. PWM Current Regulation Operation Period and Timing

After T_{off} time passes, the H-bridge output is re-enabled according to the logic states of two inputs, IN1 and IN2, and motor winding current is charging until reaching another I_{TRIP} event, this charge time is heavily depends on the VM voltage, the back-EMF of the motor, and the inductance of the motor.

BLANKING TIME

During PWM current regulation is works, each time the H-bridge enabled, the load current level can be picked-up from the internal ISEN block, the signal will delivers to comparator after a fixed delay time (T_{blank}) to avoid noises or current spike causes fault-triggered. The blanking time is fixed at 2.8μS and it also sets a minimum duty cycle of PWM in charge period.

DEAD TIME

When an output level changes from high to low, or vice versa, a dead time will automatically insert to prevent output MOSFETs shoot-through. In the dead time (T_{dt}) period, both outputs are keeps in HiZ states. If winding or inductor current is still flows during dead time inserted, the rest of current will be reset to zero through the parasitic body diode of output MOSFETs, and the voltage presents on output pin during dead time is depends on demagnetized current flow. If the current is leaving the output pin, the current will flows through the low side body diode and output potential drops below ground; if the current is entering the output pin, the current will flows through the high side body diode and output potential will exceeds the VM voltage.

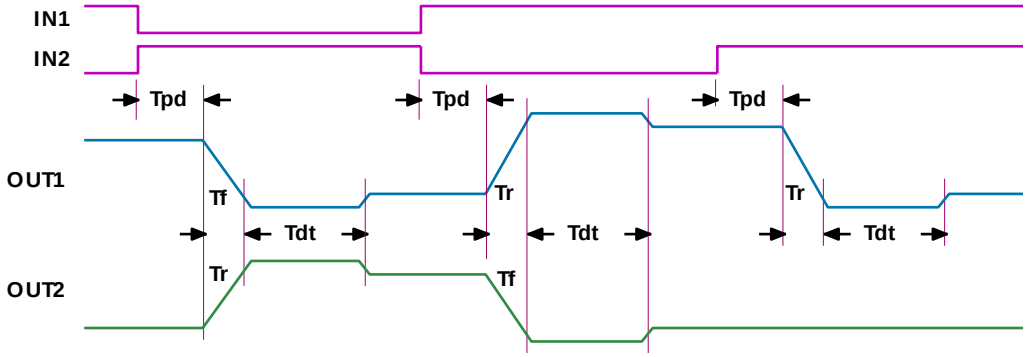


Figure 3. I/O Propagation Delay Time

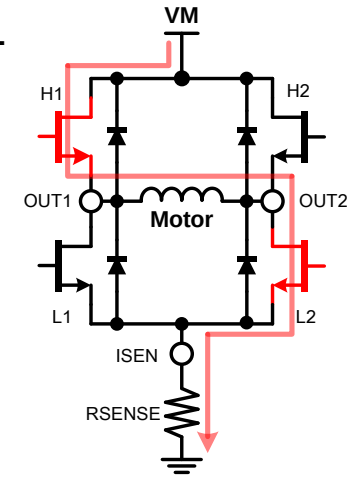
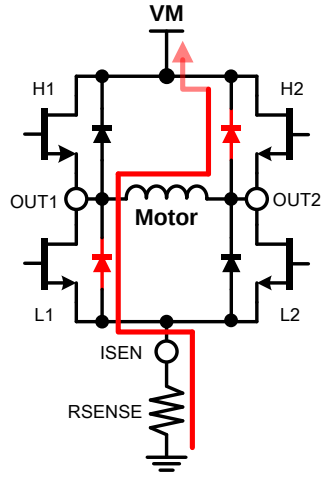
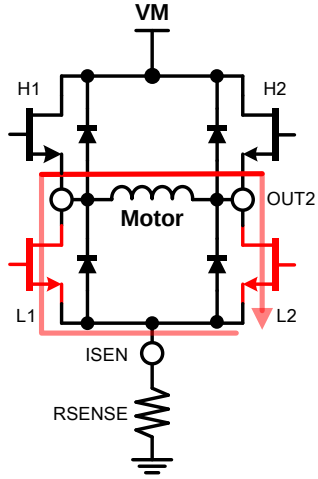
1	2	3
		
Charge	**Dead Time**	**Brake(Slow Decay)**
Turn on H1 and L2, the winding current through the H-bridge from VM to GND. When comparator threshold, is reached, the charge mode will be goes to next step.	All of MOSFETs disabled, the reset of inductor current will passes through the body diode and decays to zero.	Turn on L1 and L2 both, the circulate winding current is flows through the low side MOSFETs loop.(Brake)

Figure 4. H-Bridge Current Paths

PROTECTION CIRCUITS

The PT2482 have fully protection function to against miss-operation events.

OVER CURRENT PROTECTION (OCP)

Over current detection circuit will monitor the output current of H-bridge driver and it is irrelevant to PWM current regulation mechanism. If any output pin connected to VM, GND or both outputs be short circuit together, during the inrush current exceeds protection threshold (I_{OCP}) and be detected by OCP circuit, the output switches of the H-bridge will be disabled after the OCP deglitch time (T_{OCP}). The chip will remain disabled and wait for a rest time (T_{RTY}), after T_{RTY} time elapses the chip will enable again.

In brake mode, both low side MOSFETs are enabled and inductor/winding current is flows inside the loop, in actually it is similar to short circuit condition, therefore the SCP detection will temporary disabled in this mode.

THERMAL SHUTDOWN (TSD)

If the chip junction temperature exceeds 175℃, the H-bridge output will be turn off, until the chip temperature is cooling down to below hysteresis window, H-bridge output will be enabled again.

UNDERVOLTAGE LOCKOUT (UVLO)

In Any time the VM pin voltage drops below the under voltage lockout threshold voltage, all circuitry in the chip will be disabled and internal logic will be reset. Operation will resume when VM rises above the UVLO threshold.

FAULT INDICATION (FALTN)

Whatever which condition is happens, the OCP, TSD or UVLO, the open-drain FALTN pin will pull-down immediately and remains until fault condition no longer exist. It can be connected to microcontroller as motor driver error reporting with a pull-up resistor connects to the VCC supply of microcontroller.

POWER SUPPLY CAPACITOR RECOMMENDATIONS

Consider a real world application scenario; the motor driver is designed to drives high inductance load such like motor winding or solenoid coil. If a H-bridge turns-off all of outputs during inductor current still flowing, because the inductor current would not be reset immediately, the rest of free-wheel current would re-directs and passing through the body diode of the output FET and runs into VM supply and final decay to zero after de-magnetization time. This reverse current depends on load inductance, inductor current and re-generates current from the motor due to inertia of rotor.

In another case, the parasitic reactance (inductance + resistance) of power wire between the power supply and motor driver board with parasitic capacitance of PCB consists a LC resonates tank, during power supply sourcing current to the motor driver board, the VM voltage may drops quickly and parasitic LC will be trigged and shows oscillation spike if the local bypass capacitor is not sufficient.

To prevent unstable bounce or spike appears on VM bus, a high capacitance bounce absorber capacitor (>100μF) should be placed on VM bus line, it could absorb re-generates free-wheels current during DC motor brake and stabilize VM voltage during high forward/reverse motor current sources. A small MLCC 0.1μF bypass capacitor should be placed near the motor driver IC power pin, to reduce the spike causes by power line LC resonates.

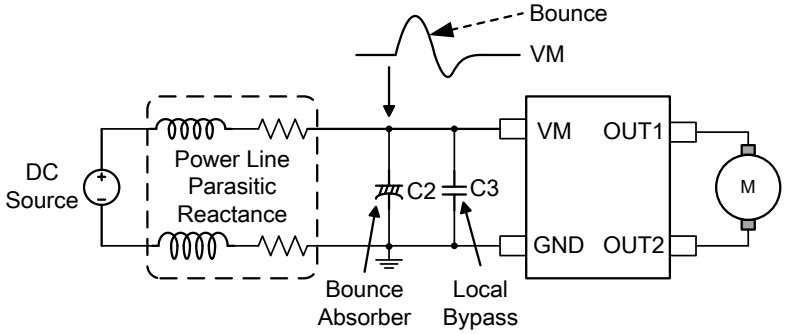
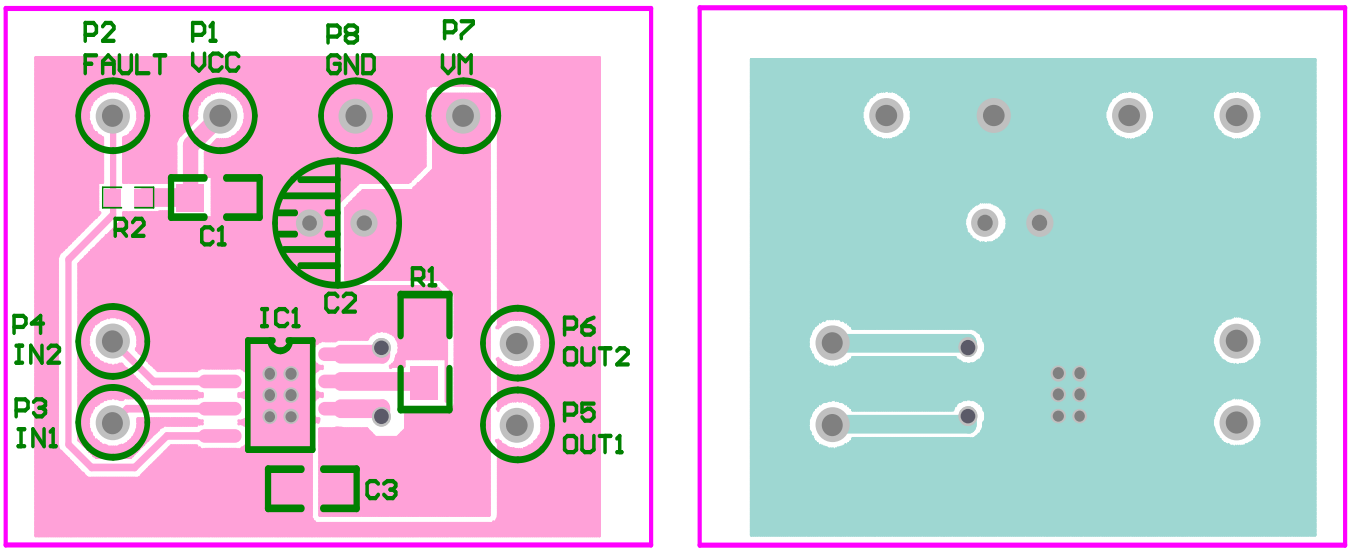


Figure 5. Motor Driver System with External Power Supply

PCB LAYOUT RECOMMENATION

The local bypass capacitor C3 should be placed near the IC power pins, and bounce absorber capacitor C2 should be placed on VM bus line. The GND plane should be placed on the component side under the chip as a low impedance power trace, and larger area of GND plane and wider cooper trace reduce the thermal resistance (θ_{JA}). The thermal pad under HSOP package should be soldered to the PCB component side and connects to the bottom side through via holes, this arrangement can further enhance the heat dissipation.

The power rating of the current sense resistor R1 is determinates by the IR drops, consider a worse case, the maximum output current is continue conducts, for example, the average output current is 2 Amps, and current sense resistance is 0.2Ω, the power dissipation of resistor is (2^2X0.2) = 0.8W, therefore a 1watt resistor is a better choice, and sense resistor should be connected to ground plane to enhance heat dissipation.



Top Side

Bottom Side

Figure 6. Simplified Layout Example

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted) (1)

Parameter	MIN	MAX	UNIT
Power supply voltage (VM)	-0.3	45	V
Logic input voltage (IN1, IN2)	-0.3	5.5	V
Logic output voltage (FALTN)	-0.3	5.5	V
Continuous phase node pin voltage (OUT1, OUT2)	-0.7	VM+0.7	V
Output current (100% duty cycle)	0	3.6	A
Operating junction temperature, Tj	-40	150	°C
Storage temperature, Tstg	-40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

Parameter	Symbol	MIN	MAX	UNIT
Power supply voltage	VM	6.5	45	V
Logic input voltage (IN1, IN2)	V_I	0	5.5	V
Logic input PWM frequency (IN1, IN2)	f_{PWM}	0	200(1)	KHz
Peak output current(2)	I_{peak}	0	3.6	A
Operating ambient temperature(2)	T_A	-40	125	°C

(1) The voltages applied to the inputs should have at least 800 ns of pulse width to ensure detection. Typical devices require at least 400ns. If the PWM frequency is 200 kHz, the usable duty cycle range is 16% to 84%.

(2) Power dissipation and thermal limits must be observed.

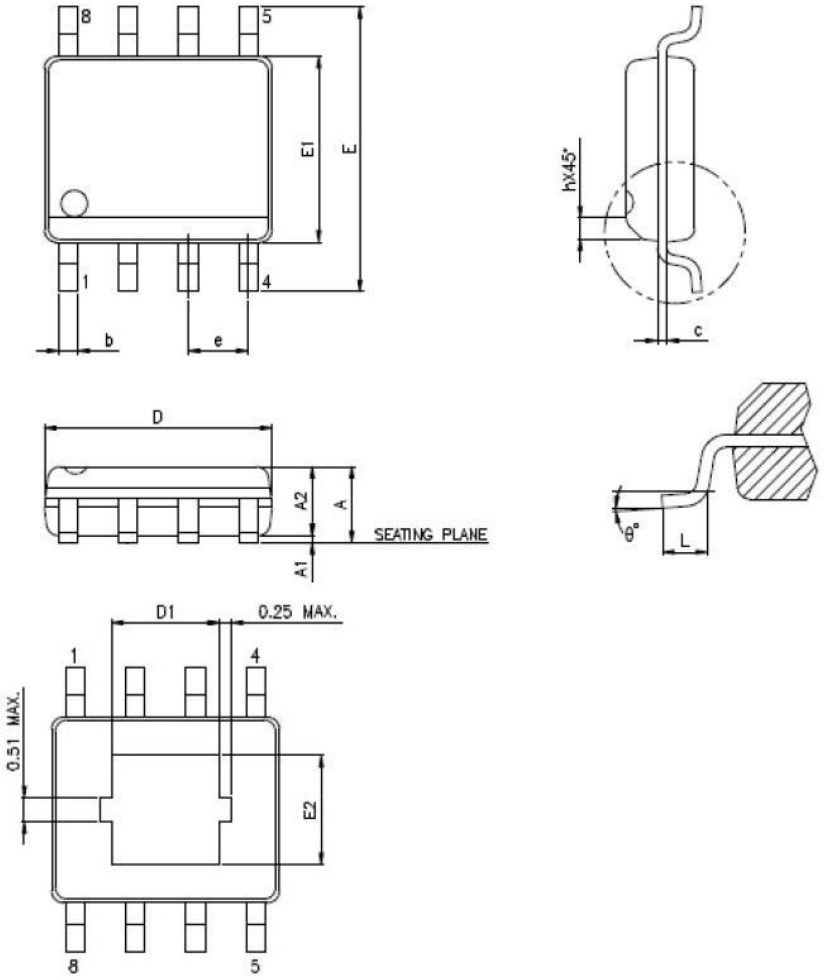
ELECTRICAL CHARACTERISTICS

TA = 25°C, VM=24V, over recommended operating conditions (unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
POWER SUPPLY (VM)						
VM operating voltage	VM		6.5		45	V
VM operating supply current	Iopr	VM = 12 V		4	10	mA
VM sleep current	Islp	VM = 12 V			8	μA
Turn-on time	Tena	VM > VUVLO with IN1 or IN2 high		50	100	μS
CONTROL LOGIC INPUTS (IN1, IN2)						
Input logic low voltage	V_{IL}				0.5	V
Input logic high voltage	V_{IH}		2			V
Input logic hysteresis	V_{HYS}			0.8		V
Input logic low current	I_{IL}	V_{IN} = 0 V	-1		1	μA
Input logic high current	I_{IH}	V_{IN} = 3.3 V		33	100	μA
Pulldown resistance	R_{PD}	to GND		100		kΩ
Propagation delay	T_{PD}	INx to OUTx change		0.6	1	μS
Time to sleep	Tslp	Inputs low to sleep		1	1.5	mS
MOTOR DRIVER OUTPUTS (OUT1, OUT2)						
High-side FET on resistance	$R_{DS(ON)}$	VM = 24 V, I = 1 A, f_{PWM} = 25 kHz		250	300	mΩ
Low-side FET on resistance	$R_{DS(ON)}$	VM = 24 V, I = 1 A, f_{PWM} = 25 kHz		250	300	mΩ
Output dead time	T_{DEAD}			200		nS
Body diode forward voltage	V_d	IOUT = 1 A		0.8	1	V
CURRENT REGULATION						
ISEN voltage for PWM current regulation	V_{TRIP}		0.32	0.35	0.38	V/V
PWM off-time	T_{OFF}			25		μS
PWM blanking time	T_{BLANK}			2.8		μS
PROTECTION CIRCUITS						
VM under voltage lockout	V_{UVLO}	VM falls until UVLO triggers		6	6.2	V
		VM rises until operation recovers		6.2	6.4	V
VM under voltage hysteresis	$V_{UV,HYS}$	Rising to falling threshold	100	180		mV
Overcurrent protection trip level	I_{SCP}	Across the Load	3.7	4.5	6.4	A
Overcurrent deglitch time	Ts_{CP}			1.5		μS
Overcurrent retry time	T_{RTY}			6		mS
Thermal shutdown temperature	T_{SD}		150	175		°C
Thermal shutdown hysteresis	T_{HYS}			40		°C
FALTN OPEN DRAIN OUTPUT						
Output low voltage	V_{OL}	I_O = 5 mA			0.5	V
Output high leakage current	I_{OH}	V_O = 3.3V			1	μA

PACKAGE INFORMATION

8 PINS, HSOP



Symbol	Dimensions(mm)		
	Min.	Nom.	Max.
A	-	-	1.70
A1	0.00	-	0.15
A2	1.25	-	-
b	0.31	-	0.51
c	0.10	-	0.25
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
D1	2.81	-	3.45
E2	2.05	-	2.56
L	0.40	0.60	1.27
θ	0°	-	8°

Notes: Refer to JEDEC MS-012 BA

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