13.56 MHz 64 Data bit Read Only Contactless Identification Device

Features

- Operating frequency range 10 MHz to 15 MHz
- RF interface optimized for 13.56 MHz operation
- Laser programmed memory array (64 data bit + 16 CRC bit)
- Modulator switch designed to preserve supply voltage
- Miller coding
- Default data rate is 26484 Baud
- Other data rates possible (mask programmable)
- On chip rectifier
- On chip resonant capacitor
- On chip supply buffer capacitor

Typical Operating Configuration

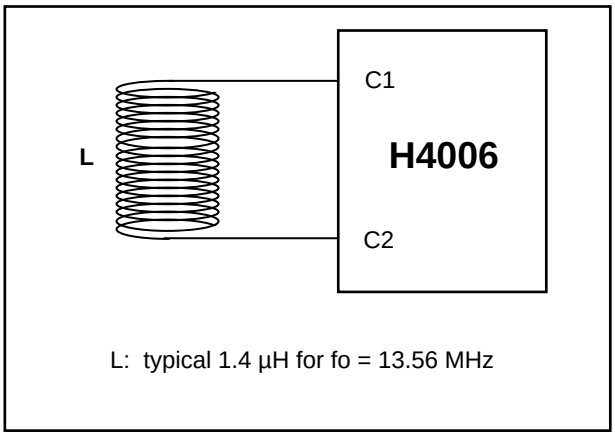


Figure 1

Description

The H4006 is a CMOS integrated circuit intended for use in electronic Read Only transponders.
The exited coil connected to the device generates the power supply via a Graetz bridge and an integrated decoupling capacitor. The clock used for the logic is also extracted from the coil. The logic is mainly composed by a miller code generator and the LROM control. The memory is factory programmed so that each IC is unique.

Pad Assignment

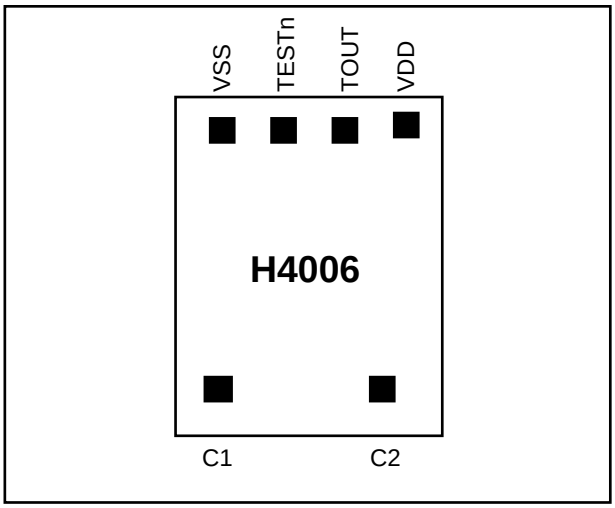


Figure 2

Applications

- Logistics automation
- Anticounterfeiting
- Access control
- Industrial transponder

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Maximum DC Current forced on COIL1 and COIL2	I_{CMAX}	±30mA
Power Supply	V_{DD}	-0.3V to 7.5V
Storage Temperature	T_{st}	-55 to +200°C
Electrostatic discharge maximum to MIL-STD-883C method 3015	VESD	2000V

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Temp.	Top	-40		+85	°C
Maximum Coil Current	Icoil	-10		10	mA
AC Voltage on Coil	Vcoil	3	14*		Vpp
Supply Frequency	fcoil	10	13.56	15	MHz

Table 2

*) The AC Voltage on Coil is limited by the on chip voltage limitation circuitry. This is according to the parameter Icoil.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however due to the unique properties of this device, anti-static precautions should be taken as for any other CMOS component.

System Principle

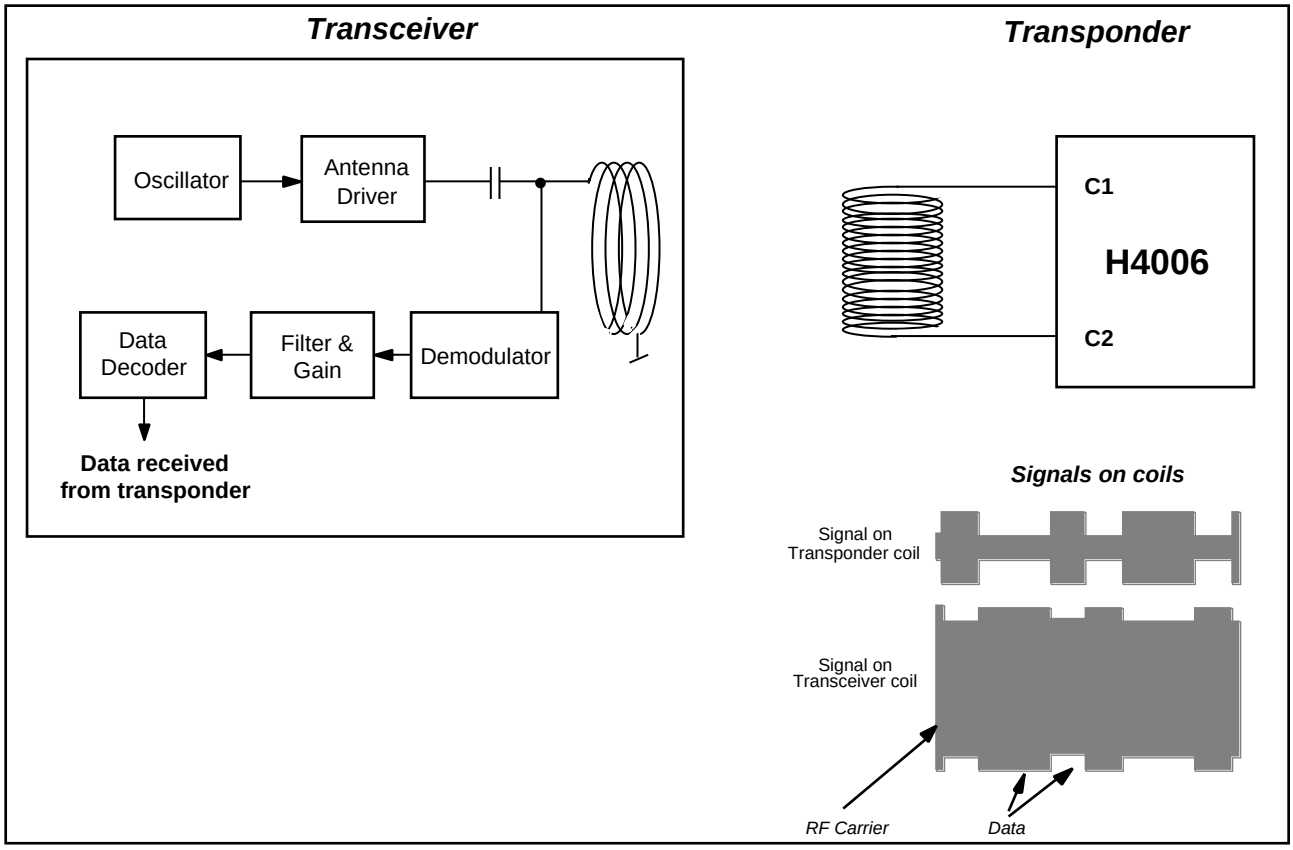


Figure 3

Electrical Characteristics

V_{DD} = 2V, V_{SS} = 0V, f_{C1} = 13.56MHz sine wave, V_{C1} = 1.0Vpp centered at (V_{DD} - V_{SS})/2, T_a = 25°C unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{DD}		1.9		[1]	V
Supply current	I_{DD}			60	150	µA
Rectifier Voltage Drop	V_{REC}	I_{C1C2} = 1mA, modulator switch on V_{REC} = (V_{C1}-V_{C2}) - (V_{DD} - V_{SS})			1.8	V
Modulator ON DC voltage drop [2]	V_{ON1} V_{ON2}	$I_{VDD\ VSS}$ = 1mA $I_{VDD\ VSS}$ = 10mA	1.9 2.4	2.3 2.8	2.8 3.3	V V
Power on reset [3]	V_R V_R - V_{MIN}		1.2 0.1	1.4 0.25	1.7 0.5	V V
Coil1 - Coil2 Capacitance	C_{RES}	V_{coil}=100mVRMS f=10kHz	92.6	94.5	96.4	pF
Series resistance of C_{RES}	R_S			3		Ω
Power Supply Capacitor	C_{sup}			140		pF

[1] Maximum voltage is defined by forcing 10 mA on C1 - C2 Table 3
[2] Measured between VDD and VSS
[3] According to Figure 7

Block Diagram

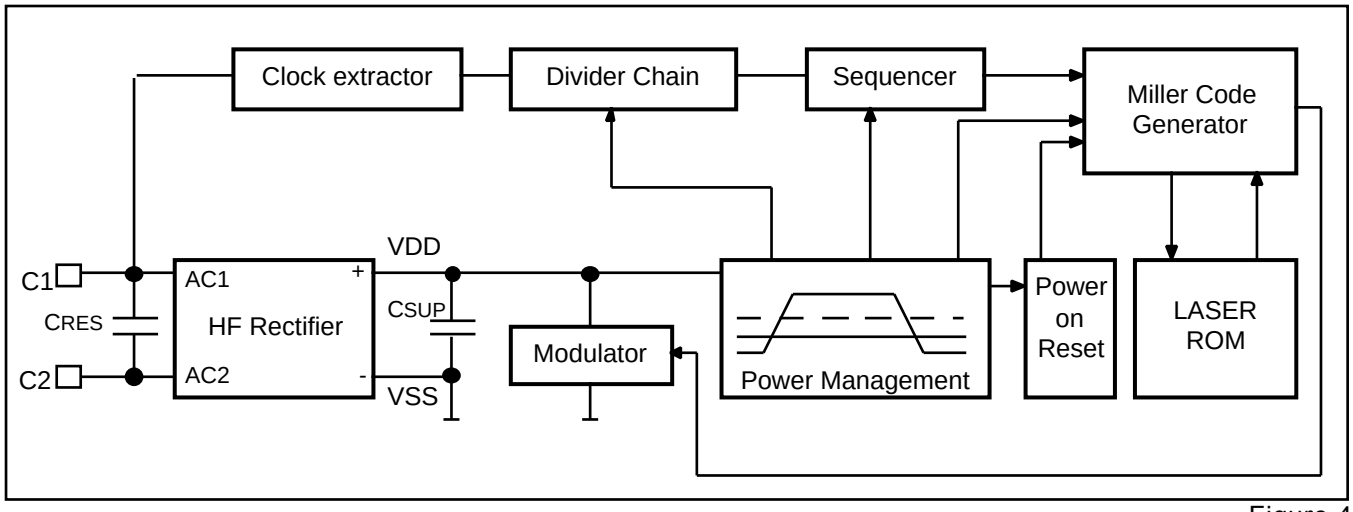


Figure 4

General description

The transponder will be activated when illuminated by a RF field of sufficient power and at any frequency that is compatible with its associated antenna and its internal power supply circuit input characteristics. The chip will Power-on-Reset itself when powered by this incoming energy that exceeds its reset threshold. After resetting itself the chip will start to transmit its memory contents as a stream of Miller code. The memory contents is transmitted by modifying the antenna matching impedance at its internal clock rate, thereby causing varying amounts of RF energy to be reflected from the antenna. This impedance variation will be achieved by connecting a modulating device across the antenna terminals. When switched on the modulating device will present a low impedance to the antenna. This will cause a change in the matching of the antenna and therefore in the amount of RF energy reflected by the transponder to the reader. This reflected signal combines with the transmitted signal in the receiver to yield an amplitude modulated signal representative of the IC memory contents. The “ON” impedance of the modulating device needs to be comparable to about 100 Ohms to affect the matching of the antenna and therefore its reflectivity.
The RF signal received from the transponder antenna will serve several purposes :

- power the chip
- provide a global reset to the chip through its POR (Power-On-Reset) function
- provide a carrier for the data transmission
- provide the input of the internal clock generation circuit (frequency division)

Functional description

Output Sequence

Transmission from the transponder will be accomplished through variation of the antenna load impedance by switching the modulating device ON and OFF.
Output sequence is composed of cycles which are repeated. Each cycle is composed of 82 bits Standard Message Structure (STDMS) which is Miller coded and a pause (LW) during which the modulating device is OFF (see figure 6 for details of Miller code).
The pause (LW) is 9bits length.
The 82 bit STDMS consists of 1 start bit, 64 data bits, 16 CRC bits and 1 stop bit.

Start bit (1)	Data(64)	CRC (16)	Stop bit (1)	LW(9)

Table 4

Memory organisation

As already mentioned above the 82 bits are stored in laser programmed ROM (LROM). The 82 bits of this LROM is partioned as followed (see table 5):

Wafer Number	5 bits
Factory reserved	4 bits
IC name	10 bits
Customer ID	13 bits
Extended lot number	18 bits
IC position	14 bits
Cyclic redundancy check	16 bits
Start and stop bits	2 bits

First bit sent is bit 0.

Memory Map

0	1	2	3	4	5
start	Wafer Number				

6	7	8	9
Factory Reserved			

10	11	12	13	14	15	16	17	18	19
IC Name									

20	21	22	23	24	25	26	27	28	29	30	31	32
Customer ID												

33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50
Extended lot number																	

51	52	53	54	55	56	57	58	59	60	61	62	63	64
IC position													

65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81
Cyclic redundancy check																stop

Table 5

Wafer number
Each wafer has a number between 1 and 25. This 5 bit wafer number contains the wafer number where the IC was.

Factory reserved bits
These 4 bits are reserved. Default value is 0hex.

IC name bits
They contains the 3 first characters device name. For this device, the value is 006hex.

Customer ID bits
This field contains a code which is defined by EM Microelectronic-Marin S.A. For standard version, the code is 0001hex.

Extended lot number
The code on the chips is unique and reflects the production lot number system of EM Microelectronic. This numbering allows full traceability of each chip.

IC position
These 14 bits give the precise position on the processed wafer.

Cyclic redundancy check
The shift register is reset to all zero with each Stop Bit.
CRC code is calculated on 64 data bits. The CRC code is calculated according to CCITT / ISO 3309 - 1984 standarts. See figure 5 for principle block schematic and generating polynomial of the CRC code.

Start and stop bits
Start bit is set to logic 1 and stop bit is set to logic 0.

CRC Block Diagram

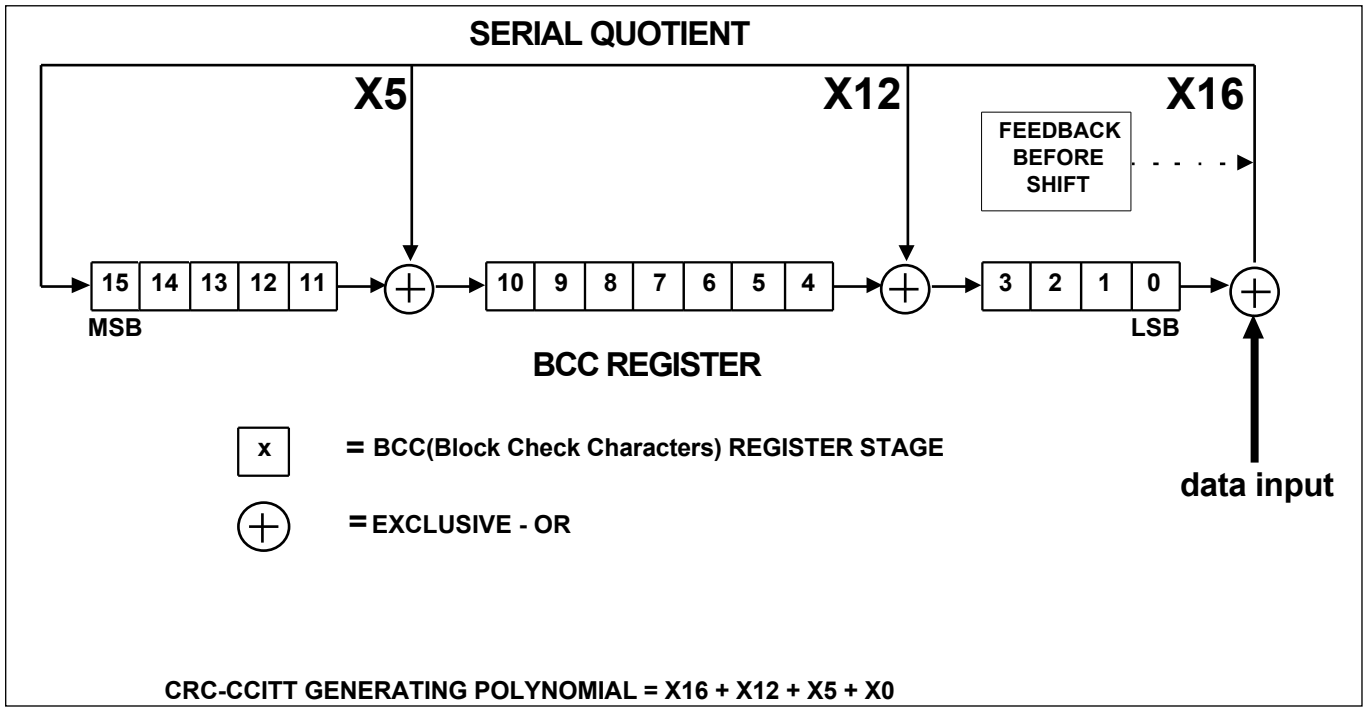


Figure 5

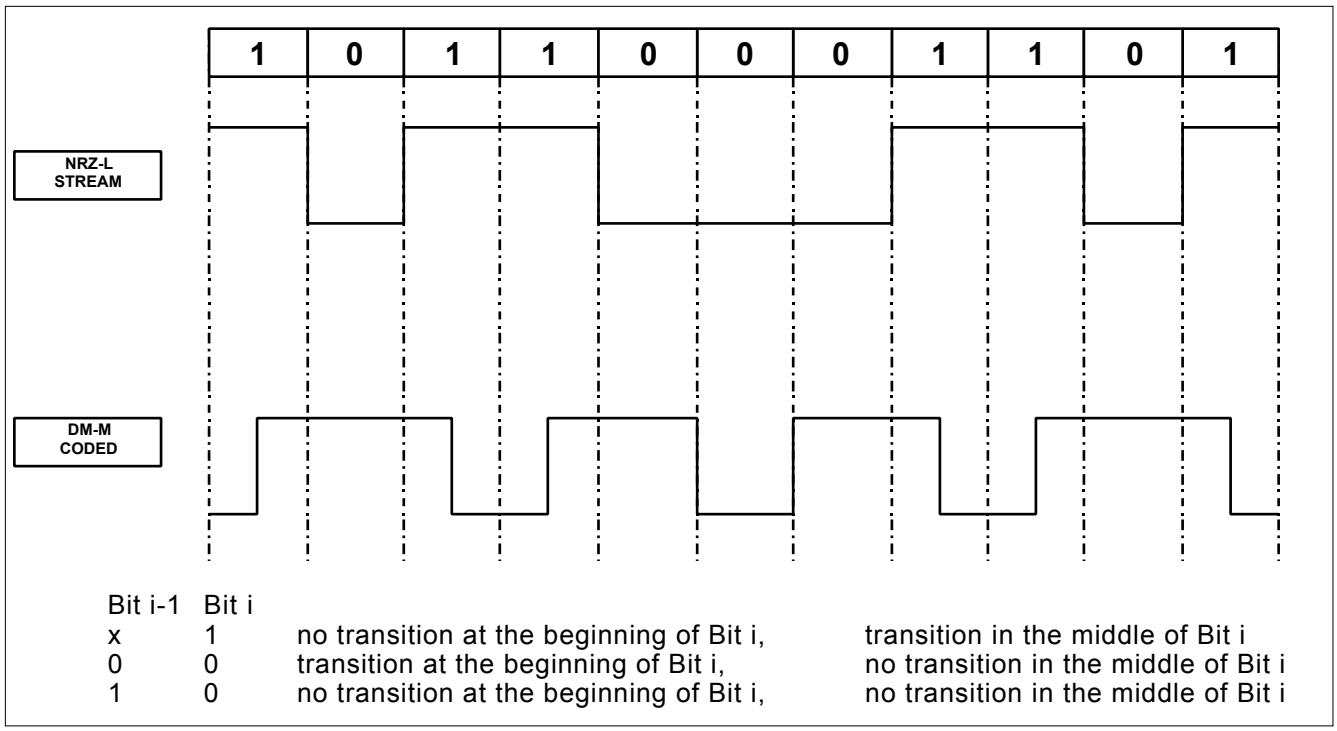
RF Interface
Resonant capacitor, Rectifier, Limiter and Modulator Switch form the unit which is interfacing to the incoming RF signal. These blocks are interdependent so they are developed as unit. They interface to the antenna which typical characteristics are:

Ls ≈ 1400 nH
Rs ≈ 3 Ohms
30 < Q < 40 at 13.56 MHz.

Resonant Capacitor
The capacitor value is adjusted by laser fusing. It can be trimmed in factory by 1pF steps to achieve the absolute value of 94.5pF typically. This option, which is available on request, allows a smaller capacitor tolerance over the whole production.

Rectifier and Limiter
A full wave rectifier (Graetz Bridge) is used to provide supply voltage to the IC. The reverse breakdown of the diodes is also used to protect the IC from overvoltages.

Modulator Switch
Due to the low impedance of the antenna and resonant capacitor the Modulator Switch has to present low RF impedance when switched ON (about 100 ohms).
The minimum time period with the Modulator Switch ON is 38 µs. At lower data rates this time is even much longer. The current consumption of divider chain running at 13 MHz is near 60 µA. Putting together this two figures it is clear that it is not possible to supply the IC during the time the Modulator Switch is ON from the integrated Supply Buffer Capacitor which value is approximately 140 pF. The IC has to get power from the RF field also during the time the Modulator Switch is ON.
This problem is solved by putting the Modulator Switch on the output of the Rectifier (between VDD and VSS) and regulating its ON resistance in function of supply voltage. When the supply voltage is high the ON impedance is low. When the supply voltage drops near the region where the operation of the IC at 13.56 MHz is not guaranteed the ON impedance is increased in order to prevent further drop.



Bit i-1	Bit i		
x	1	no transition at the beginning of Bit i,	transition in the middle of Bit i
0	0	transition at the beginning of Bit i,	no transition in the middle of Bit i
1	0	no transition at the beginning of Bit i,	no transition in the middle of Bit i

Figure 6

Power Supply Management

For a correct operation, the device must be initialised. When the transponder is put in the RF field, the supply voltage increases until it achieves Vr limit (see Figure 7). During this time and for an additionnal 64 bit period, the modulator switch is on and the device initialises its internal logic.

At this point, the data transmission starts and runs while the supply voltage is higher than Vmin. If the supply voltage decreases under this limit, the device is again in an initialising state and the modulator is on.

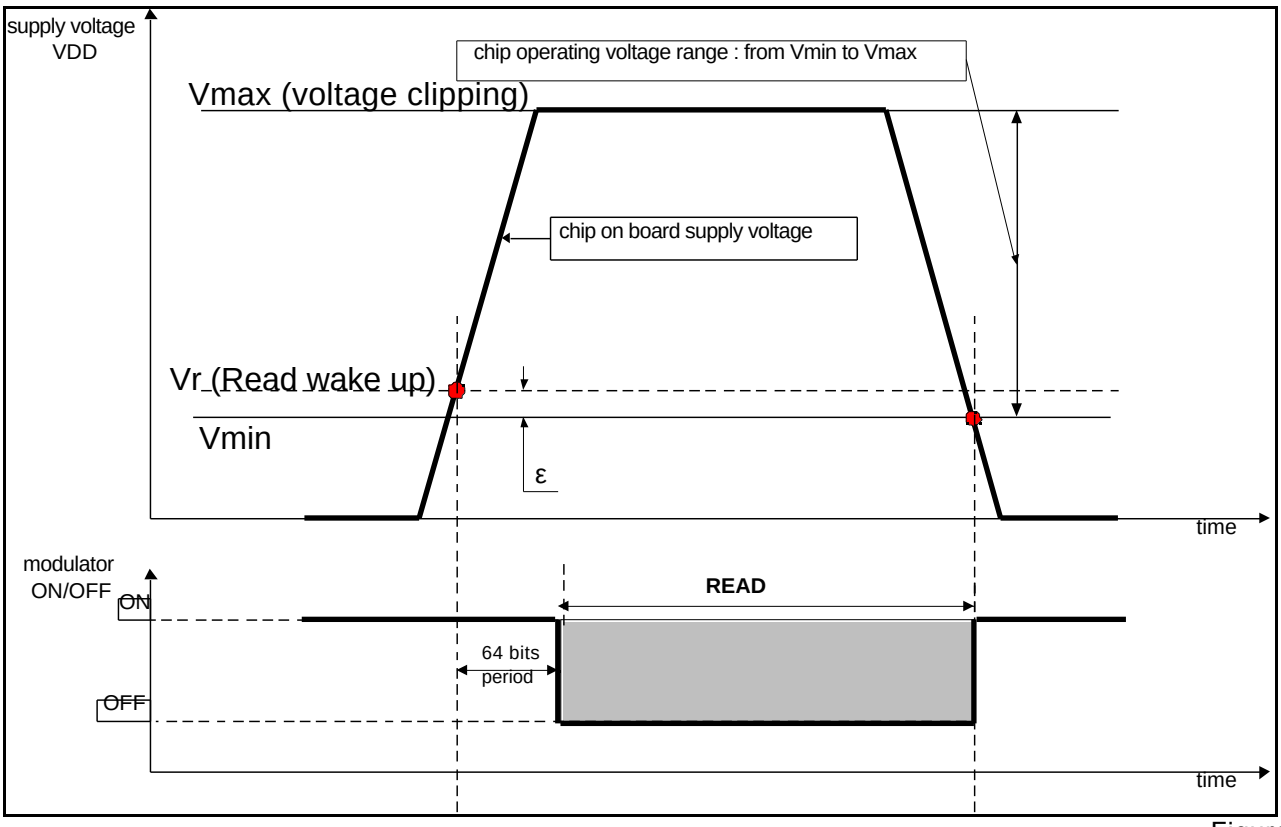


Figure 7

Miller Encoder
The input to Miller encoder is NRZ data coming from LROM. The output is coded according to Miller format and is driving the modulator Switch. See figure 6 for example of Miller code.

Clock Generation
The clock of the logic is extracted from the RF signal. The clock extracted from RF signal is driving the divider chain consisting of toggle flip-flops. The output of this divider chain is data clock with which the data from Laser ROM (LROM) is addressed, encoded and sent to Modulator Switch.
The layout of divider chain is designed in a way that different data rates can be chosen with metal mask (options).
The following division factors are possible on request:
128, 256, 1024, 2048, 4094 and 8192.
The standard is 512.

Others
As mentioned in Output Sequence, during the pause (LW) the Modulator Switch is OFF. When observing the pause duration one has to remember that the time with Modulator Switch OFF effectively observed can vary due to different terminations of STDMS. The stop bit at 0 can be represented either by Modulator Switch ON or OFF depending on the data. The start bit at 1 adds 1/2 of data period OFF (transition in the middle of bit period).
Figure below show the four possible terminations of STDMS and its influence on entire period passed by Modulator Switch OFF. Level LOW represents Modulator Switch OFF. LDB stands for last data bit.

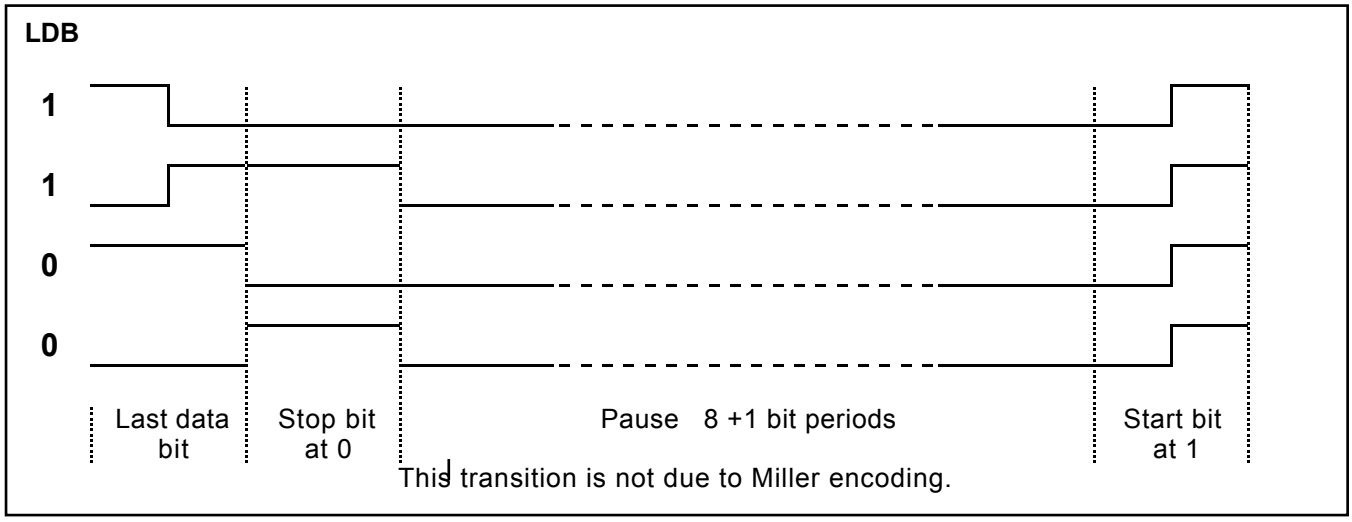


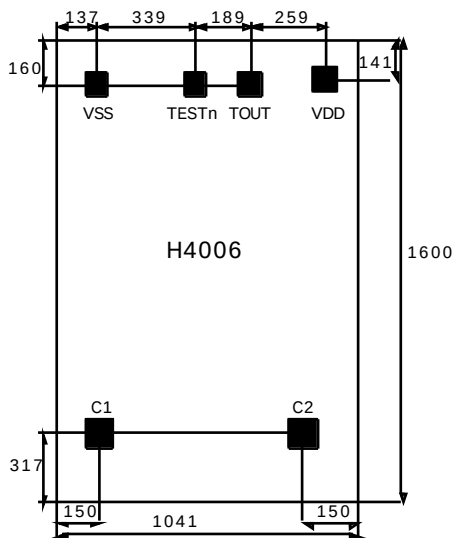
Figure 8

Pad Description

Name	Description
C2	connection to antenna
C1	connection to antenna
VDD	positive supply
Tout	test output
TESTn	test input with pull up
VSS	negative supply

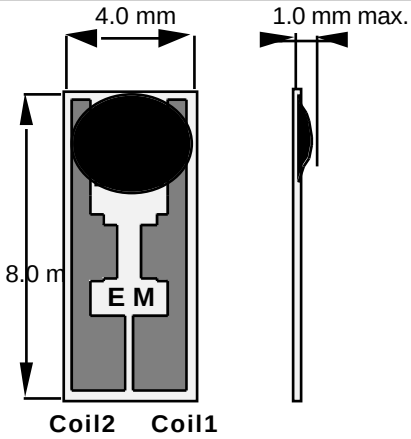
Table 6

Pad position



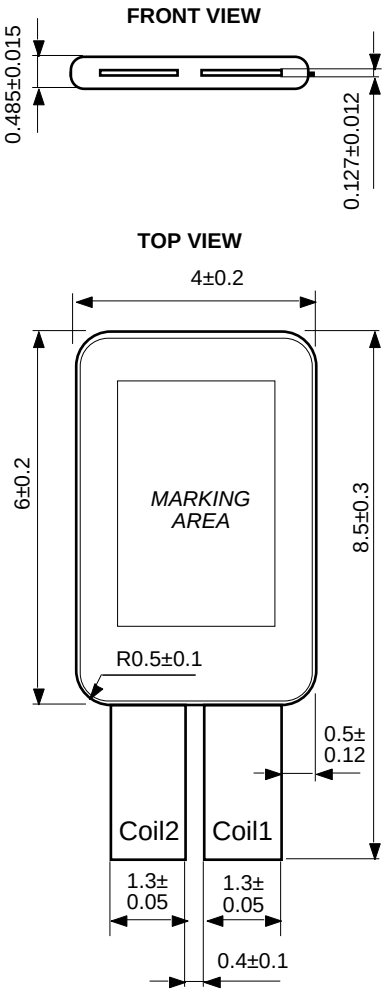
Dimensions in µm

PCB package



Dimensions in mm

CID package



Dimensions in mm

Ordering Information

The H4006 is available in :

- Chip form *	H4006 501 IC
- CIDpack	H4006 501 CID
- PCB package	H4006 501 COB

*Chip will be delivered in wafer form.
Thickness of the wafer: 180 µm ± 20 µm (7 mils)

EM MICROELECTRONIC-MARIN SA CH-2074 Marin, Switzerland Tel. +41 32 755 51 11, Fax. +41 32 755 5403