

# Am25LS2568/Am25LS2569

Four-Bit Up/Down Counters with Three-State Outputs

## DISTINCTIVE CHARACTERISTICS

- 4-bit synchronous counter, synchronously programmable
- Both synchronous and asynchronous clear inputs
- Three-state counter outputs interface directly with bus organized systems
- Internal look-ahead carry logic and two count enable lines for high speed cascaded operation
- Ripple carry output for cascading
- Clock carry output for convenient modulo configuration
- Fully buffered outputs
- Second sourced as the 54LS/74LS568 and LS569
- Advanced Low-Power Schottky technology

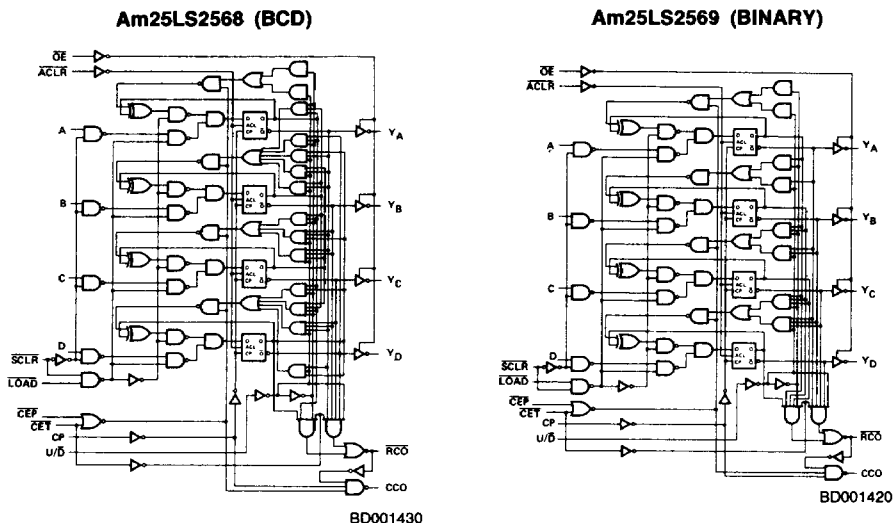
## GENERAL DESCRIPTION

The Am25LS2568 and Am25LS2569 are programmable up/down BCD and Binary counters respectively with three-state outputs for bus organized systems. All functions except output enable (OE) and asynchronous clear (ACLR) occur on the positive edge of the clock input (CP).

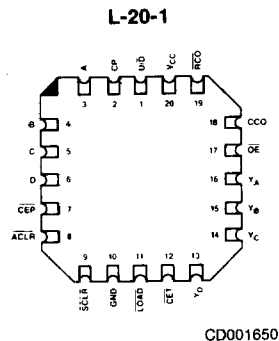
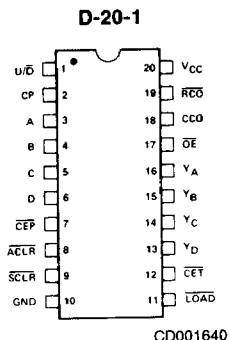
With the  $\overline{\text{LOAD}}$  input LOW, the outputs will be programmed by the parallel data inputs (A, B, C, D) on the next clock edge. Counting is enabled only when  $\overline{\text{CEP}}$  and  $\overline{\text{CET}}$  are LOW and  $\overline{\text{LOAD}}$  is HIGH. The up-down input (U/D) controls the direction of count, HIGH counts up and LOW counts down. Internal look-ahead carry logic and an active LOW ripple carry output ( $\overline{\text{RCO}}$ ) allows for high-speed counting

and cascading. During up-count, the  $\overline{\text{RCO}}$  is LOW at binary 9 for the LS2568 (binary 15 for the LS2569) and upon down-count, it is LOW at binary 0. Normal cascaded operations require only the  $\overline{\text{RCO}}$  to be connected to the succeeding block at  $\overline{\text{CET}}$ . When counting, the clocked carry output (CCO) provides a HIGH-LOW-HIGH pulse for a duration equal to the LOW time of the clock pulse and only when  $\overline{\text{RCO}}$  is LOW. Two active LOW reset lines are available, synchronous clear ( $\overline{\text{SCLR}}$ ) and a master reset asynchronous clear ( $\overline{\text{ACLR}}$ ). The output control (OE) input forces the counter output into the high-impedance state when HIGH and when LOW, the counter outputs are enabled.

## BLOCK DIAGRAM

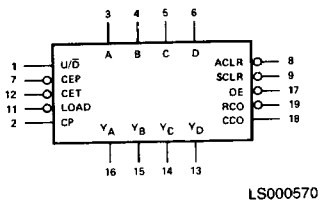


### CONNECTION DIAGRAM Top View

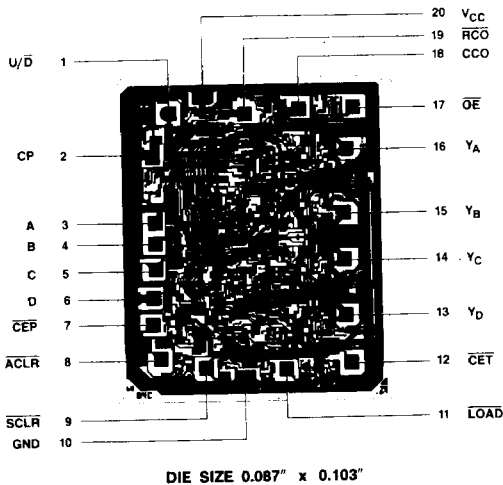


Note: Pin 1 is marked for orientation

### LOGIC SYMBOL



### METALLIZATION AND PAD LAYOUT Am25LS2568



### ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS2568/69

- D** — Package
  - D - 20-pin Cerdip
  - F - 20-pin flatpak
  - L - 20-pin leadless chip carrier
  - P - 20-pin plastic DIP
  - X - Dice
- C** — Temperature (See Operating Range)
  - C - Commercial (0°C to +70°C)
  - M - Military (-55°C to +125°C)
- B** — Screening Option
  - Blank - Standard processing
  - B - Burn-in

Device type  
BCD and Binary Counters

#### Valid Combinations

Am25LS2568/ Am25LS2569	DC, DCB, DM, DMB
	FM, FMB LC, LM, LMB PC, PCB XC, XM





#### Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

## PIN DESCRIPTION

Pin No.	Name	I/O	Description
3, 4, 5, 6	A, B, C, D	I	The four programmable data inputs.
7	CEP	I	Count Enable Parallel. Can be used to enable and inhibit counting in high speed cascaded operation. CEP must be LOW to count.
12	CET	I	Count Enable Trickle. Enables the ripple carry output for cascaded operation. Must be LOW to count.
2	CP	I	Clock Pulse. All synchronous functions occur on the LOW-to-HIGH transition of the clock.
11	LOAD	I	Enables parallel load of counter outputs from data inputs on the next clock edge. Must be HIGH to count.
1	U/D	I	Up/Down Count Control. HIGH counts up and LOW counts down.
8	ACLR	I	Asynchronous Clear. Master reset of counters to zero when ACLR is LOW, independent of the clock.
9	SCLR	I	Synchronous clear of counters to zero on the next clock edge when SCLR is LOW.
17	OE	I	A HIGH on the output control sets the four counter outputs in the high-impedance, and a LOW enables the output.
16, 15 14, 13	Y <sub>A</sub> , Y <sub>B</sub> , Y <sub>C</sub> , Y <sub>D</sub>	O	The four counter outputs.
19	RCO	O	Ripple Carry Output. Output will be LOW on the maximum count on up-count. Upon down-count, RCO is LOW at 0000.
18	CCO	O	Clock Carry Output. While counting and RCO is LOW, CCO will follow the clock HIGH-LOW-HIGH transition.

Am25LS2568/2569  
FUNCTION TABLE

MODE	INPUTS								OUTPUTS									
	LOAD	CEP	CET	U/D	ASYNC CLEAR	SYNC CLEAR	OE(1)	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	CP	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	RC	CLOCK CARRY
Clear (ASYNC)	X	X	X	1	0	X	0	X	X	X	X	X	0	0	0	0	1	1
	X	X	X	0	0	X	0	X	X	X	X	X	0	0	0	0	0	 (2)
Clear (SYNC)	X	X	X	1	1	0	0	X	X	X	X	1	0	0	0	0	1	1
	X	X	X	0	1	0	0	X	X	X	X	1	0	0	0	0	0	 (2)
Load	0	X	1	X	1	1	0	X	X	X	X	1	Q <sub>n</sub> = D <sub>n</sub>				1	1
	0	X	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	 (2)
	0	X	0	1	1	1	0	1	1	1	1(3)	1	1	1	1	1(3)	0	 (2)
Count Up	1	0	0	1	1	1	0	X	X	X	X	1	Q <sub>n+1</sub>				(4)	(5)
Count Down	1	0	0	0	1	1	0	X	X	X	X	1	Q <sub>n-1</sub>				(6)	(5)
Inhibit	1	0	1	X	1	1	0	X	X	X	X	1	N.C.				N.C.	1
	1	1	0	X	1	1	0	X	X	X	X	1	N.C.				N.C.	1
	1	1	1	X	1	1	0	X	X	X	X	1	N.C.				N.C.	1
Output Disable	X	X	X	X	X	X	1	X	X	X	X	X	Z	Z	Z	Z	N.C.	N.C.

↑ = CLOCK LOW-to-HIGH transition

X = Don't Care

D<sub>n</sub> = D<sub>0</sub> thru D<sub>3</sub> input level prior to clock transitionQ<sub>n+1</sub> = Next higher count in binary sequenceQ<sub>n-1</sub> = Next lower count in binary sequence

N.C. = No change

- Notes:
1. Register performs all correct logic for any state of OE, but OE = 0 to view outputs.
  2. Follows CLOCK if CET = CEP = 0, otherwise remains HIGH.
  3. 1001 for LS68.
  4. LOW for one full CLOCK cycle when maximum count is reached, otherwise remains HIGH.
  5. Follows CLOCK when RC = 0.
  6. LOW for one full CLOCK cycle when minimum count is reached, otherwise remains HIGH.

**ABSOLUTE MAXIMUM RATINGS**

Storage Temperature .....	-65°C to +150°C
Ambient Temperature Under Bias .....	-55°C to +125°C
Supply Voltage to Ground Potential	
Continuous .....	-0.5V to +7.0V
DC Voltage Applied to Outputs For	
High Output State .....	-0.5V to +V <sub>CC</sub> max
DC Input Voltage .....	-0.5V to +7.0V
DC Output Current, Into Outputs .....	30mA
DC Input Current .....	-30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

**OPERATING RANGES**

Commercial (C) Devices	
Temperature .....	0°C to +70°C
Supply Voltage .....	+4.75V to +5.25V
Military (M) Devices	
Temperature .....	-55°C to +125°C
Supply Voltage .....	+4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

**DC CHARACTERISTICS** over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
		V <sub>CC</sub> = MIN V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	Y <sub>i</sub>				
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = MIN V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	F <sub>CO</sub> , C <sub>CO</sub>	MIL, I <sub>OH</sub> = -1.0mA	2.4	3.4	Volts
				COM'L, I <sub>OH</sub> = -2.6mA	2.4	3.2	
			I <sub>OH</sub> = -440μA	MIL	2.5	3.4	
				COM'L	2.7	3.4	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = MIN V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 4.0mA		0.4	Volts	
			I <sub>OL</sub> = 8.0mA		0.45		
V <sub>IH</sub>	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V <sub>IL</sub>	Input LOW Level	Guaranteed input logical LOW voltage for all inputs.		MIL		0.7	Volts
				COM'L		0.8	
V <sub>i</sub>	Input Clamp Voltage	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18mA				-1.5	Volts
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4V		ACL <sub>R</sub> , OE, U/D, LOAD		-0.3	mA
				A, B, C, D, CP, C <sub>EP</sub>		-0.4	
				CET, SCL <sub>R</sub>		-0.65	
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7V				20	μA
I <sub>i</sub>	Input HIGH Current	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0V				0.1	mA
I <sub>OZ</sub>	Off-State (High-Impedance) Output Current	V <sub>CC</sub> = MAX		V <sub>O</sub> = 0.4V		-20	μA
				V <sub>O</sub> = 2.4V		20	
I <sub>SC</sub>	Output Short Circuit Current (Note 3)	V <sub>CC</sub> = MAX		-15		-85	mA
I <sub>CC</sub>	Power Supply Current (Note 4)	V <sub>CC</sub> = MAX			28	43	mA

- Notes: 1. Typical limits are at V<sub>CC</sub> = 5.0V, 25°C ambient and maximum loading.  
 2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.  
 3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.  
 4. OE = HIGH, all other inputs = GND, all outputs open.

**SWITCHING CHARACTERISTICS** ( $T_A = +25^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V}$ )

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t <sub>PLH</sub>	Clock to Any Q; $\overline{\text{Load}} = \text{LOW}$	C <sub>L</sub> = 15pF R <sub>L</sub> = 2.0k $\Omega$		12	18	ns
t <sub>PHL</sub>				14	21	
t <sub>PLH</sub>	Clock to Any Q; $\overline{\text{Load}} = \text{HIGH}$			12	18	ns
t <sub>PHL</sub>				14	21	
t <sub>PLH</sub>	$\overline{\text{CET}}$ to $\overline{\text{RCO}}$			11	16	ns
t <sub>PHL</sub>				6	10	
t <sub>PLH</sub>	U/ $\overline{\text{D}}$ to $\overline{\text{RCO}}$			15	23	ns
t <sub>PHL</sub>				13	20	
t <sub>PLH</sub>	Clock to $\overline{\text{RCO}}$			24	35	ns
t <sub>PHL</sub>				18	26	
t <sub>PLH</sub>	Clock to $\overline{\text{OCF}}$			10	15	ns
t <sub>PHL</sub>				10	15	
t <sub>PLH</sub>	$\overline{\text{CET}}$ or $\overline{\text{CEP}}$ to $\overline{\text{RCO}}$			10	15	ns
t <sub>PHL</sub>				17	25	
t <sub>PLH</sub>	$\overline{\text{ACL}}$ to Any Q		N.A.	N.A.	ns	
t <sub>PHL</sub>			17	26		
t <sub>s</sub>	Set-up	A, B, C, D	22			ns
		$\overline{\text{SCLR}}$	20			
		$\overline{\text{Load}}$	30			
		U/ $\overline{\text{D}}$	30			
		$\overline{\text{CET}}$ , $\overline{\text{CEP}}$	25			
t <sub>s</sub>	$\overline{\text{SCLR}}$ Recovery (inactive) to Clock		30			ns
t <sub>h</sub>	Data Hold		0			ns
f <sub>max</sub>	Maximum Clock Frequency (Note 1)		25	40		MHz
t <sub>pw</sub>	Clock Pulse Width		25			ns
t <sub>PZH</sub>	$\overline{\text{OE}}$ to Any Q; Enable				11	ns
t <sub>PZL</sub>					19	
t <sub>PHZ</sub>	$\overline{\text{OE}}$ to Any Q; Disable	C <sub>L</sub> = 5.0pF			18	ns
t <sub>PLZ</sub>		R <sub>L</sub> = 2.0k $\Omega$			24	

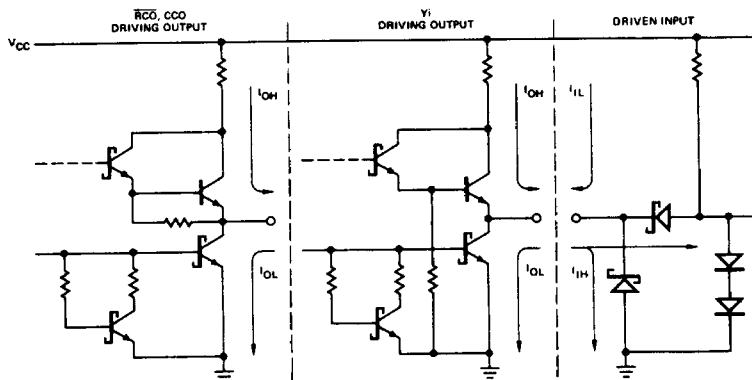
Note 1. Per industry convention, f<sub>max</sub> is the worst case value of the maximum device operating frequency with no constraints on t<sub>r</sub>, t<sub>f</sub>, pulse width or duty cycle.

**SWITCHING CHARACTERISTICS** over operating range unless otherwise specified\*

Parameters	Description	Test Conditions	COMMERCIAL		MILITARY		Units
			Am25LS		Am25LS		
			Min	Max	Min	Max	
t <sub>PLH</sub>	Clock to Any Q; $\overline{\text{Load}} = \text{LOW}$	$C_L = 50\text{pF}$ $R_L = 2.0\text{K}\Omega$		22		24	ns
t <sub>PHL</sub>				29		35	
t <sub>PLH</sub>	Clock to Any Q; $\overline{\text{Load}} = \text{HIGH}$			22		24	ns
t <sub>PHL</sub>				29		35	
t <sub>PLH</sub>	$\overline{\text{CE}}\overline{\text{T}}$ to $\overline{\text{RCO}}$			18		19	ns
t <sub>PHL</sub>				17		21	
t <sub>PLH</sub>	U/ $\overline{\text{D}}$ to $\overline{\text{RCO}}$			26		28	ns
t <sub>PHL</sub>				26		30	
t <sub>PLH</sub>	Clock to $\overline{\text{RCO}}$			39		40	ns
t <sub>PHL</sub>				34		39	
t <sub>PLH</sub>	Clock to CCO			17		18	ns
t <sub>PHL</sub>				22		27	
t <sub>PLH</sub>	$\overline{\text{CE}}\overline{\text{T}}$ or $\overline{\text{CE}}\overline{\text{P}}$ to CCO			16		17	ns
t <sub>PHL</sub>				36		45	
t <sub>PLH</sub>	$\overline{\text{ACL}}\overline{\text{R}}$ to Any Q		N.A.		N.A.	ns	
t <sub>PHL</sub>			37		45		
t <sub>s</sub>	Set-up	A, B, C, D	29		35	ns	
		SCLR	25		30		
		Load	38		45		
		U/ $\overline{\text{D}}$	38		45		
		$\overline{\text{CE}}\overline{\text{T}}$ , $\overline{\text{CE}}\overline{\text{P}}$	33		40		
t <sub>s</sub>	SCLR Recovery (inactive) to Clock	39		50	ns		
t <sub>h</sub>	Data Hold	0		5	ns		
t <sub>max</sub>	Maximum Clock Frequency (Note 1)	20		18	MHz		
t <sub>pw</sub>	Clock Pulse Width	31		37	ns		
t <sub>ZH</sub>	$\overline{\text{OE}}$ to Any Q; Enable		16		20	ns	
t <sub>ZL</sub>			26		34		
t <sub>HZ</sub>	$\overline{\text{OE}}$ to Any Q; Disable	$C_L = 5.0\text{pF}$ $R_L = 2.0\text{K}\Omega$	20		22	ns	
t <sub>LZ</sub>			30		36		

\*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.  
N.A. not applicable.

### Am25LS2568/2569 LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000270

Note: Actual current flow direction shown.

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