



STFV4N150

N-CHANNEL 1500V - 5Ω - 4A TO-220FH Very High Voltage PowerMESH™ MOSFET

Table 1: General Features

TYPE	V _{DSS}	R _{DS(on)}	I _D	P _w
STFV4N150	1500 V	< 7 Ω	4 A	40 W

- TYPICAL R_{DS(on)} = 5 Ω
- AVALANCHE RUGGEDNESS
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- HIGH SPEED SWITCHING
- FULLY PLASTIC TO-220 PACKAGE
- CREEPAGE DISTANCE PATH IS > 4mm

DESCRIPTION

Using the well consolidated high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of Power MOSFETs with outstanding performances. The strengthened layout coupled with the Company's proprietary edge termination structure, gives the lowest R_{DS(on)} per area, unrivalled gate charge and switching characteristics. The creepage path is what makes this package unique from TO-220FP. The creepage distance path between each lead and between the leads and the heatsink has been increased to >4.0mm, making this package met all stringent safety norms in high voltage applications.

APPLICATIONS

- SWITCH MODE POWER SUPPLIES

Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STFV4N150	FV4N150	TO-220FH	TUBE

Figure 1: Package

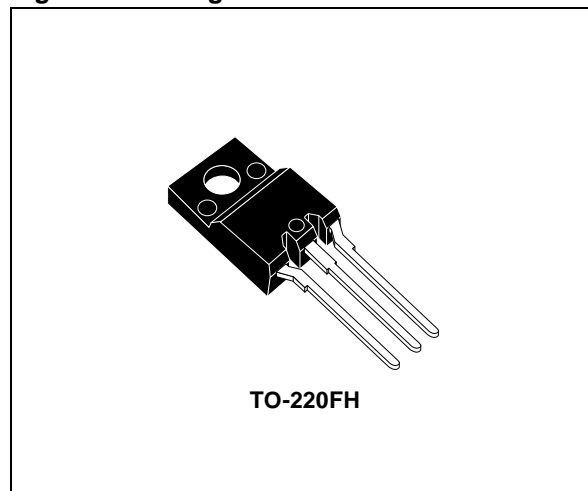


Figure 2: Internal Schematic Diagram

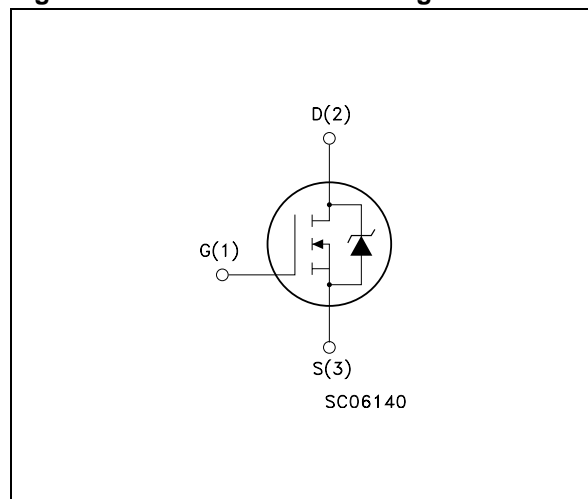


Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage ($V_{GS} = 0$)	1500	V
V_{DGR}	Drain-gate Voltage ($R_{GS} = 20 \text{ k}\Omega$)	1500	V
V_{GS}	Gate- source Voltage	± 30	V
I_D	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	4	A
I_D	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	2.5	A
$I_{DM}(\bullet)$	Drain Current (pulsed)	12	A
P_{TOT}	Total Dissipation at $T_C = 25^\circ\text{C}$	40	W
	Derating Factor	0.32	W/ $^\circ\text{C}$
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150	$^\circ\text{C}$

(●) Pulse width limited by safe operating area

(*) Limited only by maximum temperature allowed

Table 4: Thermal Data

Rthj-case	Thermal Resistance Junction-case Max	3.12	$^\circ\text{C}/\text{W}$
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	$^\circ\text{C}/\text{W}$

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	4	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50 \text{ V}$)	350	mJ

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^\circ\text{C}$ UNLESS OTHERWISE SPECIFIED)**Table 6: On /Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1 \text{ mA}$, $V_{GS} = 0$	1500			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$, $T_C = 125^\circ\text{C}$			10 500	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 30 \text{ V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10 \text{ V}$, $I_D = 2 \text{ A}$		5	7	Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)

Table 7: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	$V_{DS} = 30\text{ V}$, $I_D = 2\text{ A}$		3.5		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$		1300 120 12		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off-Delay Time Fall Time	$V_{DD} = 750\text{ V}$, $I_D = 2\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 17)		35 30 45 45		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 600\text{ V}$, $I_D = 4\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 20)		30 10 9	50	nC nC nC

Table 8: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				4 12	A A
V_{SD} (1)	Forward On Voltage	$I_{SD} = 4\text{ A}$, $V_{GS} = 0$			2	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 45\text{ V}$ (see Figure 18)		510 3 12		ns μC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 45\text{ V}$, $T_j = 150^\circ\text{C}$ (see Figure 18)		650 4 12.6		ns μC A

(1) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

(2) Pulse width limited by safe operating area.

Figure 3: Safe Operating Area

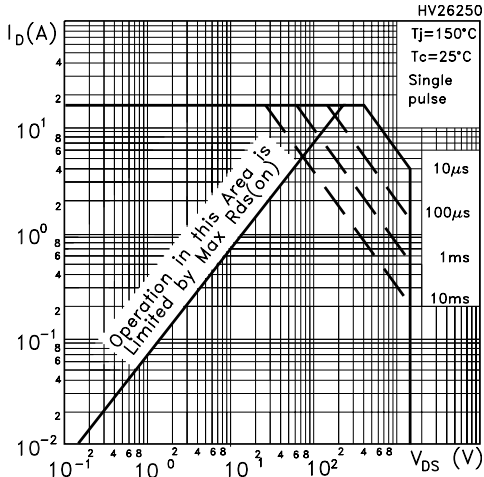


Figure 4: Output Characteristics

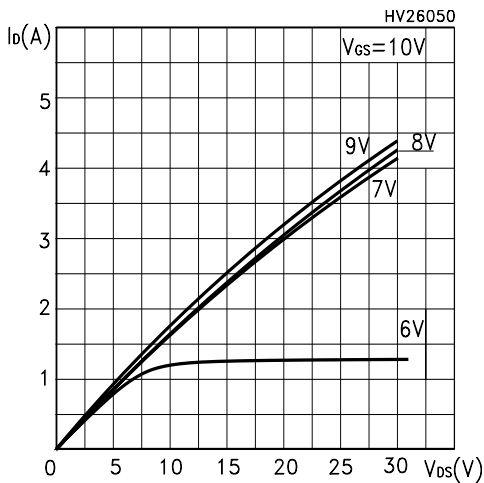


Figure 5: Transconductance

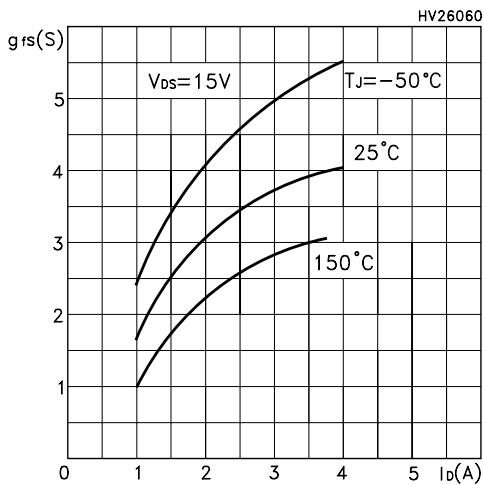


Figure 6: Thermal Impedance

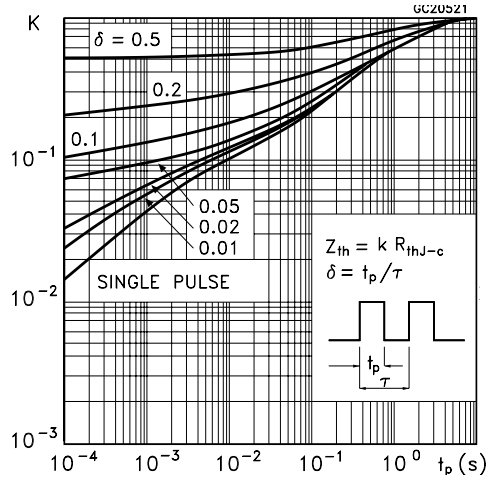


Figure 7: Transfer Characteristics

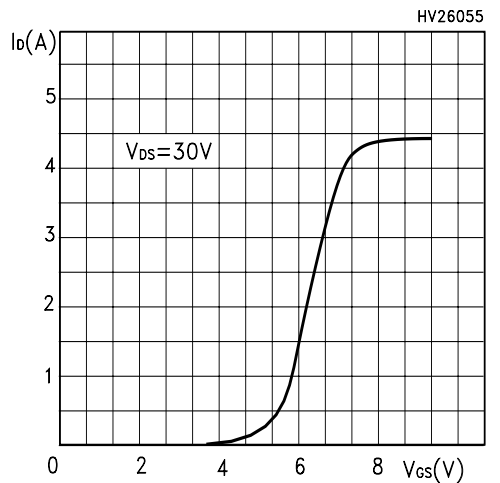


Figure 8: Static Drain-source On Resistance

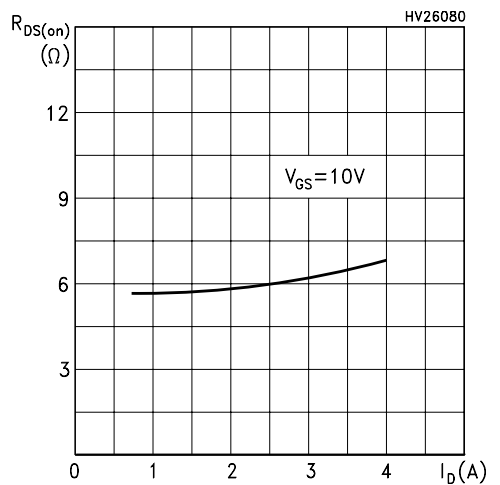


Figure 9: Gate Charge vs Gate-source Voltage

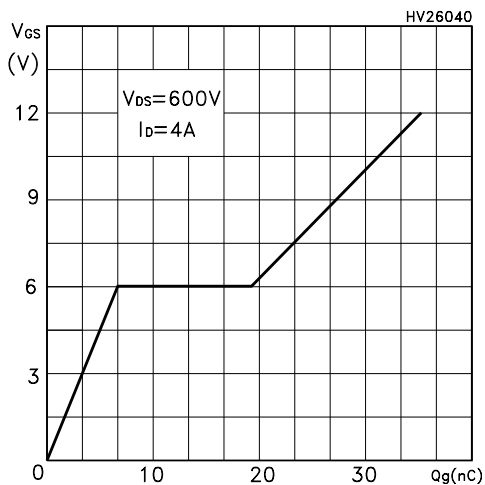


Figure 10: Normalized Gate Threshold Voltage vs Temperature

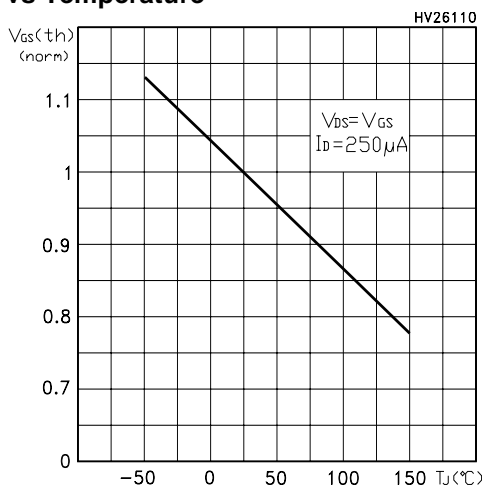


Figure 11: Source-Drain Diode Forward Characteristics

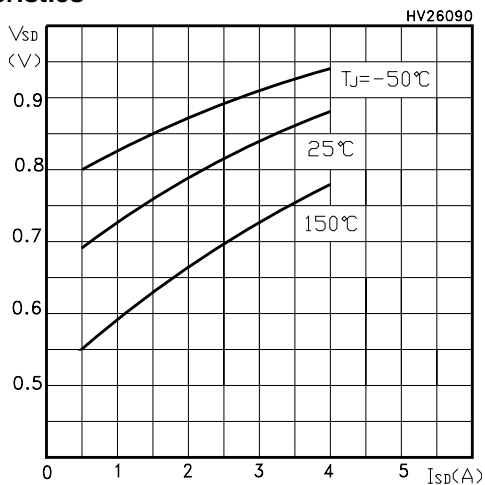


Figure 12: Capacitance Variations

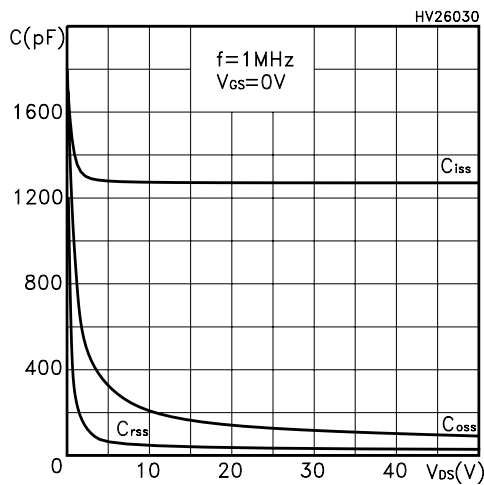


Figure 13: Normalized On Resistance vs Temperature

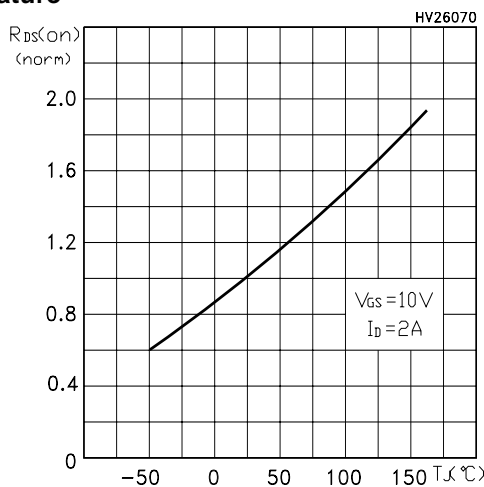


Figure 14: Normalized BVds vs Temperature

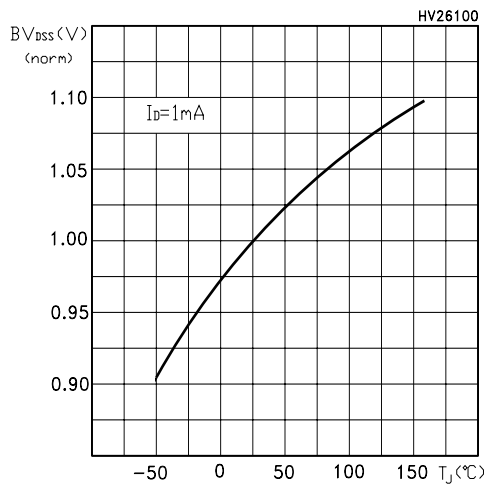


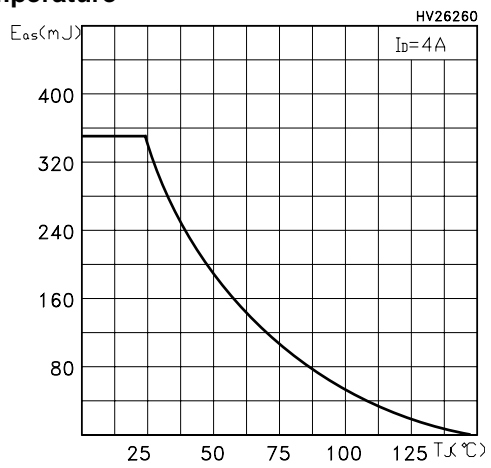
Figure 15: Maximum Avalanche Energy vs Temperature

Figure 16: Unclamped Inductive Load Test Circuit

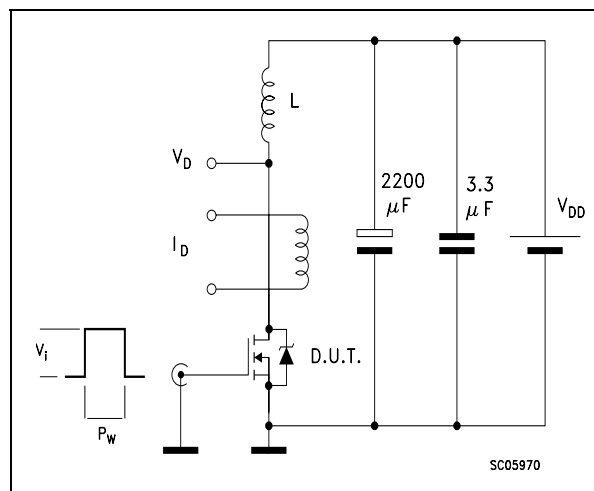


Figure 17: Switching Times Test Circuit For Resistive Load

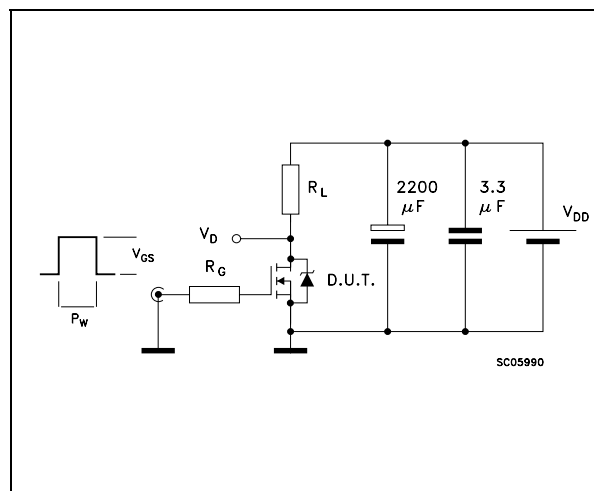


Figure 18: Test Circuit For Inductive Load Switching and Diode Recovery Times

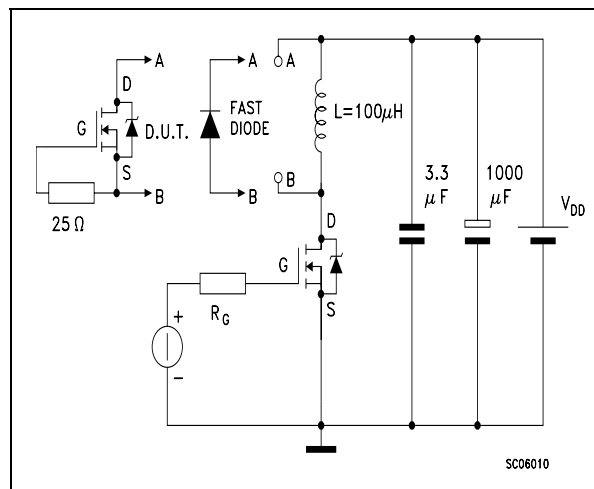


Figure 19: Unclamped Inductive Waveform

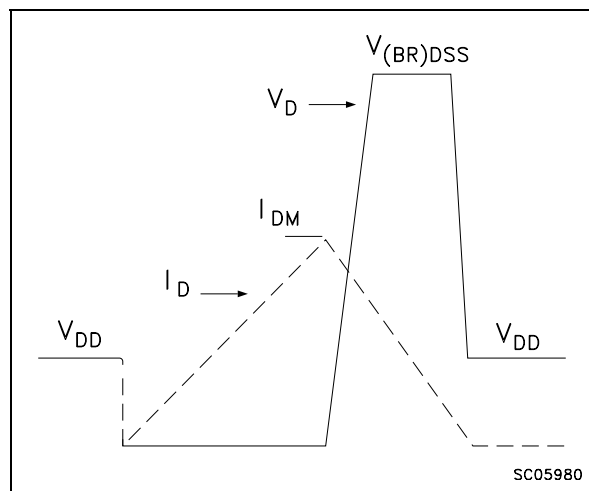


Figure 20: Gate Charge Test Circuit

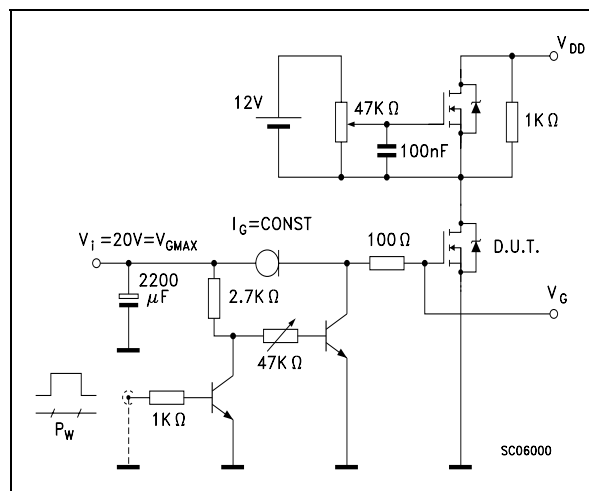


Figure 21: Test Circuit For Inductive Load Switching and Diode Recovery Times



TO-220FH (Fully plastic High voltage) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.3		1.8	0.051		0.070
F2	1.3		1.8	0.051		0.070
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L5		3.4			0.134	
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
L8	14.5		15	0.570		0.590
L9		2.4			0.094	

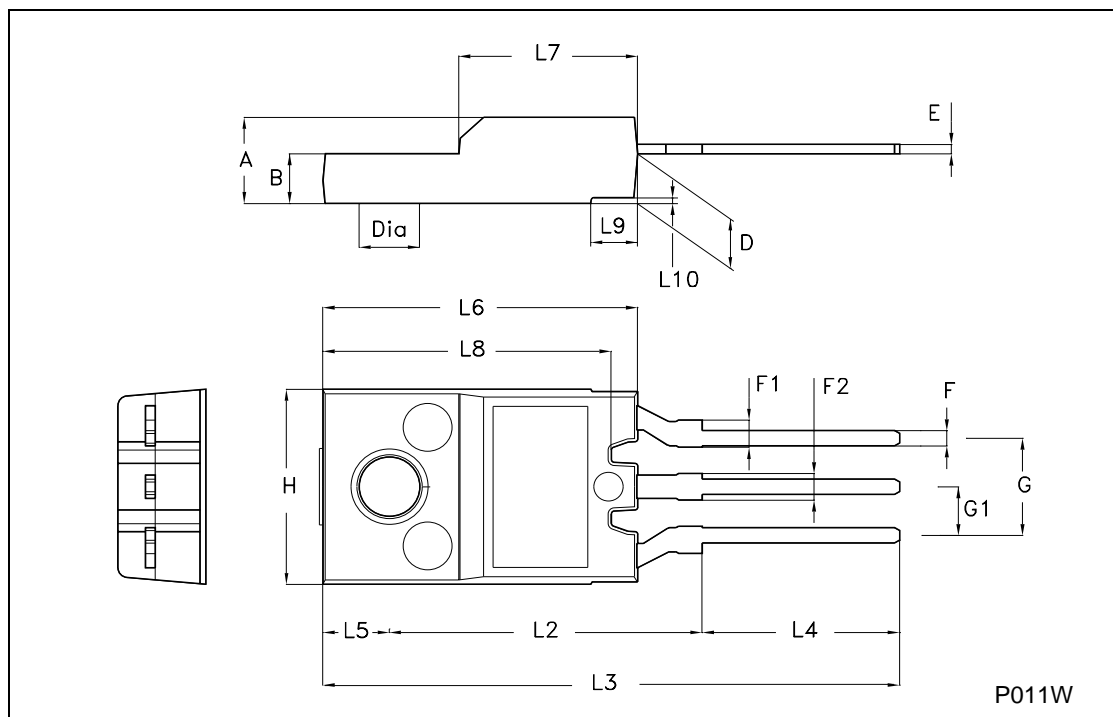


Table 9: Revision History

Date	Revision	Description of Changes
07-Jul-2005	1	First release.

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics

All other names are the property of their respective owners

© 2005 STMicroelectronics - All Rights Reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America