32K x 8 SRAM

SRAM MEMORY ARRAY

AVAILABLE AS MILITARY SPECIFICATIONS

•SMD 5962-88662
•MIL-STD-883

FEATURES

- Access Times: 12, 15, 20, 25, 35, 45, 55, 70, & 100ns
- Battery Backup: 2V data retention
- Low power standby
- High-performance, low-power CMOS double-metal process
- Single +5V (±10%) Power Supply
- Easy memory expansion with CE\
- All inputs and outputs are TTL compatible

OPTIONS MARKING

- Timing

12ns access[1]	-12
15ns access[1]	-15
20ns access	-20
25ns access	-25
35ns access	-35
45ns access	-45
55ns access[2]	-55
70ns access[2]	-70
100ns access	-100

- Package(s)[3]

Ceramic DIP (300 mil)	C	No. 108
Ceramic DIP (600 mil)	CW	No. 110
Ceramic LCC (28 leads)	EC	No. 204
Ceramic LCC (32 leads)	ECW	No. 208
Ceramic LCC	ECJ	No. 605
Ceramic Flat Pack	F	No. 302
Ceramic SOJ	DCJ	No. 500

- Operating Temperature Ranges

Military -55°C to +125°C	XT
Industrial -40°C to +85°C	IT

- 2V data retention/low power L

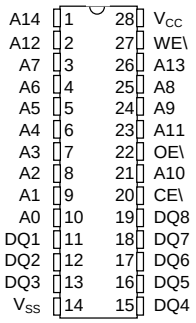
NOTES:

1. -12 available in IT only.
2. Electrical characteristics identical to those provided for the 45ns access devices.
3. Plastic SOJ (DJ Package) is available on the AS5C2568 datasheet.

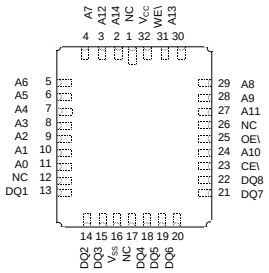
For more products and information
please visit our web site at
www.austinsemiconductor.com

PIN ASSIGNMENT (Top View)

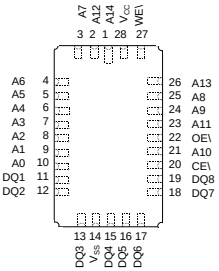
28-PIN SOJ (DCJ)
28-Pin DIP (C, CW)



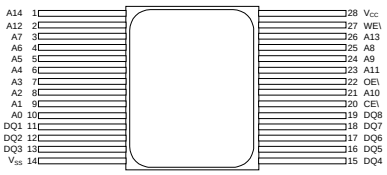
32-Pin LCC (ECW)



28-Pin LCC (EC)



28-Pin Flat Pack (F)



GENERAL DESCRIPTION

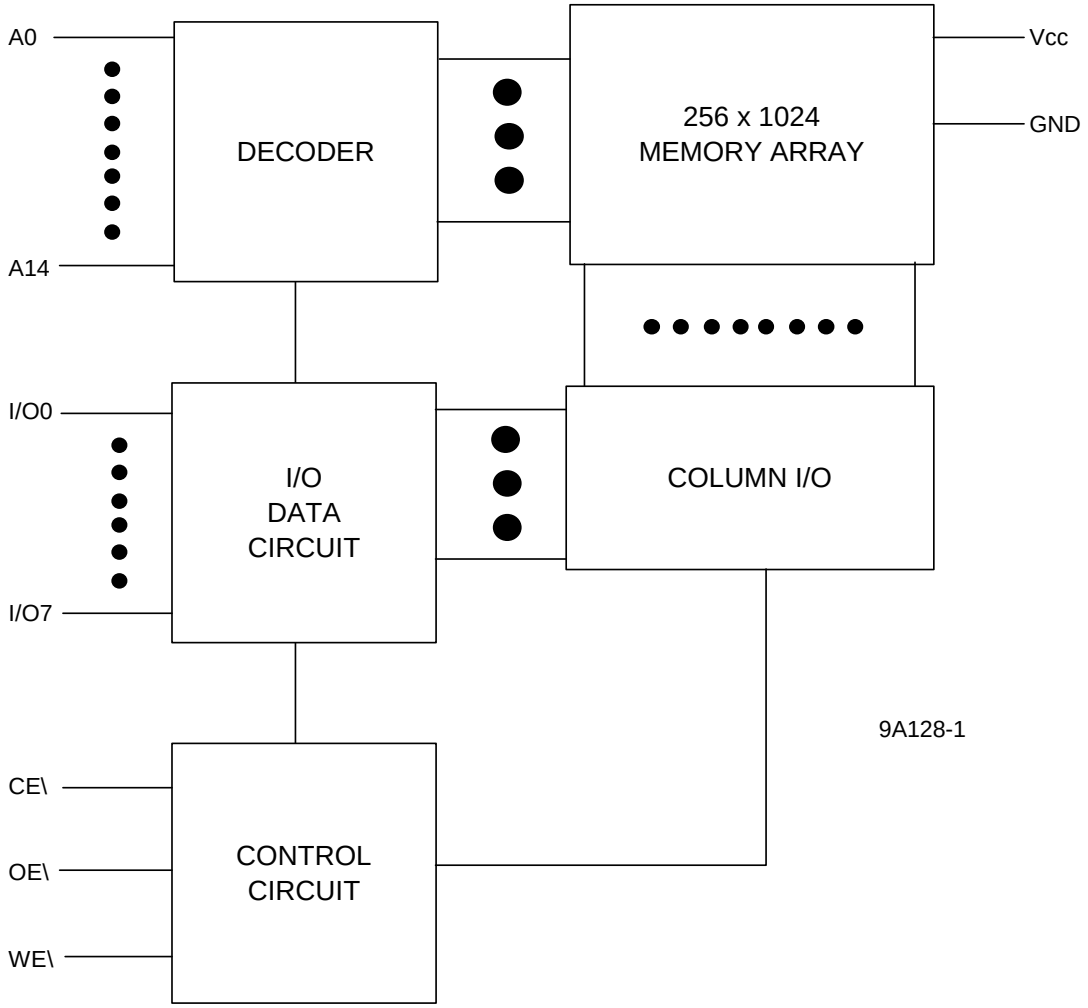
The Austin Semiconductor SRAM family employs high-speed, low power CMOS designs using a four-transistor memory cell. These SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Austin Semiconductor offers chip enable (CE\) and output enable (OE\) capability. These enhancements can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable (WE\) and CE\ inputs are both LOW. Reading is accomplished when WE\ remains HIGH and CE\ and OE\ go LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

The "L" version provides a battery backup/low voltage data retention mode, offering 2mW maximum power dissipation at 2 volts. All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	OE\	CE\	WE\	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Input or DQ Relative to Vss.....-0.5V to Vcc +0.5V
Voltage on Vcc Supply Relative to Vss.....-1V to +7V
Storage Temperature.....-65°C to +150°C
Power Dissipation.....1W
Short Circuit Output Current.....50mA
Lead Temperature (soldering 10 seconds).....+260°C
Max. Junction Temperature.....+175°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-55^oC \leq T_C \leq 125^oC$ or -40^oC to $+85^oC$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYM	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+0.5	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1,2
Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$	IL_I	-10	10	µA	
Output Leakage Current	Output(s) disabled $0V \leq V_{OUT} \leq V_{CC}$	ILo	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

				MAX							
DESCRIPTION		CONDITIONS	SYM	-12	-15	-20	-25	-35	-45	UNITS	NOTES
Power Supply Current: Operating		CE\ $\leq V_{IL}$; Vcc = MAX f = MAX = 1/ ^tRC (MIN) Output Open	Icc	190	180	170	160	150	150	mA	3
Power Supply Current: Standby	TTL	CE\ $\leq V_{IH}$; Outputs Open Vcc = MAX	I_{SBT}	60	50	40	35	35	35	mA	
	CMOS	CE\ $\geq$ Vcc-0.2V; Vcc = MAX $V_{IN} \leq$ +0.2V or $\geq$ Vcc-0.2V; f = 0 Hz, Outputs Open	I_{SBC}	20	20	20	20	20	20	mA	
		"L" Version Only	I_{SBC2}	4	4	4	4	4	4	mA	

CAPACITANCE

PARAMETER	CONDITIONS	SYM	MAX	UNITS	NOTES
Input Capacitance	$T_A = 25^oC$, f = 1MHz Vcc = 5V	C_{IN}	11	pF	4
Output Capacitance		C_{IO}	11	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($-55^{o}C \leq T_C \leq 125^{o}C$ or $-40^{o}C$ to $+85^{o}C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	SYM	-12		-15		-20		-25		-35		-45		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ CYCLE															
READ cycle time	t_{RC}	12		15		20		25		35		45		ns	
Address access time	t_{AA}		12		15		20		25		35		45	ns	
Chip enable access time	t_{ACE}		12		15		20		25		35		45	ns	
Output hold from address change	t_{OH}	2		3		3		3		3		3		ns	
Chip enable to output in Low-Z	t_{LZCE}	2		3		3		3		3		3		ns	7
Chip disable to output in High-Z	t_{HZCE}		7		10		10		15		35		20	ns	6, 7
Output enable to access time	t_{AOE}		6		8		10		15		20		20	ns	
Output enable to output in Low-Z	t_{LZOE}	0		0		0		0		2		0		ns	
Output disable to output in High-Z	t_{HZOE}		7		10		10		15		35		20	ns	6
WRITE CYCLE															
WRITE cycle time	t_{WC}	12		15		20		25		35		45		ns	
Chip enable to end of write	t_{CW}	10		12		15		20		30		40		ns	
Address valid to end of write	t_{AW}	10		12		15		20		30		40		ns	
Address setup time	t_{AS}	0		0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	2		0		0		0		0		0		ns	
WRITE pulse width	t_{WP}	10		12		15		20		30		40		ns	
Data setup time	t_{DS}	8		10		10		15		20		20		ns	
Data hold time	t_{DH}	0		0		0		0		0		3		ns	
Write disable to output in Low-Z	t_{LZWE}	0		0		0		3		3		3		ns	7
Write enable to output in High-Z	t_{HZWE}		7		10		10		15		35		20	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See figures 1 & 2

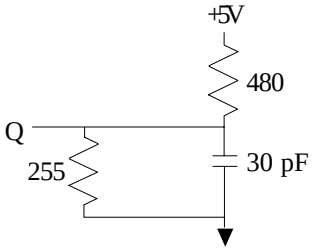


Fig. 1
OUTPUT LOAD
EQUIVALENT

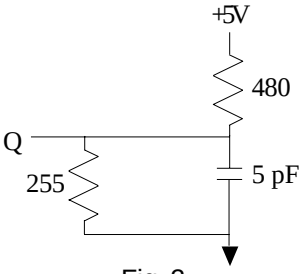


Fig. 2
OUTPUT LOAD
EQUIVALENT

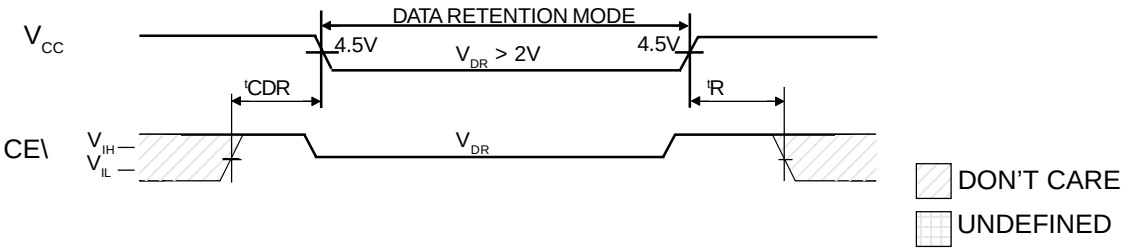
NOTES

1. All voltages referenced to V_{SS} (GND).
2. -3V for pulse width < 20ns
3. I_{CC} is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and
   $f = \frac{1}{{}^{t}RC\ (MIN)}$ Hz.
4. This parameter is guaranteed but not tested.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^{t}HZCE$, ${}^{t}HZOE$ and ${}^{t}HZWE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV typical from steady state voltage, allowing for actual tester RC time constant.
7. At any given temperature and voltage condition, ${}^{t}HZCE$ is less than ${}^{t}LZCE$, and ${}^{t}HZWE$ is less than ${}^{t}LZWE$.
8. WE\ is HIGH for READ cycle.
9. Device is continuously selected. Chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^{t}RC$ = Read Cycle Time.
12. Chip enable (CE\) and write enable (WE\) can initiate and terminate a WRITE cycle.

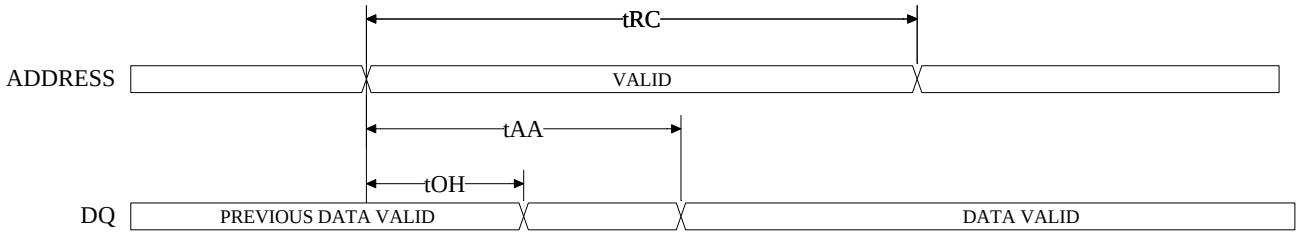
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS	SYM	MIN	MAX	UNITS	NOTES
V_{CC} for Retention Data		V_{DR}	2		V	
Data Retention Current	CE\ ≥ (V_{CC}-0.2V) V_{IN} ≥ (V_{CC}-0.2V) or ≤ 0.2V	I_{CCDR}		1	mA	
Chip Deselect to Data Retention Time		t_{CDR}	0	--	ns	4
Operation Recovery Time		t_R	t_{RC}		ns	4, 11

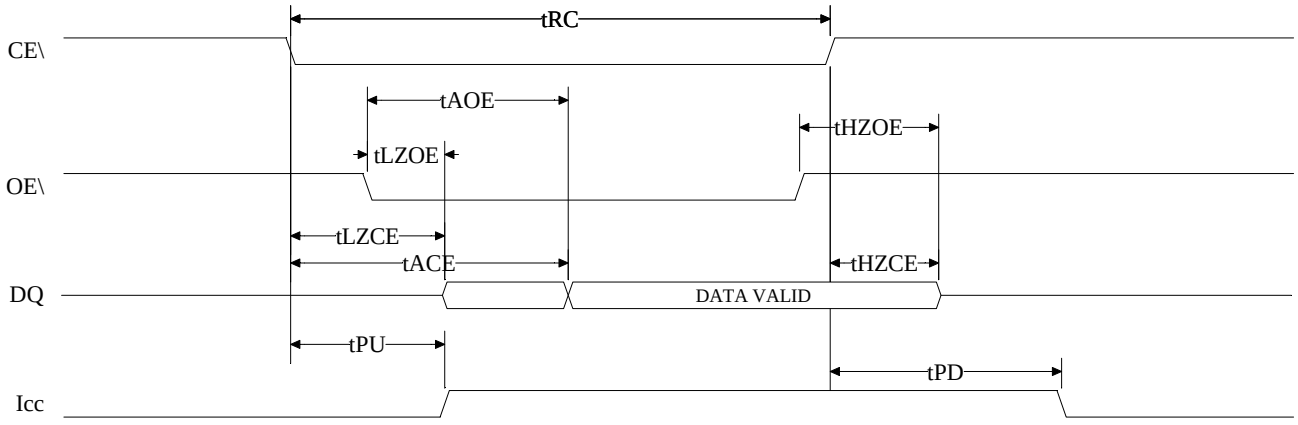
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]

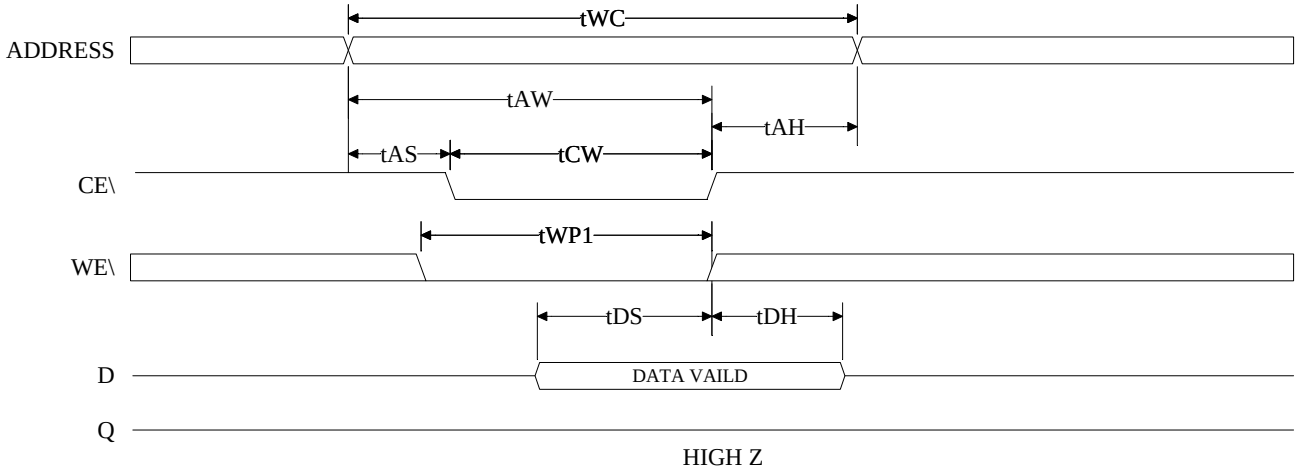


READ CYCLE NO. 2 [7, 8, 10, 12]



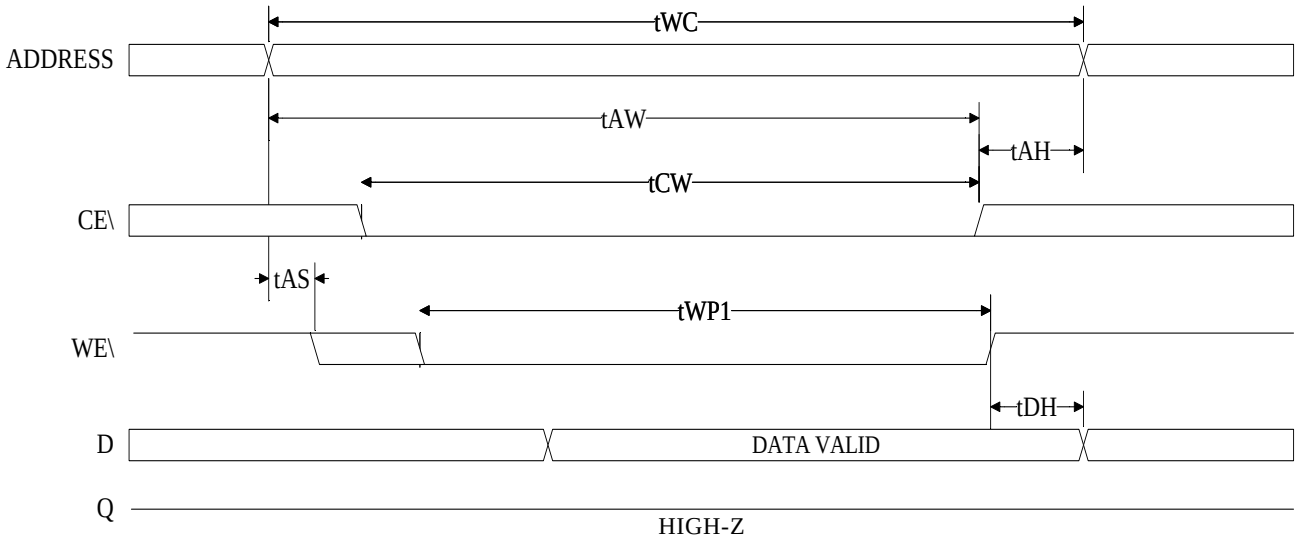
WRITE CYCLE NO. 1 [12]

(Chip Enabled Controlled)



WRITE CYCLE NO. 2 [7, 12]

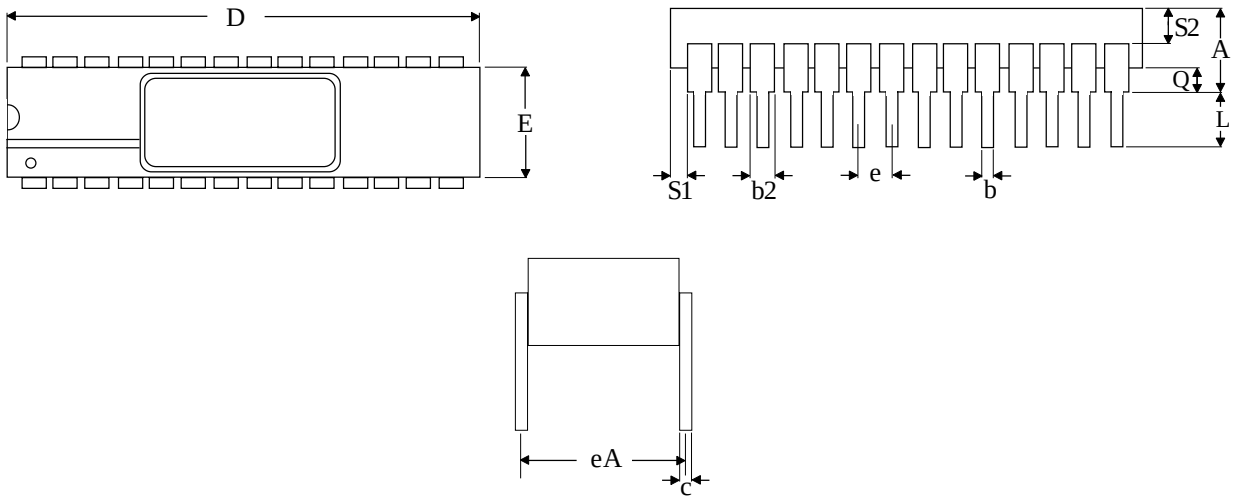
(Write Enabled Controlled)



NOTE: Output enable (OE\) is inactive (HIGH).

MECHANICAL DEFINITIONS*

ASI Case #108 (Package Designator C)
SMD 5962-88662, Case Outline N



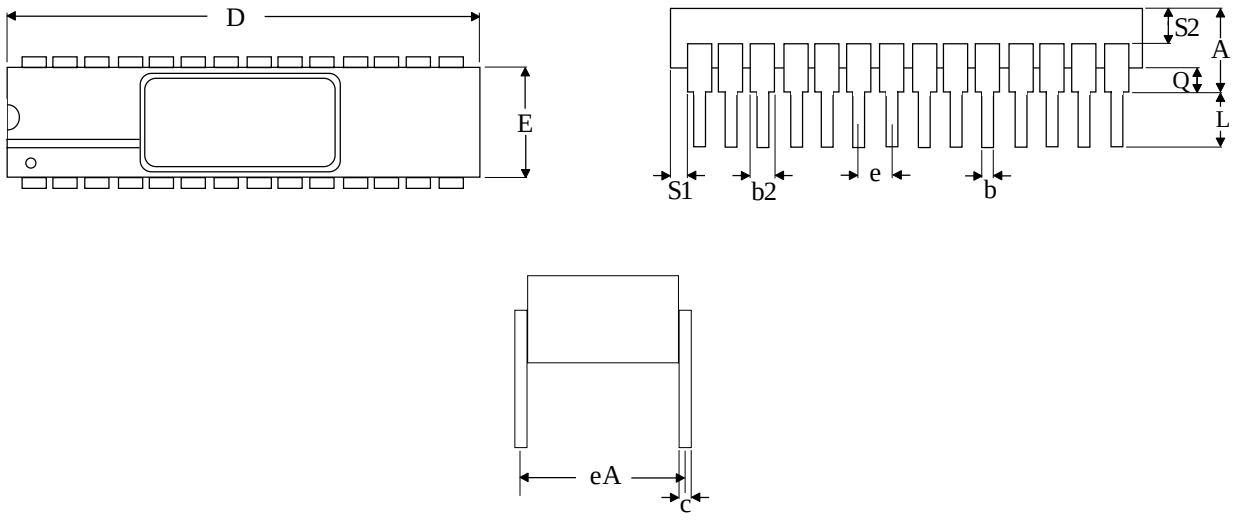
SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	---	0.225
b	0.014	0.026
b2	0.045	0.065
c	0.008	0.018
D	---	1.485
E	0.240	0.310
eA	0.300 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.070
S1	0.005	---
S2	0.005	---

NOTE: *These dimensions are per the SMD. ASI's package dimensional limits may differ, but they will be within the SMD limits.*

**** All measurements are in inches.***

MECHANICAL DEFINITIONS*

ASI Case #110 (Package Designator CW)
SMD 5962-88662, Case Outline X



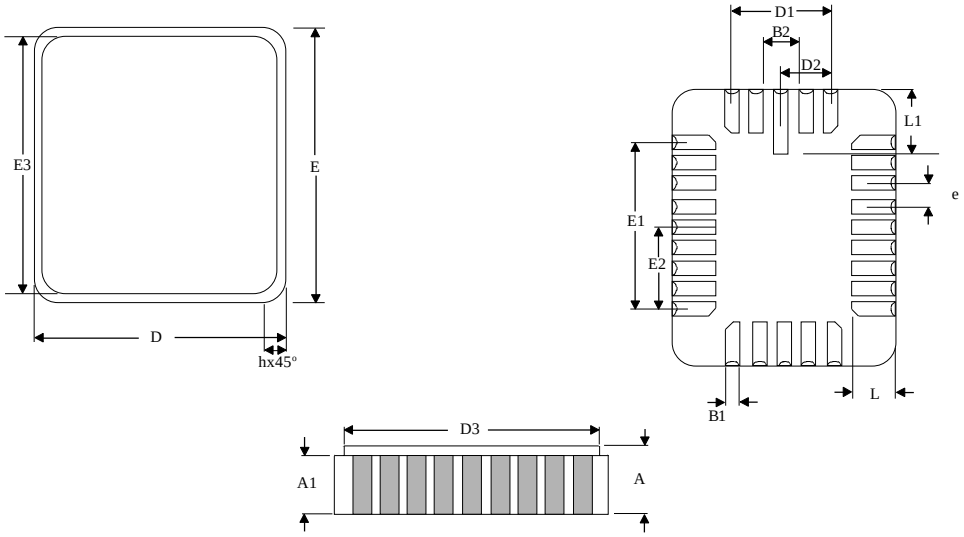
SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	---	0.232
b	0.014	0.026
b2	0.045	0.065
c	0.008	0.018
D	---	1.490
E	0.500	0.610
eA	0.600 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	---
S2	0.005	---

NOTE: *These dimensions are per the SMD. ASI's package dimensional limits may differ, but they will be within the SMD limits.*

**** All measurements are in inches.***

MECHANICAL DEFINITIONS*

ASI Case #204 (Package Designator EC)
SMD 5962-88662, Case Outline U



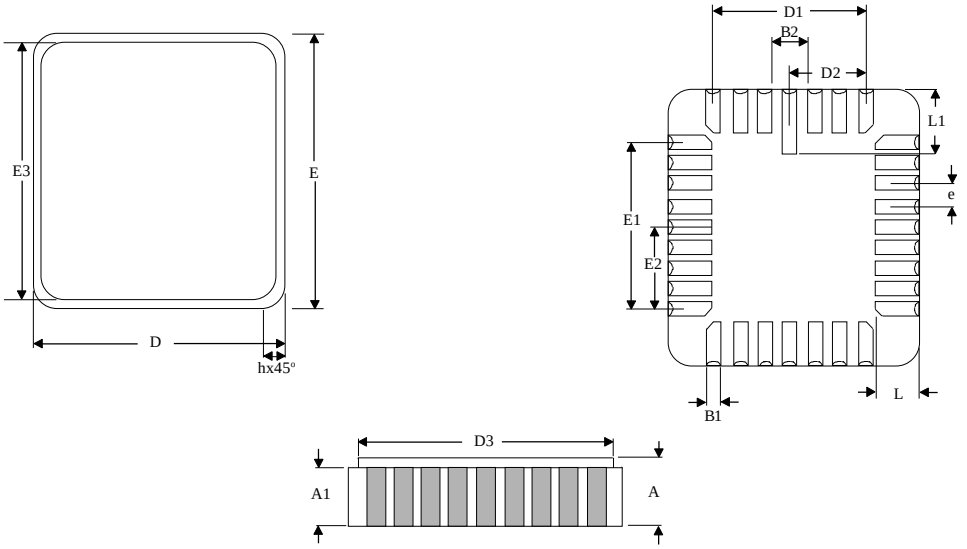
SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.060	0.120
A1	0.050	0.088
B1	0.022	0.028
B2	0.072 REF	
D	0.342	0.358
D1	0.200 BSC	
D2	0.100 BSC	
D3	---	0.358
E	0.540	0.560
E1	0.400 BSC	
E2	0.200 BSC	
E3	---	0.558
e	0.050 BSC	
h	0.040 REF	
L	0.045	0.055
L1	0.075	0.095

NOTE: *These dimensions are per the SMD. ASI's package dimensional limits may differ, but they will be within the SMD limits.*

**** All measurements are in inches.***

MECHANICAL DEFINITIONS*

ASI Case #208 (Package Designator ECW)
SMD 5962-88662, Case Outline Y



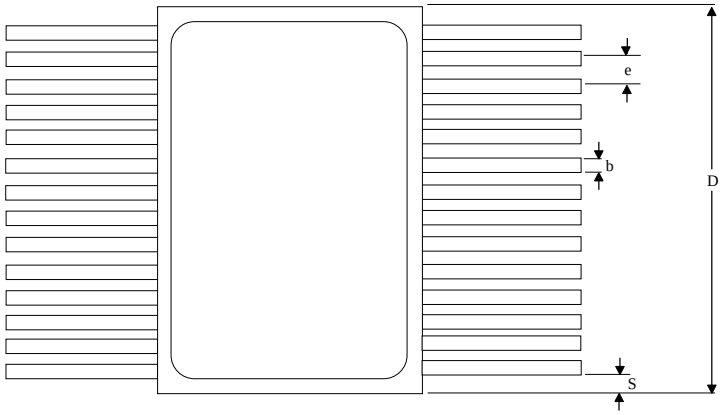
SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.060	0.120
A1	0.050	0.088
B1	0.022	0.028
B2	0.072 REF	
D	0.442	0.458
D1	0.300 BSC	
D2	0.150 BSC	
D3	---	0.458
E	0.540	0.560
E1	0.400 BSC	
E2	0.200 BSC	
E3	---	0.558
e	0.050 BSC	
h	0.040 REF	
L	0.045	0.055
L1	0.075	0.095

NOTE: *These dimensions are per the SMD. ASI's package dimensional limits may differ, but they will be within the SMD limits.*

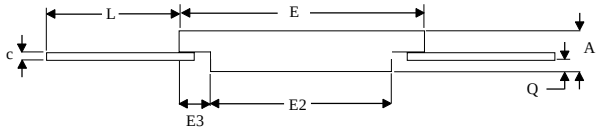
**** All measurements are in inches.***

MECHANICAL DEFINITIONS*

ASI Case #302 (Package Designator F)
SMD 5962-88662, Case Outline T



Top View



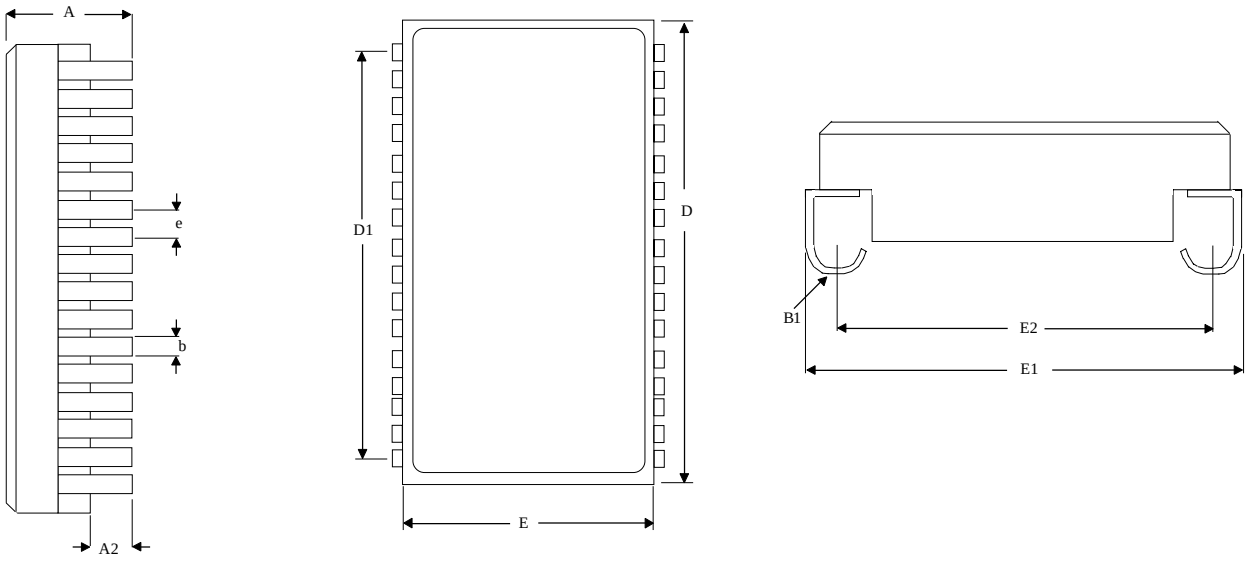
SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.090	0.130
b	0.015	0.019
c	0.004	0.009
D	---	0.740
E	0.380	0.420
E2	0.180	---
E3	0.030	---
e	0.050 BSC	
L	0.250	0.370
Q	0.026	0.045
S	0.000	0.045

NOTE: *These dimensions are per the SMD. ASI's package dimensional limits may differ, but they will be within the SMD limits.*

**** All measurements are in inches.***

MECHANICAL DEFINITIONS*

ASI Case #500 (Package Designator DCJ)



SYMBOL	ASI SPECIFICATIONS	
	MIN	MAX
A	0.132	0.144
A2	0.026	0.036
B1	0.030	0.040
b	0.015	0.019
D	0.712	0.728
D1	0.640	0.660
E	0.405	0.415
E1	0.435	0.445
E2	0.360	0.380
e	0.045	0.055

**** All measurements are in inches.***

ORDERING INFORMATION

EXAMPLE: MT5C2568CW-25L/XT

Device Number	Package Type	Speed ns	Options**	Process
MT5C2568	C	-12	L	/*
MT5C2568	CW	-12	L	/*
MT5C2568	C	-15	L	/*
MT5C2568	CW	-15	L	/*
MT5C2568	C	-20	L	/*
MT5C2568	CW	-20	L	/*
MT5C2568	C	-25	L	/*
MT5C2568	CW	-25	L	/*
MT5C2568	C	-35	L	/*
MT5C2568	CW	-35	L	/*
MT5C2568	C	-45	L	/*
MT5C2568	CW	-45	L	/*
MT5C2568	C	-55	L	/*
MT5C2568	CW	-55	L	/*
MT5C2568	C	-70	L	/*
MT5C2568	CW	-70	L	/*
MT5C2568	CW	-100	L	/*

EXAMPLE: MT5C2568ECW-15L/IT

Device Number	Package Type	Speed ns	Options**	Process
MT5C2568	EC	-12	L	/*
MT5C2568	ECW	-12	L	/*
MT5C2568	EC	-15	L	/*
MT5C2568	ECW	-15	L	/*
MT5C2568	EC	-20	L	/*
MT5C2568	ECW	-20	L	/*
MT5C2568	EC	-25	L	/*
MT5C2568	ECW	-25	L	/*
MT5C2568	EC	-35	L	/*
MT5C2568	ECW	-35	L	/*
MT5C2568	EC	-45	L	/*
MT5C2568	ECW	-45	L	/*
MT5C2568	EC	-55	L	/*
MT5C2568	ECW	-55	L	/*
MT5C2568	EC	-70	L	/*
MT5C2568	ECW	-70	L	/*
MT5C2568	ECW	-100	L	/*

EXAMPLE: MT5C2568F-55/XT

Device Number	Package Type	Speed ns	Options**	Process
MT5C2568	F	-12	L	/*
MT5C2568	F	-15	L	/*
MT5C2568	F	-20	L	/*
MT5C2568	F	-25	L	/*
MT5C2568	F	-35	L	/*
MT5C2568	F	-45	L	/*
MT5C2568	F	-55	L	/*
MT5C2568	F	-70	L	/*
MT5C2568	F	-100	L	/*

EXAMPLE: MT5C2568DCJ-70L/IT

Device Number	Package Type	Speed ns	Options**	Process
MT5C2568	DCJ	-12	L	/* /*
MT5C2568	DCJ	-15	L	/* /*
MT5C2568	DCJ	-20	L	/* /*
MT5C2568	DCJ	-25	L	/* /*
MT5C2568	DCJ	-35	L	/* /*
MT5C2568	DCJ	-45	L	/* /*
MT5C2568	DCJ	-55	L	/* /*
MT5C2568	DCJ	-70	L	/* /*

*AVAILABLE PROCESSES

IT = Industrial Temperature Range -40°C to +85°C
XT = Extended Temperature Range -55°C to +125°C
883C = Full Military Processing -55°C to +125°C

12ns offered in IT only

**DEFINITION OF OPTIONS

2V Data Retention / Low Power L

ASI TO DSCC PART NUMBER CROSS REFERENCE*

ASI Package Designator C & CW

ASI Part #	SMD Part #
MT5C2568C-20/883C	5962-8866207NX
MT5C2568C-25/883C	5962-8866206NX
MT5C2568C-35/883C	5962-8866205NX
MT5C2568C-45/883C	5962-8866204NX
MT5C2568C-55/883C	5962-8866203NX
MT5C2568C-70/883C	5962-8866202NX
MT5C2568CW-20/883C	5962-8866207XX
MT5C2568CW-25/883C	5962-8866206XX
MT5C2568CW-35/883C	5962-8866205XX
MT5C2568CW-45/883C	5962-8866204XX
MT5C2568CW-55/883C	5962-8866203XX
MT5C2568CW-70/883C	5962-8866202XX
MT5C2568CW-100/883C	5962-8866201XX

ASI Package Designator EC & ECW

ASI Part #	SMD Part #
MT5C2568EC-20/883C	5962-8866207UX
MT5C2568EC-25/883C	5962-8866206UX
MT5C2568EC-35/883C	5962-8866205UX
MT5C2568EC-45/883C	5962-8866204UX
MT5C2568EC-55/883C	5962-8866203UX
MT5C2568EC-70/883C	5962-8866202UX
MT5C2568ECW-20/883C	5962-8866207YX
MT5C2568ECW-25/883C	5962-8866206YX
MT5C2568ECW-35/883C	5962-8866205YX
MT5C2568ECW-45/883C	5962-8866204YX
MT5C2568ECW-55/883C	5962-8866203YX
MT5C2568ECW-70/883C	5962-8866202YX
MT5C2568ECW-100/883C	5962-8866201YX

ASI Package Designator F

ASI Part #	SMD Part #
MT5C2568F-20/883C	5962-8866207TX
MT5C2568F-25/883C	5962-8866206TX
MT5C2568F-35/883C	5962-8866205TX
MT5C2568F-45/883C	5962-8866204TX
MT5C2568F-55/883C	5962-8866203TX
MT5C2568F-70/883C	5962-8866202TX
MT5C2568F-100/883C	5962-8866201TX

** ASI part number is for reference only. Orders received referencing the SMD part number will be processed per the SMD.*