CMOS Digital Integrated Circuit Silicon Monolithic

TZ2100 Series

Application Processor Lite *ApP Lite*

Overview

TZ2100 series are application processors utilizing a single 600 MHz ARM® Cortex® -A9 core with a floating point unit (FPU), a 2D graphics, a parallel LCD controller interface, camera input interface and an 1 MB of integrated SRAM. This device is highly integrated, as a main processor for various applications with integrated a USB host or device controller (optional), an Ethernet controller, an extended external buses, and rich interfaces.

The TZ2100 processors are supported a security service with an encryption and decryption capability (optional) to enable construction of a robust secure system. These products are suitable for various applications, in addition, an SRAM and a RTC for back-up mode of power state are incorporated.

The TZ2100 series are family products of ***ApP Lite***.

Applications

This product is leveraged to meet needs of following applications; human machine interface, machine to machine interface, single-board computing and portable data terminal.

Features

- Host CPU
  - ARM Cortex-A9 MP Core (Revision r4p1)
    Up to 600 MHz operation frequency
  - ARMv7-A instruction set architecture
  - Floating point unit (FPU)
  - 32 KB L1 I cache/ D cache
  - 128 KB L2 cache
  - Memory management unit: 128-entry TLB
  - Debug technology:
    CoreSight™ (revision: r2p0-01)
    v7 debug architecture, JTAG debug interface
  - Proprietary low power mode for WFI
- System contoller
  - System management unit (SMU):
    Reset management, clock controller
  - Power management unit (PMU):
    External and internal power management
  - Secure services (optional)
    AES, SHA-1, SHA-256, RSA
    Random number generator (RNG)
  - Interruption controller
- SDRAM controller
  - DDR3 / 3L memory interface (16-bit width)
  - Data rate: 800 Mbps
  - Memory size: up to 512 MB
  - ODT control
- Integrated SRAM
  - 1 MB SRAM
  - 32 KB SRAM for data backup
    Low power dissipation for data retention
- Real time clock (RTC)
  Low power dissipation
  - Clock frequency: 32.768 kHz
  - Clock timer, Calendar
  - Time adjustment, alarm interrupt, Periodic interrupt, BCD format
- DMA controller
  - AXI protocol DMA with DMA330 supported
  - Multiple transfer mode
    Memory to Memory, Memory to Peripheral, and Peripheral to Memory
  - 8 channels thread for DMA transfer and one channel thread for DMA management
- Timer
  - 16 channels of 32-bit down counter
    enable one channel as watch dog timer
- 2D graphics accelerator
  - Toshiba original graphics accelerator
  - Blitting, Rotation, Transforming, Drawing
- YUV to RGB converter
  - Input format: YUV 4:2:0 8bit, YUV 4:2:2 8bit
  - Input resolution: QVGA, VGA, up to 2048×2048
  - Output format: RGBA8888, ARGB8888, RGB565, RGB888

- LCD controller
  - Parallel output: RGB 24 bits
  - Output resolution: up to WVGA
  - Frame rate: up to 60 fps
  - Input format: RGBA8888, ARGB8888, RGB565, ARGB1555
  - Alpha blending: up to five planes
- Camera input:
  - One channel
  - Parallel input: 8-bit Data
  - Frame rate: up to 60 fps
  - Resolution (by 8-pixel): up to 2048 × 2048
  - Input format: YUV 4:2:2 8-bit, RAW8, RGB565, ITU-RBT.656
- Audio interfaces
  - Two channels: 1 channel dedicated for output
1 channel for input and output
  - Format: I2S stereo, LR stereo, PCM monaural
  - Sampling clock: 192 kHz, 96 kHz, 48 kHz, 44.1 kHz, 32 kHz, etc.
- USB2.0 host interface (optional)
  - One port USB 2.0 (EHCI rev 1.0, OHCI)
  - Data transfer rate: 480 Mbps / 12 Mbps / 1.5 Mbps
  - Transmission mode: control, interrupt, bulk, isochronous
- USB2.0 device interface (optional)
  - One port (exclusively used by Host / Device)
  - Data transfer rate: 480 Mbps / 12 Mbps / 1.5 Mbps
  - Transmission mode: control, interrupt, bulk, isochronous
- 10/100 Ethernet MAC
  - One Ethernet MAC channel for 10/100 Mbps
  - IEEE Standard 802.3,2000 Edition
  - Support full duplex/half duplex communication
  - RMII (10/100 Mbps) interface to Ethernet PHY device
  - IEEE802.3x flow control function
  - Support Jumbo Frame (up to 4 KB)
- eMMC / SD Card / SDIO interface
  - Two channels for 4-bit data width.
  - One channel for 8bit-data width.
  - Data transmission rate: 150 MHz (max)
  - Supported standard:
eMMC Ver. 4.5, SD Ver. 3.0, and SDIO Ver. 3.0
DS, HS, SDR12, SDR25, SDR50, SDR104 modes.
  - SD card control terminals
- SPI Flash Memory Controller interface
  - Chip select: 2-bit
  - Data bus width: Single, Dual or Quad mode interface
  - Data transmission rate: up to 50 MHz
  - Memory size: from 64 KB to 128 MB
- SPI interfaces (for master controller and transmission)
  - Seven channels for transmission or two for master controller can be selected.
Data transmission rate: up to 25 MHz
  - One channel for slave controller
Data transmission rate: up to 5 MHz
- External BUS interface
  - Data BUS width: 32 bits, 16 bits and 8 bits
- Coexistence is allowed.
  - Address BUS width: 27 bits
  - Memory capacity: up to 768 MB
  - Chip select: 4-bit
  - Asynchronous read/write, asynchronous page read, synchronous burst read/write.
  - Asynchronous boot devices are supported.
- UART interfaces
  - Four channels. One channel without flow control port.
  - Data transmission rate: up to 1.5 Mbps
  - Flow control ports
Compatible with UART 16550 data format
Support external clock input.
Full duplex transmission mode and DMA transfer mode
- I^2C bus interfaces
  - Four channels
  - Open drain output and Schmidt-trigger input
  - Support fast mode plus (up to 1000 kbps), Fast mode, Standard mode
  - A master (compatible with a multi-master) or a slave is selectable.
- Parallel port input interface
  - One channel
  - Data width: 8-bit
  - Data FIFO: 8-bit × 16-stage
- GPIO interface
  - Up to 128 channels
  - External inputs can be used as interrupt signals.
- AD converter inputs
  - Four input channels
  - 12-bit successive AD converter
  - Sampling rate: up to 1.07 MHz
- PWM outputs
  - Six channels
  - Frequencies and duty ratios can be arbitrarily set.

List of Products

This table shows TZ2100 Series lineups. The following table shows the items which have a difference in specifications.

Product Number	Maximum CPU Operation Frequency (MHz)	Operating Temperature Range Ta (°C)	Internal Voltage Range (V)	Security service availability	USB 2.0 Interface
TZ2100XBG(O,2)	300	-40 to 85	1.00 to 1.20	—	—
TZ2100XBG(O,5)	300	-20 to 80	1.00 to 1.20	—	Host / Device
TZ2102XBG(O,3)	600	-20 to 80	1.06 to 1.21	—	Host
TZ2102XBG(O,6)	600	-40 to 85	1.10 to 1.20	—	Host / Device
TZ2101XBG(O,6)	600	-40 to 85	1.10 to 1.20	Available	Host / Device

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- Reference standard
  - DDR3 SDRAM SPECIFICATION

Conventions in this document

- The numerical values are expressed as follows.
  Hexadecimal number**:** 0xABC
  Decimal number**:** 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary number**:** 0b111 - It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m**:**n].
  Example**:** S[3**:**0] shows four signal names S3, S2, S1, and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example**:** ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example**:** ***[XYZ1]***, ***[XYZ2]***, and ***[XYZ3]*** to ***[XYZn]***
- The bit range of a register is written like as [m**:**n].
  Example**:** Bit[3**:**0] expresses the range of bits 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example**:** ***[ABCD]***.EFG = 0x01 (hexadecimal), ***[XYZn]***.VW = 1 (binary)
- Word and Byte represent the following bit length.
  Byte**:** 8-bit
  Half word**:** 16-bit
  Word**:** 32-bit
  Double word**:** 64-bit
- Properties of each bit in a register are expressed as follows.
  R**:** Read only
  W**:** Write only
  W1C**:** Write 1 Clear - The corresponding bit is cleared (=0) when "1" is written to this bit.
  W1S**:** Write 1 Set - The corresponding bit is set (=1) when "1" is written to this bit.
  R/W**:** Read and Write are possible.
  R/W0C**:** Read/Write 0 Clear
  R/W1C**:** Read/Write 1 Clear
  R/W1S**:** Read/Write 1 Set
  RS/WC**:** Read Set/Write Clear - Set after read operation, cleared after write operation.
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, don't use the read value.
- The value read from the bit having default value of "—" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value. In the cases that default is "—", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "—", follow the definition of each register.

1. Features

1.1. CPU

(1) Host CPU
ARM Cortex-A9 MP Core (Revision r4p1)

Instruction set architecture:	ARMv7-A architecture
Operation frequency:	600 MHz (Note 1) / 300 MHz / 150 MHz / 75 MHz etc., selectable
Level-1 instruction cache:	32 KB (4-way set associative)
Lvevl-1 date cache:	32 KB (4-way set associative)
Level-2 cache:	128 KB (8-way set associative)
Data engine:	Floating point unit (FPU) Support single and double precision data processing
Internal bus:	64-bit AXI master interface
Debug technology:	ARM® CoreSight™ (revision: r2p0-01) v7 debug architecture, JTAG debug interface
Memory management unit:	128-entry TLB
Pipe line:	Super scalar, out of order

Proprietary low power mode to minimize power consumption in Wait for Interruption command

Note 1: TZ2101XBG, TZ2102XBG only

1.2. System controller

(1) System management unit (SMU)
Reset management, clock controller

(2) Power management unit (PMU)
External and internal power management

(3) Secure services (optional)
AES, SHA-1, SHA-256, RSA,
Random number generator (RNG)

(4) Interruption controller
Output interrupt requests to the host CPU

1.3. SDRAM controller

(1) SDRAM controller
DDR3 / 3L memory interface

Bus width:	16-bit
Data rate:	800 Mbps
Memory size:	up to 512 MB

Support self-Refresh mode
ODT controller

1.4. Integrated Memory

(1) Internal SRAM
1 MB SRAM is contained for data and programming.

(2) SRAM for data backup
32 KB SRAM for data backup.
Low power dissipation for data retention in a separated power domain

1.5. Real time clock (RTC)

(1) Real time clock (RTC)
Frequency of oscillation: 32.768 kHz
Clock display (hour, minute, second), am-pm / 24-hour
Calendar (month, week, date, and leap year)
Time adjustment, alarm interrupt, Periodic interrupt, BCD format
Low power dissipation in a separated power domain

1.6. Peripheral functions

(1) DMA controller
Multiple transfer mode (Memory to Memory, Memory to Peripheral, Peripheral to Memory)
Original instruction set enables programmable DMA transfer.
Eight channel threads for DMA transfer and one channel thread for DMA management

(2) Timer
16 channels of 32-bit down counter.
One counter can be selected as a watchdog timer (WDT).

1.7. Graphics Accelerator, YUV Conversion and LCD Controller

(1) 2D graphics accelerator
Toshiba original graphics accelerator
Blitting engine (Alpha blending), Transforming engine, Rotation engine (Rotation, Scaling, Transparent), Drawing engine (Anti-Aliasing)
Output format: RGBA8888, ARGB8888, RGB565, ARGB1555

(2) YUV converter
YUV to RGB conversion
Input resolution: QVGA, VGA, 2048 × 2048 (max)
Input format: YUV_4:2:0 8-bit, YUV_4:2:2 8-bit
Output format: RGBA8888, ARGB8888, RGB565, RGB888

(3) LCD controller
Parallel output: 24-bit (RGB), Vsync, Hsync, Clock, Valid
Output resolution: WVGA (800 × 480) (max)
Frame rate: up to 60 fps
Input format: RGBA8888, ARGB8888, RGB565, ARGB1555
Alpha blending: up to Five planes

1.8. Camera Input

(1) 8-bit Parallel

Parallel input:	8-bit Data, Vsync, Hsync/ Enable, Clock
Frame rate:	up to 60 fps
Resolution:	up to 2048 × 2048 (by 8-pixel)
Input format:	YUV 4:2:2 8-bit, RAW8, RGB565, ITU-RBT.656

1.9. Audio interfaces

(1) Audio Interfaces

Two channels:	One channel dedicated for output, and the other one for output and input. Selectable master or slave
Audio format:	I2S stereo, LR stereo, PCM monaural
Sampling frequency:	192 kHz, 96 kHz, 48 kHz, 44.1 kHz, 32 kHz, 24 kHz

1.10. High-speed interface Controller

(1) USB2.0 host interface (optional)

USB2.0 host:	1 port Complaint with USB2.0 (EHCI rev 1.0, OHCI supported)
Data transmission rate:	480 Mbps, 12 Mbps or 1.5 Mbps
Transmission mode:	control, interrupt, bulk, isochronous

(2) USB2.0 device interface (optional)

USB2.0 device:	1 port (exclusive use for Host / Device)
Data transmission rate:	480 Mbps, 12 Mbps or 1.5 Mbps
Transmission mode:	control, interrupt, bulk, isochronous

(3) 10/100 Ethernet MAC Interface

One MAC channel for 10/100 Mbps transmission speed
Complaint with IEEE Standard 802.3,2000 Edition
Support full duplex/half duplex communication
RMII (10/100 Mbps) interface to Ethernet PHY device
IEEE802.3x flow control
Jumbo Frame supported (up to 4 KB)
Upper level protocol function supported (automatic checksum calculation for receiving data)
Dedicated controller for PHY device register access
Interruption synchronizing mode

1.11. Peripheral Interfaces

(1) External Bus Interface

Chip select:	4 bits
Data width:	32-bit / 16-bit / 8-bit (these widths can coexist)
Address width:	27 bits
Corresponding Memory size:	up to 768 MB
Transfer system:	Asynchronous read/write Asynchronous page read Synchronous burst read/write
Boot device support:	Chip enable 0 enables use of a 32-/16-bit device as an asynchronous boot device.

(2) eMMC / SD Card / SDIO Interface

Three channels:	The data width of one channel is 8 bits and two channels are 4 bits.
Data transmission rate:	150 MHz (max)
Boot device support:	One channel of eMMC and one channel of a SD card can be used as boot devices.
Transmission mode:	DS/HS/SDR12/SDR25/SDR50/SDR104 for SD card/SDIO Backward-compatibility/High-Speed/HS200 for eMMC
SD card control pins:	card detection, write protection, power, 3.3 V / 1.8 V voltage switch
Supported standard:	eMMC Ver. 4.5, SD Ver 3.0, and SDIO Ver 3.0.

(3) SPI Flash memory controller interface

Chip select:	2-bit
Boot device support	
Data bus width:	Single, Dual or Quad mode
Data transmission rate:	50 MHz (max)
Memory size:	from 64 KB to 128 MB
Support four bytes addressing mode	

(4) SPI interfaces (for master controller and transmission)

Two channels can be selected for the master controller. Up to seven channels for transmission can be selected.

BUS width:	Single mode interface
Data transmission rate:	25 MHz as the maximum frequency, and 1/1 to 1/32767 prescaler is available.
Data FIFO:	16-bit × 16-stage

(5) SPI interface (for slave controller)

One channel	
Bit width:	Single mode interface
Data transmission rate:	up to 5 MHz
Data FIFO:	16-bit × 16 stage

(6) UART interfaces

Four channels

Data transmission rate: up to 1.5 Mbps

Three channels with flow control port

- Auto flow control (CTS/RTS)
- Complaint with UART 16550 data format
- Support external clock input
- Support full duplex communication, DMA transmission mode

One channel without flow control port (e.g. debug terminal)

(7) I^2C bus interfaces
Four channels
Open drain output and Schmidt-trigger input

Data transmission rate:	Standard mode:	up to 100 kbps,
	Fast mode:	up to 400 kbps
	Fast mode plus:	up to 1000 kbps
Operation mode:	Master (support multi-master) or Slave	

(8) Parallel port input interface
Operate as a target and receives write data from an external host.

Data width:	8-bit
FIFO:	8-bit × 16-stage

Support the active polarity of a strobe signal.

(9) GPIO interfaces
128 channels
124 channels are shared with other functions (Open drain output at six channels).
Four channels are dedicated pins. The I/O power supply is VDD3V3_PA (described in Section 3.3.18).
Input or output direction configurable
External inputs can be used as interrupt signals.
Configurable to set pull-up or pull-down resister

(10) AD converter
Four channels
12-bit successive conversion

Sampling frequency:	1.07 MHz (max) when using one channel
	379 kHz (max) when using four channels

(11) PWM output
Six channels
Configurable frequency and duty of pluses and synchronous output mode is supported.
Configurable pulse generator

2. Block Diagram

Figure 2.1 shows a block diagram of the TZ2100 Series.

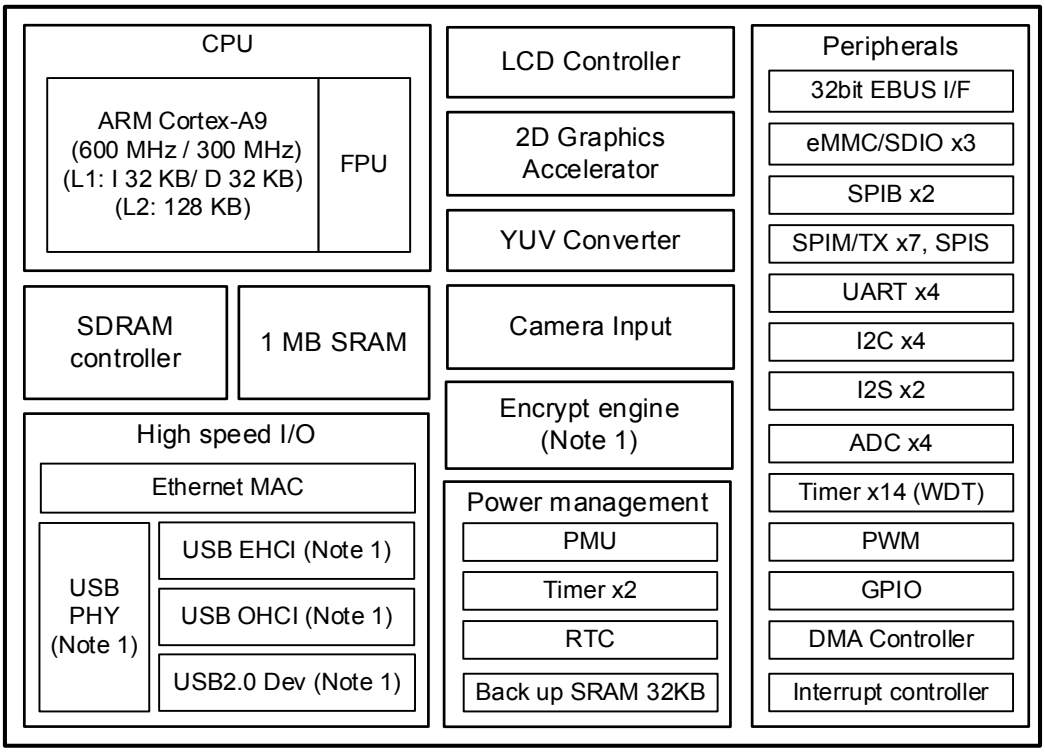


Figure 2.1 Block diagram

Note 1: There are optional functions as follows:
USB2.0 device, USB2.0 host, security service functions.

3. Pin Information

3.1. Pin Alignment

Figure 3.1 shows a pin alignment of this product.

TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	VSS	EMMC0_DAT0	EMMC0_DAT4	EB0_CE3_N	EB0_CLKO	EB0_ADD2	EB0_ADD11	EB0_ADD14	EB0_ADD19	EB0_ADD24	EB0_DAT1	EB0_DAT5	EB0_DAT9	EB0_DAT10	EB0_DAT11	EB0_DAT13	EB0_DAT14	EB0_DAT15	VSS
B	EMMC0_CLK	EMMC0_DAT1	EMMC0_DAT5	EB0_CE2_N	EB0_OE_N	EB0_ADD3	EB0_ADD9	EB0_ADD13	EB0_ADD18	EB0_ADD23	EB0_DAT0	EB0_DAT4	EB0_DAT8	EB0_DAT12	EB0_DAT16	EB0_DAT18	EB0_DAT19	EB0_DAT20	EB0_DAT22
C	EMMC0_CLKB	EMMC0_DAT2	EMMC0_DAT6	EB0_CE1_N		EB0_ADD4	EB0_ADD8		EB0_ADD17	EB0_ADD22	EB0_AVD_N		EB0_DAT6	EB0_DAT17	EB0_DAT23	EB0_DAT24	EB0_DAT25	EB0_DAT26	EB0_DAT27
D	EMMC0_CMD	EMMC0_DAT3	EMMC0_DAT7	EB0_CE0_N	EB0_ADD1	EB0_ADD6	EB0_ADD7	EB0_ADD12	EB0_ADD16	EB0_ADD21	EB0_ADD26	EB0_DAT3	EB0_DAT7	EB0_DAT21	EB0_DAT28	EB0_DAT30	EB0_DAT29	EB0_DAT31	EB0_WE_N
E	SD0_DAT3	SD0_DAT2	SD0_DAT1	EB0_CLKI	EB0_ADD0	EB0_ADD5	EB0_ADD10	EB0_ADD15	EB0_ADD20		EB0_ADD25	EB0_DAT2			EB0_BE2_N	EB0_BE0_N		EB0_BE1_N	EB0_BE3_N
F	SD0_DAT0	SD0_CMD	SD0_CLKB	SD0_CLK	GPIO0_15										GPIO1_1	GPIO1_0	EB0_WAIT_N	XIN_32K	XOUT_32K
G	GPIO0_16	GPIO0_17	GPIO0_19	GPIO0_20	GPIO0_18		VDD1V8_3V3_EMMC	VDD1V8_3V3_EMMC	VDD1V8_3V3_SD1	VDD1V8_3V3_SD1	VDD3V3_PL_EBUS	VDD3V3_PL_EBUS	VDD3V3_PB		BAK_ISOEN_N	DBG_TRST_N	DBG_TMS	DBG_TDI	DBG_TDO
H	GPIO0_21	GPIO0_22		GPIO0_24	GPIO0_23		VDD1V8_3V3_SD0	VSS	VDDC_PA	VSS	VDDC_PA	VSS	VDD3V3_PB		DBG_TCK	LOWPWR		SYS_WAKEUP	WDT_RSTOUT_N
J	GPIO0_25	GPIO0_26	GPIO0_27	GPIO0_29	GPIO0_28		VDD1V8_3V3_SD0	VDDC_PA	VSS	VSS	VSS	VDDC_PA	VDD3V3_PA		SYS_RESET_N	DBG_SRST_N	VSS	GPIO0_2	GPIO0_1
K	GPIO0_30	GPIO0_31	SPIB0_CLK	SPIB0_IO1	SPIB0_IO0		VDD3V3_PL_I2C	VSS	VSS	VSS	VSS	VSS	VDD3V3_PA		GPIO0_3	GPIO0_0	POR_OUT_N	XIN	XOUT
L	SPIB0_IO2	SPIB0_IO3		SPIB0_CS0_N	SPIB0_CS1_N		VDD3V3_PL_I2C	VDDC_PA	VSS	VSS	VSS	VDDC_PA	VDDPLL1			PD_BGR33	PD_POR33	VDD3V3_USB	VDD3V3_USB
M	BOOTSEL0	BOOTSEL1	BOOTSEL2	BOOTSEL3	BOOTSEL4		VDDC_PA	VSS	VDDC_PA	VSS	VDDC_PA	VSS	VDDPLL0		USB0_REXT	USB0_CLK	USB0_VBUS	USB0_DM	USB0_DP
N	BOOTSEL5	UA0_RXD	UA0_TXD	GPIO0_10	GPIO0_11		VSS	VDDC_PA	VDD1V1_DDR	VDD1V1_DDR	VSS	VDDC_PA	VDDPLL2			VSSUSB	USB0_TEST	VSSUSB	VSSUSB
P	GPIO0_13	GPIO0_14		I2C0_SDA	GPIO0_12		DDR0_VREF	VSS	VDD_DDRIO	VDD_DDRIO	DDR0_ZQ	VPGM	VDD1V1_DDRPLL			VDD3V3_ADC	VSSADC	SAD0_DIN2	SAD0_DIN3
R	I2C0_SCL	GPIO0_4	GPIO0_5	GPIO0_6	GPIO0_7											VDD3V3_ADC	VSSADC	SAD0_DIN0	SAD0_DIN1
T	GPIO0_8	GPIO0_9	VSS	DDR0_DQ12		DDR0_DQ10	DDR0_DQ8	DDR0_DQ0	DDR0_DQ6	DDR0_RAS_N	DDR0_WE_N	DDR0_BA2	DDR0_CA0		VSS	VSS	VSS	VSS	VSS
U	DDR0_DQ11	VSS	DDR0_DM1	VSS	DDR0_DQ14	VSS	DDR0_DM0	DDR0_DQ2	DDR0_DQ4	DDR0_CAS_N	DDR0_ODT	DDR0_BA0	DDR0_CA3	DDR0_CA2	DDR0_CA9	DDR0_CA13	VSS	DDR0_CK_P	VSS
V	DDR0_DQ13	DDR0_DQ15	VSS	DDR0_DQS_N1	VSS	DDR0_DQS_P0	VSS	DDR0_DQ3	DDR0_DQ5	DDR0_CS_N	DDR0_CA15	DDR0_CA8	DDR0_RESET_N	DDR0_CA5	DDR0_CA7	DDR0_BA1	VSS	DDR0_CK_N	VSS
W	VSS	DDR0_DQ9	VSS	DDR0_DQS_P1	VSS	DDR0_DQS_N0	VSS	DDR0_DQ1	DDR0_DQ7	DDR0_CKE	DDR0_CA10	DDR0_CA6	DDR0_CA11	DDR0_CA14	DDR0_CA4	DDR0_CA1	DDR0_CA12	VSS	VSS

Figure 3.1 Pin alignment of this product

3.2. Pin List (Ball number order)

Table 3.1 shows pin lists.

Table 3.1 Pin List (Ball number order) 1/4

Ball Number	Pin name	Power supply of pin	Ball Number	Pin Name	Power supply of pin
A1	VSS	—	C6	EB0_ADD4	VDD3V3_PL_EBUS
A2	EMMC0_DAT0	VDD1V8_3V3_EMMC	C7	EB0_ADD8	VDD3V3_PL_EBUS
A3	EMMC0_DAT4	VDD1V8_3V3_EMMC	C9	EB0_ADD17	VDD3V3_PL_EBUS
A4	EB0_CE3_N	VDD1V8_3V3_SD1	C10	EB0_ADD22	VDD3V3_PL_EBUS
A5	EB0_CLKO	VDD1V8_3V3_SD1	C11	EB0_AVD_N	VDD3V3_PL_EBUS
A6	EB0_ADD2	VDD3V3_PL_EBUS	C13	EB0_DAT6	VDD3V3_PL_EBUS
A7	EB0_ADD11	VDD3V3_PL_EBUS	C14	EB0_DAT17	VDD3V3_PL_EBUS
A8	EB0_ADD14	VDD3V3_PL_EBUS	C15	EB0_DAT23	VDD3V3_PL_EBUS
A9	EB0_ADD19	VDD3V3_PL_EBUS	C16	EB0_DAT24	VDD3V3_PL_EBUS
A10	EB0_ADD24	VDD3V3_PL_EBUS	C17	EB0_DAT25	VDD3V3_PL_EBUS
A11	EB0_DAT1	VDD3V3_PL_EBUS	C18	EB0_DAT26	VDD3V3_PL_EBUS
A12	EB0_DAT5	VDD3V3_PL_EBUS	C19	EB0_DAT27	VDD3V3_PL_EBUS
A13	EB0_DAT9	VDD3V3_PL_EBUS	D1	EMMC0_CMD	VDD1V8_3V3_EMMC
A14	EB0_DAT10	VDD3V3_PL_EBUS	D2	EMMC0_DAT3	VDD1V8_3V3_EMMC
A15	EB0_DAT11	VDD3V3_PL_EBUS	D3	EMMC0_DAT7	VDD1V8_3V3_EMMC
A16	EB0_DAT13	VDD3V3_PL_EBUS	D4	EB0_CE0_N	VDD1V8_3V3_SD1
A17	EB0_DAT14	VDD3V3_PL_EBUS	D5	EB0_ADD1	VDD3V3_PL_EBUS
A18	EB0_DAT15	VDD3V3_PL_EBUS	D6	EB0_ADD6	VDD3V3_PL_EBUS
A19	VSS	—	D7	EB0_ADD7	VDD3V3_PL_EBUS
B1	EMMC0_CLK	VDD1V8_3V3_EMMC	D8	EB0_ADD12	VDD3V3_PL_EBUS
B2	EMMC0_DAT1	VDD1V8_3V3_EMMC	D9	EB0_ADD16	VDD3V3_PL_EBUS
B3	EMMC0_DAT5	VDD1V8_3V3_EMMC	D10	EB0_ADD21	VDD3V3_PL_EBUS
B4	EB0_CE2_N	VDD1V8_3V3_SD1	D11	EB0_ADD26	VDD3V3_PL_EBUS
B5	EB0_OE_N	VDD1V8_3V3_SD1	D12	EB0_DAT3	VDD3V3_PL_EBUS
B6	EB0_ADD3	VDD3V3_PL_EBUS	D13	EB0_DAT7	VDD3V3_PL_EBUS
B7	EB0_ADD9	VDD3V3_PL_EBUS	D14	EB0_DAT21	VDD3V3_PL_EBUS
B8	EB0_ADD13	VDD3V3_PL_EBUS	D15	EB0_DAT28	VDD3V3_PL_EBUS
B9	EB0_ADD18	VDD3V3_PL_EBUS	D16	EB0_DAT30	VDD3V3_PL_EBUS
B10	EB0_ADD23	VDD3V3_PL_EBUS	D17	EB0_DAT29	VDD3V3_PL_EBUS
B11	EB0_DAT0	VDD3V3_PL_EBUS	D18	EB0_DAT31	VDD3V3_PL_EBUS
B12	EB0_DAT4	VDD3V3_PL_EBUS	D19	EB0_WE_N	VDD3V3_PL_EBUS
B13	EB0_DAT8	VDD3V3_PL_EBUS	E1	SD0_DAT3	VDD1V8_3V3_SD0
B14	EB0_DAT12	VDD3V3_PL_EBUS	E2	SD0_DAT2	VDD1V8_3V3_SD0
B15	EB0_DAT16	VDD3V3_PL_EBUS	E3	SD0_DAT1	VDD1V8_3V3_SD0
B16	EB0_DAT18	VDD3V3_PL_EBUS	E4	EB0_CLKI	VDD1V8_3V3_SD1
B17	EB0_DAT19	VDD3V3_PL_EBUS	E5	EB0_ADD0	VDD3V3_PL_EBUS
B18	EB0_DAT20	VDD3V3_PL_EBUS	E6	EB0_ADD5	VDD3V3_PL_EBUS
B19	EB0_DAT22	VDD3V3_PL_EBUS	E7	EB0_ADD10	VDD3V3_PL_EBUS
C1	EMMC0_CLKB	VDD1V8_3V3_EMMC	E8	EB0_ADD15	VDD3V3_PL_EBUS
C2	EMMC0_DAT2	VDD1V8_3V3_EMMC	E9	EB0_ADD20	VDD3V3_PL_EBUS
C3	EMMC0_DAT6	VDD1V8_3V3_EMMC	E11	EB0_ADD25	VDD3V3_PL_EBUS
C4	EB0_CE1_N	VDD1V8_3V3_SD1	E12	EB0_DAT2	VDD3V3_PL_EBUS

Table 3.1 Pin List (Ball number order) 2/4

Ball Number	Pin Name	Power supply of pin	Ball Number	Pin Name	Power supply of pin
E15	EB0_BE2_N	VDD3V3_PL_EBUS	H15	DBG_TCK	VDD3V3_PA
E16	EB0_BE0_N	VDD3V3_PL_EBUS	H16	LOWPWR	VDD3V3_PA
E18	EB0_BE1_N	VDD3V3_PL_EBUS	H18	SYS_WAKEUP	VDD3V3_PA
E19	EB0_BE3_N	VDD3V3_PL_EBUS	H19	WDT_RSTOUT_N	VDD3V3_PA
F1	SD0_DAT0	VDD1V8_3V3_SD0	J1	GPIO0_25	VDD3V3_PL_I2C
F2	SD0_CMD	VDD1V8_3V3_SD0	J2	GPIO0_26	VDD3V3_PL_I2C
F3	SD0_CLKB	VDD1V8_3V3_SD0	J3	GPIO0_27	VDD3V3_PL_I2C
F4	SD0_CLK	VDD1V8_3V3_SD0	J4	GPIO0_29	VDD3V3_PL_I2C
F5	GPIO0_15	VDD3V3_PL_I2C	J5	GPIO0_28	VDD3V3_PL_I2C
F15	GPIO1_1	VDD3V3_PL_EBUS	J7	VDD1V8_3V3_SD0	—
F16	GPIO1_0	VDD3V3_PL_EBUS	J8	VDDC_PA	—
F17	EB0_WAIT_N	VDD3V3_PL_EBUS	J9	VSS	—
F18	XIN_32K	VDD3V3_PB	J10	VSS	—
F19	XOUT_32K	VDD3V3_PB	J11	VSS	—
G1	GPIO0_16	VDD3V3_PL_I2C	J12	VDDC_PA	—
G2	GPIO0_17	VDD3V3_PL_I2C	J13	VDD3V3_PA	—
G3	GPIO0_19	VDD3V3_PL_I2C	J15	SYS_RESET_N	VDD3V3_PA
G4	GPIO0_20	VDD3V3_PL_I2C	J16	DBG_SRST_N	VDD3V3_PA
G5	GPIO0_18	VDD3V3_PL_I2C	J17	VSS	—
G7	VDD1V8_3V3_EMMC	—	J18	GPIO0_2	VDD3V3_PA
G8	VDD1V8_3V3_EMMC	—	J19	GPIO0_1	VDD3V3_PA
G9	VDD1V8_3V3_SD1	—	K1	GPIO0_30	VDD3V3_PL_I2C
G10	VDD1V8_3V3_SD1	—	K2	GPIO0_31	VDD3V3_PL_I2C
G11	VDD3V3_PL_EBUS	—	K3	SPIB0_CLK	VDD3V3_PL_I2C
G12	VDD3V3_PL_EBUS	—	K4	SPIB0_IO1	VDD3V3_PL_I2C
G13	VDD3V3_PB	—	K5	SPIB0_IO0	VDD3V3_PL_I2C
G15	BAK_ISOEN_N	VDD3V3_PB	K7	VDD3V3_PL_I2C	—
G16	DBG_TRST_N	VDD3V3_PA	K8	VSS	—
G17	DBG_TMS	VDD3V3_PA	K9	VSS	—
G18	DBG_TDI	VDD3V3_PA	K10	VSS	—
G19	DBG_TDO	VDD3V3_PA	K11	VSS	—
H1	GPIO0_21	VDD3V3_PL_I2C	K12	VSS	—
H2	GPIO0_22	VDD3V3_PL_I2C	K13	VDD3V3_PA	—
H4	GPIO0_24	VDD3V3_PL_I2C	K15	GPIO0_3	VDD3V3_PA
H5	GPIO0_23	VDD3V3_PL_I2C	K16	GPIO0_0	VDD3V3_PA
H7	VDD1V8_3V3_SD0	—	K17	POR_OUT_N	VDD3V3_PA
H8	VSS	—	K18	XIN	VDD3V3_PA
H9	VDDC_PA	—	K19	XOUT	VDD3V3_PA
H10	VSS	—	L1	SPIB0_IO2	VDD3V3_PL_I2C
H11	VDDC_PA	—	L2	SPIB0_IO3	VDD3V3_PL_I2C
H12	VSS	—	L4	SPIB0_CS0_N	VDD3V3_PL_I2C
H13	VDD3V3_PB	—	L5	SPIB0_CS1_N	VDD3V3_PL_I2C

Table 3.1 Pin List (Ball number order) 3/4

Ball Number	Pin Name	Power supply of pin	Ball Number	Pin Name	Power supply of pin
L7	VDD3V3_PL_I2C	—	N18	VSSUSB	—
L8	VDDC_PA	—	N19	VSSUSB	—
L9	VSS	—	P1	GPIO0_13	VDD3V3_PL_I2C
L10	VSS	—	P2	GPIO0_14	VDD3V3_PL_I2C
L11	VSS	—	P4	I2C0_SDA	VDD3V3_PL_I2C
L12	VDDC_PA	—	P5	GPIO0_12	VDD3V3_PL_I2C
L13	VDDPLL1	—	P7	DDR0_VREF	VDD_DDRIO
L16	PD_BGR33	—	P8	VSS	—
L17	PD_POR33	—	P9	VDD_DDRIO	—
L18	VDD3V3_USB	—	P10	VDD_DDRIO	—
L19	VDD3V3_USB	—	P11	DDR0_ZQ	VDD_DDRIO
M1	BOOTSEL0	VDD3V3_PL_I2C	P12	VPGM	—
M2	BOOTSEL1	VDD3V3_PL_I2C	P13	VDD1V1_DDRPLL	—
M3	BOOTSEL2	VDD3V3_PL_I2C	P16	VDD3V3_ADC	—
M4	BOOTSEL3	VDD3V3_PL_I2C	P17	VSSADC	—
M5	BOOTSEL4	VDD3V3_PL_I2C	P18	SAD0_DIN2	VDD3V3_ADC
M7	VDDC_PA	—	P19	SAD0_DIN3	VDD3V3_ADC
M8	VSS	—	R1	I2C0_SCL	VDD3V3_PL_I2C
M9	VDDC_PA	—	R2	GPIO0_4	VDD3V3_PL_I2C
M10	VSS	—	R3	GPIO0_5	VDD3V3_PL_I2C
M11	VDDC_PA	—	R4	GPIO0_6	VDD3V3_PL_I2C
M12	VSS	—	R5	GPIO0_7	VDD3V3_PL_I2C
M13	VDDPLL0	—	R16	VDD3V3_ADC	—
M15	USB0_REXT	VDD3V3_USB	R17	VSSADC	—
M16	USB0_CLK	VDD3V3_USB	R18	SAD0_DIN0	VDD3V3_ADC
M17	USB0_VBUS	VDD3V3_USB	R19	SAD0_DIN1	VDD3V3_ADC
M18	USB0_DM	VDD3V3_USB	T1	GPIO0_8	VDD3V3_PL_I2C
M19	USB0_DP	VDD3V3_USB	T2	GPIO0_9	VDD3V3_PL_I2C
N1	BOOTSEL5	VDD3V3_PL_I2C	T3	VSS	—
N2	UA0_RXD	VDD3V3_PL_I2C	T4	DDR0_DQ12	VDD_DDRIO
N3	UA0_TXD	VDD3V3_PL_I2C	T6	DDR0_DQ10	VDD_DDRIO
N4	GPIO0_10	VDD3V3_PL_I2C	T7	DDR0_DQ8	VDD_DDRIO
N5	GPIO0_11	VDD3V3_PL_I2C	T8	DDR0_DQ0	VDD_DDRIO
N7	VSS	—	T9	DDR0_DQ6	VDD_DDRIO
N8	VDDC_PA	—	T10	DDR0_RAS_N	VDD_DDRIO
N9	VDD1V1_DDR	—	T11	DDR0_WE_N	VDD_DDRIO
N10	VDD1V1_DDR	—	T12	DDR0_BA2	VDD_DDRIO
N11	VSS	—	T13	DDR0_CA0	VDD_DDRIO
N12	VDDC_PA	—	T15	VSS	—
N13	VDDPLL2	—	T16	VSS	—
N16	VSSUSB	—	T17	VSS	—
N17	USB0_TEST	VDD3V3_USB	T18	VSS	—

Table 3.1 Pin List (Ball number order) 4/4

Ball Number	Pin Name	Power supply of pin	Ball Number	Pin Name	Power supply of pin
T19	VSS	—	V10	DDR0_CS_N	VDD_DDRIO
U1	DDR0_DQ11	VDD_DDRIO	V11	DDR0_CA15	VDD_DDRIO
U2	VSS	—	V12	DDR0_CA8	VDD_DDRIO
U3	DDR0_DM1	VDD_DDRIO	V13	DDR0_RESET_N	VDD_DDRIO
U4	VSS	—	V14	DDR0_CA5	VDD_DDRIO
U5	DDR0_DQ14	VDD_DDRIO	V15	DDR0_CA7	VDD_DDRIO
U6	VSS	—	V16	DDR0_BA1	VDD_DDRIO
U7	DDR0_DM0	VDD_DDRIO	V17	VSS	—
U8	DDR0_DQ2	VDD_DDRIO	V18	DDR0_CK_N	VDD_DDRIO
U9	DDR0_DQ4	VDD_DDRIO	V19	VSS	—
U10	DDR0_CAS_N	VDD_DDRIO	W1	VSS	—
U11	DDR0_ODT	VDD_DDRIO	W2	DDR0_DQ9	VDD_DDRIO
U12	DDR0_BA0	VDD_DDRIO	W3	VSS	—
U13	DDR0_CA3	VDD_DDRIO	W4	DDR0_DQS_P1	VDD_DDRIO
U14	DDR0_CA2	VDD_DDRIO	W5	VSS	—
U15	DDR0_CA9	VDD_DDRIO	W6	DDR0_DQS_N0	VDD_DDRIO
U16	DDR0_CA13	VDD_DDRIO	W7	VSS	—
U17	VSS	—	W8	DDR0_DQ1	VDD_DDRIO
U18	DDR0_CK_P	VDD_DDRIO	W9	DDR0_DQ7	VDD_DDRIO
U19	VSS	—	W10	DDR0_CKE	VDD_DDRIO
V1	DDR0_DQ13	VDD_DDRIO	W11	DDR0_CA10	VDD_DDRIO
V2	DDR0_DQ15	VDD_DDRIO	W12	DDR0_CA6	VDD_DDRIO
V3	VSS	—	W13	DDR0_CA11	VDD_DDRIO
V4	DDR0_DQS_N1	VDD_DDRIO	W14	DDR0_CA14	VDD_DDRIO
V5	VSS	—	W15	DDR0_CA4	VDD_DDRIO
V6	DDR0_DQS_P0	VDD_DDRIO	W16	DDR0_CA1	VDD_DDRIO
V7	VSS	—	W17	DDR0_CA12	VDD_DDRIO
V8	DDR0_DQ3	VDD_DDRIO	W18	VSS	—
V9	DDR0_DQ5	VDD_DDRIO	W19	VSS	—

3.3. Signal description (in order of pin function)

Some of pins are assigned multiple functions with this product. To define a function on a pin, setting appropriate pin configuration registers is required after booting up this product. The setting needs to be done with care since some of the configuration bits may affect multiple different pins in one bit at once.

IDX	Signal	In / Out	Description	Pin share
Index by each function	Signal name	IO's direction or attribute	Description of signal	"yes" means that multiple functions are signed to this pin

According to the above table, tables shown in 3.3.1 or afterwards show signal descriptions by function group. The input/output columns may describe "Analog", "Power" and "GND".

3.3.1. Clock Sources and Reset

IDX	Signal name	In / Out	Description
1	XIN	In	Resonator input for the system clock (24 MHz) Oscillator Input for the system clock (24 MHz)
2	XOUT	Out	Resonator output for the system clock (24 MHz)
3	XIN_32K	In	Resonator input for the RTC (32.768 kHz)
4	XOUT_32K	IO	Resonator output for the RTC (32.768 kHz) Oscillator Input for the RTC (32.768 kHz)
5	SYS_RESET_N	In	System reset input
6	POR_OUT_N	Out	Power on reset output
7	WDT_RSTOUT_N	Out	Watch dog timer reset output
8	BAK_ISOEN_N	In	Backup power domain enable input
9	DBG_SRST_N	In	CPU (without debug resource) system reset input
10	SYS_WAKEUP	In	Wake up interrupt input
11	LOWPWR	Out	Low power enable output

3.3.2. DDR3/DDR3L Memory Interface

IDX	Signal name	In / Out	Description
1	DDR0_CK_P	Out	DDR3/DDR3L differential clock output (plus)
2	DDR0_CK_N	Out	DDR3/DDR3L differential clock output (minus)
3	DDR0_CKE	Out	DDR3/DDR3L clock enable
4	DDR0_CA15	Out	DDR3/DDR3L address 15
5	DDR0_CA14	Out	DDR3/DDR3L address 14
6	DDR0_CA13	Out	DDR3/DDR3L address 13
7	DDR0_CA12	Out	DDR3/DDR3L address 12
8	DDR0_CA11	Out	DDR3/DDR3L address 11
9	DDR0_CA10	Out	DDR3/DDR3L address 10
10	DDR0_CA9	Out	DDR3/DDR3L address 9
11	DDR0_CA8	Out	DDR3/DDR3L address 8
12	DDR0_CA7	Out	DDR3/DDR3L address 7
13	DDR0_CA6	Out	DDR3/DDR3L address 6
14	DDR0_CA5	Out	DDR3/DDR3L address 5
15	DDR0_CA4	Out	DDR3/DDR3L address 4
16	DDR0_CA3	Out	DDR3/DDR3L address 3
17	DDR0_CA2	Out	DDR3/DDR3L address 2
18	DDR0_CA1	Out	DDR3/DDR3L address 1

IDX	Signal name	In / Out	Description
19	DDR0_CA0	Out	DDR3/DDR3L address 0
20	DDR0_BA2	Out	DDR3/DDR3L bank address 2
21	DDR0_BA1	Out	DDR3/DDR3L bank address 1
22	DDR0_BA0	Out	DDR3/DDR3L bank address 0
23	DDR0_RAS_N	Out	DDR3/DDR3L row address selection signal
24	DDR0_CAS_N	Out	DDR3/DDR3L column address selection signal
25	DDR0_DQ15	IO	DDR3/DDR3L data bus 15
26	DDR0_DQ14	IO	DDR3/DDR3L data bus 14
27	DDR0_DQ13	IO	DDR3/DDR3L data bus 13
28	DDR0_DQ12	IO	DDR3/DDR3L data bus 12
29	DDR0_DQ11	IO	DDR3/DDR3L data bus 11
30	DDR0_DQ10	IO	DDR3/DDR3L data bus 10
31	DDR0_DQ9	IO	DDR3/DDR3L data bus 9
32	DDR0_DQ8	IO	DDR3/DDR3L data bus 8
33	DDR0_DQ7	IO	DDR3/DDR3L data bus 7
34	DDR0_DQ6	IO	DDR3/DDR3L data bus 6
35	DDR0_DQ5	IO	DDR3/DDR3L data bus 5
36	DDR0_DQ4	IO	DDR3/DDR3L data bus 4
37	DDR0_DQ3	IO	DDR3/DDR3L data bus 3
38	DDR0_DQ2	IO	DDR3/DDR3L data bus 2
39	DDR0_DQ1	IO	DDR3/DDR3L data bus 1
40	DDR0_DQ0	IO	DDR3/DDR3L data bus 0
41	DDR0_DQS_P1	IO	DDR3/DDR3L differential data strobe plus 1
42	DDR0_DQS_P0	IO	DDR3/DDR3L differential data strobe plus 0
43	DDR0_DQS_N1	IO	DDR3/DDR3L differential data strobe minus 1
44	DDR0_DQS_N0	IO	DDR3/DDR3L differential data strobe minus 0
45	DDR0_DM1	IO	DDR3/DDR3L write data byte mask 1
46	DDR0_DM0	IO	DDR3/DDR3L write data byte mask 0
47	DDR0_CS_N	Out	DDR3/DDR3L chip select
48	DDR0_WE_N	Out	DDR3/DDR3L write enable
49	DDR0_VREF	Analog	DDR3/DDR3L DQ reference voltage
50	DDR0_ODT	Out	DDR3/DDR3L ODT enable
51	DDR0_RESET_N	Out	DDR3/DDR3L reset output
52	DDR0_ZQ	Analog	DDR3/DDR3L reference resister input

Connect a bridge terminal resistor (recommended value**:** 220 Ω) between the DDR0_CK_P and the DDR0_CK_N.

3.3.3. SPI Flash Memory Controller Interface

IDX	Signal name	In / Out	Description	Pin share
1	SPIB0_CLK	Out	SPIB0 clock output	yes
2	SPIB0_IO0	IO	SPIB0 serial data output	yes
3	SPIB0_IO1	IO	SPIB0 serial data input	yes
4	SPIB0_IO2	IO	SPIB0 quad data 2	yes
5	SPIB0_IO3	IO	SPIB0 quad data 3	yes
6	SPIB0_CS0_N	Out	SPIB0 chip select 0	yes
7	SPIB0_CS1_N	Out	SPIB0 chip select 1	yes

3.3.4. eMMC / SD card / SDIO Interfaces

IDX	Signal name	In / Out	Description	Pin share
1	SD0_CD	In	SD0 card detection	yes
2	SD0_WP	In	SD0 card write protection	yes
3	SD0_V18EN	Out	SD0 card 1.8 V/3.3 V control	yes
4	SD0_POWER	Out	SD0 card power supply voltage control	yes
5	SD0_CLK	Out	SD0 clock output	yes
6	SD0_CLKB	In	SD0 timing control clock B	yes
7	SD0_CMD	IO	SD0 command	yes
8	SD0_DAT0	IO	SD0 data 0	yes
9	SD0_DAT1	IO	SD0 data 1	yes
10	SD0_DAT2	IO	SD0 data 2	yes
11	SD0_DAT3	IO	SD0 data 3	yes
12	SD1_CD	In	SD1 card detection	yes
13	SD1_WP	In	SD1 card write protection	yes
14	SD1_V18EN	Out	SD1 card 1.8 V/3.3 V control	yes
15	SD1_POWER	Out	SD1 card power supply voltage control	yes
16	SD1_CLK	Out	SD1 clock output	yes
17	SD1_CLKB	In	SD1 timing control clock B	yes
18	SD1_CMD	IO	SD1 command	yes
19	SD1_DAT0	IO	SD1 data 0	yes
20	SD1_DAT1	IO	SD1 data 1	yes
21	SD1_DAT2	IO	SD1 data 2	yes
22	SD1_DAT3	IO	SD1 data 3	yes
23	EMMC0_CLK	Out	eMMC clock output	yes
24	EMMC0_CLKB	In	eMMC timing control clock B	yes
25	EMMC0_CMD	IO	eMMC command	yes
26	EMMC0_DAT0	IO	eMMC data 0	yes
27	EMMC0_DAT1	IO	eMMC data 1	yes
28	EMMC0_DAT2	IO	eMMC data 2	yes
29	EMMC0_DAT3	IO	eMMC data 3	yes
30	EMMC0_DAT4	IO	eMMC data 4	yes
31	EMMC0_DAT5	IO	eMMC data 5	yes
32	EMMC0_DAT6	IO	eMMC data 6	yes
33	EMMC0_DAT7	IO	eMMC data 7	yes

3.3.5. External BUS interface

IDX	Signal name	In / Out	Description	Pin share
1	EB0_ADD26	Out	EBUS address 26	yes
2	EB0_ADD25	Out	EBUS address 25	yes
3	EB0_ADD24	Out	EBUS address 24	yes
4	EB0_ADD23	Out	EBUS address 23	yes
5	EB0_ADD22	Out	EBUS address 22	yes
6	EB0_ADD21	Out	EBUS address 21	yes
7	EB0_ADD20	Out	EBUS address 20	yes
8	EB0_ADD19	Out	EBUS address 19	yes
9	EB0_ADD18	Out	EBUS address 18	yes
10	EB0_ADD17	Out	EBUS address 17	yes
11	EB0_ADD16	Out	EBUS address 16	yes
12	EB0_ADD15	Out	EBUS address 15	yes
13	EB0_ADD14	Out	EBUS address 14	yes
14	EB0_ADD13	Out	EBUS address 13	yes
15	EB0_ADD12	Out	EBUS address 12	yes
16	EB0_ADD11	Out	EBUS address 11	yes
17	EB0_ADD10	Out	EBUS address 10	yes
18	EB0_ADD9	Out	EBUS address 9	yes
19	EB0_ADD8	Out	EBUS address 8	yes
20	EB0_ADD7	Out	EBUS address 7	yes
21	EB0_ADD6	Out	EBUS address 6	yes
22	EB0_ADD5	Out	EBUS address 5	yes
23	EB0_ADD4	Out	EBUS address 4	yes
24	EB0_ADD3	Out	EBUS address 3	yes
25	EB0_ADD2	Out	EBUS address 2	yes
26	EB0_ADD1	Out	EBUS address 1	yes
27	EB0_ADD0	Out	EBUS address 0	yes
28	EB0_DAT31	IO	EBUS data 31	yes
29	EB0_DAT30	IO	EBUS data 30	yes
30	EB0_DAT29	IO	EBUS data 29	yes
31	EB0_DAT28	IO	EBUS data 28	yes
32	EB0_DAT27	IO	EBUS data 27	yes
33	EB0_DAT26	IO	EBUS data 26	yes
34	EB0_DAT25	IO	EBUS data 25	yes
35	EB0_DAT24	IO	EBUS data 24	yes
36	EB0_DAT23	IO	EBUS data 23	yes
37	EB0_DAT22	IO	EBUS data 22	yes
38	EB0_DAT21	IO	EBUS data 21	yes
39	EB0_DAT20	IO	EBUS data 20	yes
40	EB0_DAT19	IO	EBUS data 19	yes
41	EB0_DAT18	IO	EBUS data 18	yes
42	EB0_DAT17	IO	EBUS data 17	yes
43	EB0_DAT16	IO	EBUS data 16	yes
44	EB0_DAT15	IO	EBUS data 15	yes
45	EB0_DAT14	IO	EBUS data 14	yes
46	EB0_DAT13	IO	EBUS data 13	yes
47	EB0_DAT12	IO	EBUS data 12	yes
48	EB0_DAT11	IO	EBUS data 11	yes
49	EB0_DAT10	IO	EBUS data 10	yes
50	EB0_DAT9	IO	EBUS data 9	yes

IDX	Signal name	In / Out	Description	Pin share
51	EB0_DAT8	IO	EBUS data 8	yes
52	EB0_DAT7	IO	EBUS data 7	yes
53	EB0_DAT6	IO	EBUS data 6	yes
54	EB0_DAT5	IO	EBUS data 5	yes
55	EB0_DAT4	IO	EBUS data 4	yes
56	EB0_DAT3	IO	EBUS data 3	yes
57	EB0_DAT2	IO	EBUS data 2	yes
58	EB0_DAT1	IO	EBUS data 1	yes
59	EB0_DAT0	IO	EBUS data 0	yes
60	EB0_CE3_N	Out	EBUS chip enable 3	yes
61	EB0_CE2_N	Out	EBUS chip enable 2	yes
62	EB0_CE1_N	Out	EBUS chip enable 1	yes
63	EB0_CE0_N	Out	EBUS chip enable 0	yes
64	EB0_BE3_N	Out	EBUS byte enable [31:24]	yes
65	EB0_BE2_N	Out	EBUS byte enable [23:16]	yes
66	EB0_BE1_N	Out	EBUS byte enable [15:8]	yes
67	EB0_BE0_N	Out	EBUS byte enable [7:0]	yes
68	EB0_AVD_N	Out	EBUS address validity detection output	yes
69	EB0_WE_N	Out	EBUS write enable	yes
70	EB0_OE_N	Out	EBUS output enable	yes
71	EB0_WAIT_N	In	EBUS wait input	yes
72	EB0_CLKI	In	EBUS clock input	yes
73	EB0_CLKO	Out	EBUS clock	yes

3.3.6. UART interface

IDX	Signal name	In / Out	Description	Pin share
1	UA0_RXD	In	UART0 serial data input	—
2	UA0_TXD	Out	UART0 serial data output	—
3	UA1_RXD	In	UART1 serial data input	yes
4	UA1_TXD	Out	UART1 serial data output	yes
5	UA1_CTS_N	In	UART1 CTS input	yes
6	UA1_RTS_N	Out	UART1 RTS output	yes
7	UA1_EXCLK	In	UART1 external clock input	yes
8	UA2_RXD	In	UART2 serial data input	yes
9	UA2_TXD	Out	UART2 serial data output	yes
10	UA2_CTS_N	In	UART2 CTS input	yes
11	UA2_RTS_N	Out	UART2 RTS output	yes
12	UA3_RXD	In	UART3 serial data input	yes
13	UA3_TXD	Out	UART3 serial data output	yes
14	UA3_CTS_N	In	UART3 CTS input	yes
15	UA3_RTS_N	Out	UART3 RTS output	yes

3.3.7. I²C bus interface

IDX	Signal name	In / Out	Description	Pin share
1	I2C0_SDA	IO	I2C0 data	—
2	I2C0_SCL	IO	I2C0 clock	—
3	I2C1_SDA	IO	I2C1 data	yes
4	I2C1_SCL	IO	I2C1 clock	yes
5	I2C2_SDA	IO	I2C2 data	yes
6	I2C2_SCL	IO	I2C2 clock	yes
7	I2C3_SDA	IO	I2C3 data	yes
8	I2C3_SCL	IO	I2C3 clock	yes

Note: Each pin has open drain type interface.

3.3.8. SPI Interfaces (for Master Controller)

IDX	Signal name	In / Out	Description	Pin share
1	SPIM0_CLK	Out	SPIM0 clock output	yes
2	SPIM0_DI	In	SPIM0 serial data input	yes
3	SPIM0_DO	Out	SPIM0 serial data output	yes
4	SPIM0_CS_N	Out	SPIM0 chip select	yes
5	SPIM1_CLK	Out	SPIM1 clock output	yes
6	SPIM1_DI	In	SPIM1 serial data input	yes
7	SPIM1_DO	Out	SPIM1 serial data output	yes
8	SPIM1_CS_N	Out	SPIM1 chip select	yes

Note: The SPIM0 and the SPITX0 can NOT be used at the same time in an application, the SPIM1 and the SPITX1 can NOT be used at the same time, too.

3.3.9. SPI Interfaces (Dedicated for Transmission)

IDX	Signal name	In / Out	Description	Pin share
1	SPITX0_CLK	Out	SPITX0 clock output	yes
2	SPITX0_DO	Out	SPITX0 data output	yes
3	SPITX0_CS_N	Out	SPITX0 chip select	yes
4	SPITX1_CLK	Out	SPITX1 clock output	yes
5	SPITX1_DO	Out	SPITX1 data output	yes
6	SPITX1_CS_N	Out	SPITX1 chip select	yes
7	SPITX2_CLK	Out	SPITX2 clock output	yes
8	SPITX2_DO	Out	SPITX2 data output	yes
9	SPITX2_CS_N	Out	SPITX2 chip select	yes
10	SPITX3_CLK	Out	SPITX3 clock output	yes
11	SPITX3_DO	Out	SPITX3 data output	yes
12	SPITX3_CS_N	Out	SPITX3 chip select	yes
13	SPITX4_CLK	Out	SPITX4 clock output	yes
14	SPITX4_DO	Out	SPITX4 data output	yes
15	SPITX4_CS_N	Out	SPITX4 chip select	yes
16	SPITX5_CLK	Out	SPITX5 clock output	yes
17	SPITX5_DO	Out	SPITX5 data output	yes
18	SPITX5_CS_N	Out	SPITX5 chip select	yes
19	SPITX6_CLK	Out	SPITX6 clock output	yes
20	SPITX6_DO	Out	SPITX6 data output	yes
21	SPITX6_CS_N	Out	SPITX6 chip select	yes

Note: The SPIM0 and the SPITX0 can NOT be used at the same time in an application. The SPIM1 and the SPITX1 can NOT be used at the same time, too.

3.3.10. SPI Interface (for Slave Controller)

IDX	Signal name	In / Out	Description	Pin share
1	SPIS0_CLK	In	SPIS0 clock input	yes
2	SPIS0_DI	In	SPIS0 serial data input	yes
3	SPIS0_DO	Out	SPIS0 serial data output	yes
4	SPIS0_CS_N	In	SPIS0 chip select	yes

Note: Select one of pin combinations J5/J3/K1/J4 or H1/G3/G4/H2 in an application.

3.3.11. USB2.0 Host or Device Interface

IDX	Signal name	In / Out	Description
1	USB0_DP	IO	USB port I/O data (DP)
2	USB0_DM	IO	USB port I/O data (DM)
3	USB0_REXT	Analog	to connect an external resister (Note 1)
4	USB0_VBUS	Analog	VBUS voltage detection (for device mode)
5	USB0_CLK	In	Input to the clock generator for USB (12 MHz) * option for external oscillator connection
6	USB0_TEST	Analog	Test pin

Note 1: Connect to GND with 174 Ω (±1%) resistor.

3.3.12. Ethernet MAC Interface

IDX	Signal name	In / Out	Description	Pin share
1	ETH0_TXD0	Out	Ethernet RMII transmission data 0	yes
2	ETH0_TXD1	Out	Ethernet RMII transmission data 1	yes
3	ETH0_TXEN	Out	Ethernet RMII transmission enable	yes
4	ETH0_RXD0	In	Ethernet RMII receiving data 0	yes
5	ETH0_RXD1	In	Ethernet RMII receiving data 1	yes
6	ETH0_CRSDV	In	Ethernet RMII carrier sense / receiving data valid	yes
7	ETH0_MDC	Out	Ethernet management data clock	yes
8	ETH0_MDIO	IO	Ethernet management data I/O	yes
9	ETH0_REFCLK	In	Ethernet RMII reference clock	yes

3.3.13. Camera Input

IDX	Signal name	In / Out	Description	Pin share
1	CAM0_CLK	In	Input for clock from camera sensor	yes
2	CAM0_VSYNC	In	Input for vertical synch	yes
3	CAM0_HSYNC	In	Input for data enable or horizontal synch	yes
4	CAM0_DATA0	In	Camera Input data 0	yes
5	CAM0_DATA1	In	Camera Input data 1	yes
6	CAM0_DATA2	In	Camera Input data 2	yes
7	CAM0_DATA3	In	Camera Input data 3	yes
8	CAM0_DATA4	In	Camera Input data 4	yes
9	CAM0_DATA5	In	Camera Input data 5	yes
10	CAM0_DATA6	In	Camera Input data 6	yes
11	CAM0_DATA7	In	Camera Input data 7	yes

3.3.14. Display Output

IDX	Signal name	In / Out	Description	Pin share
1	LCD0_RD0	Out	LCD_R_Data0 output	yes
2	LCD0_RD1	Out	LCD_R_Data1 output	yes
3	LCD0_RD2	Out	LCD_R_Data2 output	yes
4	LCD0_RD3	Out	LCD_R_Data3 output	yes
5	LCD0_RD4	Out	LCD_R_Data4 output	yes
6	LCD0_RD5	Out	LCD_R_Data5 output	yes
7	LCD0_RD6	Out	LCD_R_Data6 output	yes
8	LCD0_RD7	Out	LCD_R_Data7 output	yes
9	LCD0_GD0	Out	LCD_G_Data0 output	yes
10	LCD0_GD1	Out	LCD_G_Data1 output	yes
11	LCD0_GD2	Out	LCD_G_Data2 output	yes
12	LCD0_GD3	Out	LCD_G_Data3 output	yes
13	LCD0_GD4	Out	LCD_G_Data4 output	yes
14	LCD0_GD5	Out	LCD_G_Data5 output	yes
15	LCD0_GD6	Out	LCD_G_Data6 output	yes
16	LCD0_GD7	Out	LCD_G_Data7 output	yes
17	LCD0_BD0	Out	LCD_B_Data0 output	yes
18	LCD0_BD1	Out	LCD_B_Data1 output	yes
19	LCD0_BD2	Out	LCD_B_Data2 output	yes
20	LCD0_BD3	Out	LCD_B_Data3 output	yes
21	LCD0_BD4	Out	LCD_B_Data4 output	yes
22	LCD0_BD5	Out	LCD_B_Data5 output	yes
23	LCD0_BD6	Out	LCD_B_Data6 output	yes
24	LCD0_BD7	Out	LCD_B_Data7 output	yes
25	LCD0_HSYNC	Out	LCD_HSYNC output	yes
26	LCD0_VSYNC	Out	LCD_VSYNC output	yes
27	LCD0_VALID	Out	LCD_VALID output	yes
28	LCD0_CLK	Out	LCD clock output	yes

3.3.15. Audio Interface

IDX	Signal name	In / Out	Description	Pin share
1	I2S_MCKI	In	Audio master clock input	yes
2	I2S_MCKO	Out	Audio master clock output	yes
3	I2S0_BCK	IO	I2S0 audio serial clock	yes
4	I2S0_LRCK	IO	I2S0 audio L/R clock	yes
5	I2S0_DO	Out	I2S0 audio serial data output	yes
6	I2S1_BCK	IO	I2S1 audio serial clock	yes
7	I2S1_LRCK	IO	I2S1 audio L/R clock	yes
8	I2S1_DO	Out	I2S1 audio serial data output	yes
9	I2S1_DI	In	I2S1 audio serial data input	yes

3.3.16. PWM Output

IDX	Signal name	In / Out	Description	Pin share
1	PWM0_OUT0	Out	PWM output 0	yes
2	PWM0_OUT1	Out	PWM output 1	yes
3	PWM0_OUT2	Out	PWM output 2	yes
4	PWM0_OUT3	Out	PWM output 3	yes
5	PWM0_OUT4	Out	PWM output 4	yes
6	PWM0_OUT5	Out	PWM output 5	yes

3.3.17. Parallel Port Input Interface

IDX	Signal name	In / Out	Description	Pin share
1	PPI0_DI0	In	Parallel data input 0	yes
2	PPI0_DI1	In	Parallel data input 1	yes
3	PPI0_DI2	In	Parallel data input 2	yes
4	PPI0_DI3	In	Parallel data input 3	yes
5	PPI0_DI4	In	Parallel data input 4	yes
6	PPI0_DI5	In	Parallel data input 5	yes
7	PPI0_DI6	In	Parallel data input 6	yes
8	PPI0_DI7	In	Parallel data input 7	yes
9	PPI0_STB_N	In	Strobe input for parallel data input	yes
10	PPI0_ACK	Out	Acknowledge output for parallel data input	yes
11	PPI0_WBUSY	Out	Output of receive FIFO status	yes

3.3.18. GPIO Interfaces

IDX	Signal name	In / Out	Description	Pin share
1	GPIO0_0	IO	Programmable I/O 0 Note: The I/O power supply is VDD3V3_PA.	—
2	GPIO0_1	IO	Programmable I/O 1 Note: The I/O power supply is VDD3V3_PA.	—
3	GPIO0_2	IO	Programmable I/O 2 Note: The I/O power supply is VDD3V3_PA.	—
4	GPIO0_3	IO	Programmable I/O 3 Note: The I/O power supply is VDD3V3_PA.	—
5	GPIO0_4	IO	Programmable I/O 4 Note: Open drain type I/O	yes
6	GPIO0_5	IO	Programmable I/O 5 Note: Open drain type I/O	yes
7	GPIO0_6	IO	Programmable I/O 6 Note: Open drain type I/O	yes
8	GPIO0_7	IO	Programmable I/O 7 Note: Open drain type I/O	yes
9	GPIO0_8	IO	Programmable I/O 8 Note: Open drain type I/O	yes
10	GPIO0_9	IO	Programmable I/O 9 Note: Open drain type I/O	yes
11	GPIO0_10	IO	Programmable I/O 10	yes
12	GPIO0_11	IO	Programmable I/O 11	yes
13	GPIO0_12	IO	Programmable I/O 12	yes
14	GPIO0_13	IO	Programmable I/O 13	yes
15	GPIO0_14	IO	Programmable I/O 14	yes
16	GPIO0_15	IO	Programmable I/O 15	yes
17	GPIO0_16	IO	Programmable I/O 16	yes
18	GPIO0_17	IO	Programmable I/O 17	yes
19	GPIO0_18	IO	Programmable I/O 18	yes
20	GPIO0_19	IO	Programmable I/O 19	yes
21	GPIO0_20	IO	Programmable I/O 20	yes
22	GPIO0_21	IO	Programmable I/O 21	yes
23	GPIO0_22	IO	Programmable I/O 22	yes
24	GPIO0_23	IO	Programmable I/O 23	yes
25	GPIO0_24	IO	Programmable I/O 24	yes
26	GPIO0_25	IO	Programmable I/O 25	yes
27	GPIO0_26	IO	Programmable I/O 26	yes
28	GPIO0_27	IO	Programmable I/O 27	yes
29	GPIO0_28	IO	Programmable I/O 28	yes
30	GPIO0_29	IO	Programmable I/O 29	yes
31	GPIO0_30	IO	Programmable I/O 30	yes
32	GPIO0_31	IO	Programmable I/O 31	yes
33	GPIO1_0	IO	Programmable I/O 32	yes
34	GPIO1_1	IO	Programmable I/O 33	yes
35	GPIO1_2	IO	Programmable I/O 34	yes
36	GPIO1_3	IO	Programmable I/O 35	yes
37	GPIO1_4	IO	Programmable I/O 36	yes
38	GPIO1_5	IO	Programmable I/O 37	yes
39	GPIO1_6	IO	Programmable I/O 38	yes
40	GPIO1_7	IO	Programmable I/O 39	yes
41	GPIO1_8	IO	Programmable I/O 40	yes

IDX	Signal name	In / Out	Description	Pin share
42	GPIO1_9	IO	Programmable I/O 41	yes
43	GPIO1_10	IO	Programmable I/O 42	yes
44	GPIO1_11	IO	Programmable I/O 43	yes
45	GPIO1_12	IO	Programmable I/O 44	yes
46	GPIO1_13	IO	Programmable I/O 45	yes
47	GPIO1_14	IO	Programmable I/O 46	yes
48	GPIO1_15	IO	Programmable I/O 47	yes
49	GPIO1_16	IO	Programmable I/O 48	yes
50	GPIO1_17	IO	Programmable I/O 49	yes
51	GPIO1_18	IO	Programmable I/O 50	yes
52	GPIO1_19	IO	Programmable I/O 51	yes
53	GPIO1_20	IO	Programmable I/O 52	yes
54	GPIO1_21	IO	Programmable I/O 53	yes
55	GPIO1_22	IO	Programmable I/O 54	yes
56	GPIO1_23	IO	Programmable I/O 55	yes
57	GPIO1_24	IO	Programmable I/O 56	yes
58	GPIO1_25	IO	Programmable I/O 57	yes
59	GPIO1_26	IO	Programmable I/O 58	yes
60	GPIO1_27	IO	Programmable I/O 59	yes
61	GPIO1_28	IO	Programmable I/O 60	yes
62	GPIO1_29	IO	Programmable I/O 61	yes
63	GPIO1_30	IO	Programmable I/O 62	yes
64	GPIO1_31	IO	Programmable I/O 63	yes
65	GPIO2_0	IO	Programmable I/O 64	yes
66	GPIO2_1	IO	Programmable I/O 65	yes
67	GPIO2_2	IO	Programmable I/O 66	yes
68	GPIO2_3	IO	Programmable I/O 67	yes
69	GPIO2_4	IO	Programmable I/O 68	yes
70	GPIO2_5	IO	Programmable I/O 69	yes
71	GPIO2_6	IO	Programmable I/O 70	yes
72	GPIO2_7	IO	Programmable I/O 71	yes
73	GPIO2_8	IO	Programmable I/O 72	yes
74	GPIO2_9	IO	Programmable I/O 73	yes
75	GPIO2_10	IO	Programmable I/O 74	yes
76	GPIO2_11	IO	Programmable I/O 75	yes
77	GPIO2_12	IO	Programmable I/O 76	yes
78	GPIO2_13	IO	Programmable I/O 77	yes
79	GPIO2_14	IO	Programmable I/O 78	yes
80	GPIO2_15	IO	Programmable I/O 79	yes
81	GPIO2_16	IO	Programmable I/O 80	yes
82	GPIO2_17	IO	Programmable I/O 81	yes
83	GPIO2_18	IO	Programmable I/O 82	yes
84	GPIO2_19	IO	Programmable I/O 83	yes
85	GPIO2_20	IO	Programmable I/O 84	yes
86	GPIO2_21	IO	Programmable I/O 85	yes
87	GPIO2_22	IO	Programmable I/O 86	yes
88	GPIO2_23	IO	Programmable I/O 87	yes
89	GPIO2_24	IO	Programmable I/O 88	yes
90	GPIO2_25	IO	Programmable I/O 89	yes
91	GPIO2_26	IO	Programmable I/O 90	yes
92	GPIO2_27	IO	Programmable I/O 91	yes
93	GPIO2_28	IO	Programmable I/O 92	yes
94	GPIO2_29	IO	Programmable I/O 93	yes
95	GPIO2_30	IO	Programmable I/O 94	yes

IDX	Signal name	In / Out	Description	Pin share
96	GPIO2_31	IO	Programmable I/O 95	yes
97	GPIO3_0	IO	Programmable I/O 96	yes
98	GPIO3_1	IO	Programmable I/O 97	yes
99	GPIO3_2	IO	Programmable I/O 98	yes
100	GPIO3_3	IO	Programmable I/O 99	yes
101	GPIO3_4	IO	Programmable I/O 100	yes
102	GPIO3_5	IO	Programmable I/O 101	yes
103	GPIO3_6	IO	Programmable I/O 102	yes
104	GPIO3_7	IO	Programmable I/O 103	yes
105	GPIO3_8	IO	Programmable I/O 104	yes
106	GPIO3_9	IO	Programmable I/O 105	yes
107	GPIO3_10	IO	Programmable I/O 106	yes
108	GPIO3_11	IO	Programmable I/O 107	yes
109	GPIO3_12	IO	Programmable I/O 108	yes
110	GPIO3_13	IO	Programmable I/O 109	yes
111	GPIO3_14	IO	Programmable I/O 110	yes
112	GPIO3_15	IO	Programmable I/O 111	yes
113	GPIO3_16	IO	Programmable I/O 112	yes
114	GPIO3_17	IO	Programmable I/O 113	yes
115	GPIO3_18	IO	Programmable I/O 114	yes
116	GPIO3_19	IO	Programmable I/O 115	yes
117	GPIO3_20	IO	Programmable I/O 116	yes
118	GPIO3_21	IO	Programmable I/O 117	yes
119	GPIO3_22	IO	Programmable I/O 118	yes
120	GPIO3_23	IO	Programmable I/O 119	yes
121	GPIO3_24	IO	Programmable I/O 120	yes
122	GPIO3_25	IO	Programmable I/O 121	yes
123	GPIO3_26	IO	Programmable I/O 122	yes
124	GPIO3_27	IO	Programmable I/O 123	yes
125	GPIO3_28	IO	Programmable I/O 124	yes
126	GPIO3_29	IO	Programmable I/O 125	yes
127	GPIO3_30	IO	Programmable I/O 126	yes
128	GPIO3_31	IO	Programmable I/O 127	yes

3.3.19. AD Converter Input

IDX	Signal name	In / Out	Description
1	SAD0_DIN0	In	Successive AD converter input 0
2	SAD0_DIN1	In	Successive AD converter input 1
3	SAD0_DIN2	In	Successive AD converter input 2
4	SAD0_DIN3	In	Successive AD converter input 3

Note: 100 Ω or less drive impedance is recommended for a signal to be input to each SAD DIN pin.

3.3.20. JTAG interface for debugging

IDX	Signal name	In / Out	Description
1	DBG_TCK	In	Debug clock input Clock signal for the debug circuit of the ARM core
2	DBG_TDO	Out	Debug data output Serial data output for the debug circuit of the ARM core
3	DBG_TDI	In	Debug data input Serial data input for the debug circuit of the ARM core
4	DBG_TMS	In	Debug mode selection Debug mode select signal for the debug circuit of the ARM core
5	DBG_TRST_N	In	Debug reset Reset input signal for the debug circuit of the ARM core
6	DBG_SRST_N	In	Debug CPU reset Reset input signal for the ARM CPU

3.3.21. Others

IDX	Signal name	In / Out	Description	Pin share
1	VPGM	—	Test pin Connect to the GND	—
2	PD_BGR33	—	Test pin Connect to the GND	—
3	PD_POR33	—	Test pin Connect to the GND	—
4	BOOTSEL0	In	Boot mode select input 0	yes
5	BOOTSEL1	In	Boot mode select input 1	yes
6	BOOTSEL2	In	Boot mode select input 2	yes
7	BOOTSEL3	In	Boot mode select input 3	yes
8	BOOTSEL4	In	Boot mode select input 4	yes
9	BOOTSEL5	In	Boot mode select input 5	yes

3.3.22. VDDs and VSSs

IDX	Ball number	Pin name (note)	Attribute	Description
1	H9, H11, J8, J12, L8, L12, M7, M9, M11, N8, N12	VDDC_PA	Power	1.1 V power supply for CORE digital
2	N9, N10	VDD1V1_DDR	Power	1.1 V DDR digital power supply
3	P13	VDD1V1_DDRPLL	Power	1.1 V power supply for DDR PLL
4	P9, P10	VDD_DDRIO	Power	Power supply for DDR3 interface (when using the DDR3). 1.5 V for DDR3 or 1.35 V for DDR3L
5	M13	VDDPLL0	Power	1.1 V power supply for the clock PLL
6	L13	VDDPLL1	Power	1.1 V power supply for the clock PLL
7	N13	VDDPLL2	Power	1.1 V power supply for the clock PLL
8	P16, R16	VDD3V3_ADC	Power	3.3 V power supply for the AD converter reference voltage
9	L18, L19	VDD3V3_USB	Power	USB 3.3 V power supply
10	G7, G8	VDD1V8_3V3_EMMC	Power	Power supply for EMMC I/O
11	H7, J7	VDD1V8_3V3_SD0	Power	Power supply for SD0 I/O
12	G9, G10	VDD1V8_3V3_SD1	Power	Power supply for SD1 I/O
13	K7, L7	VDD3V3_PL_I2C	Power	Power supply for I2C I/O
14	G11, G12	VDD3V3_PL_EBUS	Power	Power supply for EBUS I/O
15	J13, K13	VDD3V3_PA	Power	3.3 V power supply for PA digital I/O
16	G13, H13	VDD3V3_PB	Power	3.3 V power supply for backup
17	A1, A19, H8, H10, H12, J9, J10, J11, J17, K8, K9, K10, K11, K12, L9, L10, L11, M8, M10, M12, N7, N11, P8, T3, T15, T16, T17, T18, T19, U2,U4,U6, U17,U19, V3, V5, V7, V17, V19, W1, W3, W5, W7, W18, W19	VSS	GND	GND
18	P17, R17	VSSADC	GND	ADC analog GND
19	N16, N18, N19	VSSUSB	GND	USB analog GND

Note: It is handled as a pin name in this section.

3.4. Setting Pin Functions

Some of pins are assigned to multiple functions in this product. The functions are switched by setting a register appropriately after booting up this product.

3.4.1. Setting pin function with Registers

The pin function can be selected after booting up by setting the below pin function configuration control registers (***[IO_PIN_SEL*]***) in the GCONF module.

Control register	Abbreviation	Address
[IO_PIN_SEL0]	PINS0	0x50028600
[IO_PIN_SEL1]	PINS1	0x50028604
[IO_PIN_SEL2]	PINS2	0x50028608
[IO_PIN_SEL3]	PINS3	0x5002860C
[IO_PIN_SEL4]	PINS4	0x50028610
[IO_PIN_SEL5]	PINS5	0x50028614

The following shows that each bit of the registers ***[IO_PIN_SEL*]*** selects a kind of function. After booting up, all bits of the registers are reset to zero, and the default functions are allocated to pins. Setting 0b1 at the bit of the registers changes function at the pin. The setting needs to be done with care since some of the configuration bits may affect multiple pins in one bit at once.

Don't set the plural function of anything but the default assigned to an identical ball at the same time. (The function which has high priority is chosen by function selection in share pin change setting, and the order of its priority will be default < function 3 < function 2 < function 1.)

* Basically, share pins set only the used function.

Table 3.2 shows the shared pins switching table.

Table 3.2 Shared Pin Switching Table

Ball num-ber	Default Signal name (Pin name)	Function 1		Function 2		Function 3	
		Control bit	Signal name	Control bit	Signal name	Control bit	Signal name
M1	BOOTSEL0	—	—	PINS4[0]	GPIO2_0	PINS2[0]	PWM0_OUT0
M2	BOOTSEL1	—	—	PINS4[1]	GPIO2_1	PINS2[1]	PWM0_OUT1
M3	BOOTSEL2	—	—	PINS4[2]	GPIO2_2	PINS2[2]	PWM0_OUT2
M4	BOOTSEL3	—	—	PINS4[3]	GPIO2_3	PINS2[3]	PWM0_OUT3
M5	BOOTSEL4	—	—	PINS4[4]	GPIO2_4	PINS2[4]	PWM0_OUT4
N1	BOOTSEL5	—	—	PINS4[5]	GPIO2_5	PINS2[5]	PWM0_OUT5
E5	EB0_ADD0	—	—	PINS3[27]	GPIO1_27	PINS2[7]	LCD0_CLK
D5	EB0_ADD1	—	—	PINS3[28]	GPIO1_28	PINS2[7]	LCD0_VSYNC
A6	EB0_ADD2	—	—	PINS3[29]	GPIO1_29	PINS2[7]	LCD0_HSYNC
B6	EB0_ADD3	—	—	PINS3[30]	GPIO1_30	PINS2[7]	LCD0_VALID
C6	EB0_ADD4	—	—	PINS3[31]	GPIO1_31	PINS2[7]	LCD0_RD0
E6	EB0_ADD5	—	—	—	—	PINS2[7]	LCD0_RD1
D6	EB0_ADD6	—	—	—	—	PINS2[7]	LCD0_RD2
D7	EB0_ADD7	—	—	—	—	PINS2[7]	LCD0_RD3
C7	EB0_ADD8	—	—	—	—	PINS2[7]	LCD0_RD4
B7	EB0_ADD9	—	—	—	—	PINS2[7]	LCD0_RD5
E7	EB0_ADD10	—	—	—	—	PINS2[7]	LCD0_RD6
A7	EB0_ADD11	—	—	—	—	PINS2[7]	LCD0_RD7
D8	EB0_ADD12	—	—	—	—	PINS2[7]	LCD0_GD0
B8	EB0_ADD13	—	—	—	—	PINS2[7]	LCD0_GD1
A8	EB0_ADD14	—	—	—	—	PINS2[7]	LCD0_GD2
E8	EB0_ADD15	—	—	PINS4[19]	GPIO2_19	PINS2[7]	LCD0_GD3
D9	EB0_ADD16	—	—	PINS4[20]	GPIO2_20	PINS2[7]	LCD0_GD4
C9	EB0_ADD17	—	—	PINS4[21]	GPIO2_21	PINS2[7]	LCD0_GD5
B9	EB0_ADD18	—	—	PINS4[22]	GPIO2_22	PINS2[7]	LCD0_GD6
A9	EB0_ADD19	—	—	PINS4[23]	GPIO2_23	PINS2[7]	LCD0_GD7
E9	EB0_ADD20	—	—	PINS4[24]	GPIO2_24	PINS2[7]	LCD0_BD0

Ball num-ber	Default Signal name (Pin name)	Function 1		Function 2		Function 3	
		Control bit	Signal name	Control bit	Signal name	Control bit	Signal name
D10	EB0_ADD21	—	—	PINS4[25]	GPIO2_25	PINS2[7]	LCD0_BD1
C10	EB0_ADD22	—	—	PINS4[26]	GPIO2_26	PINS2[7]	LCD0_BD2
B10	EB0_ADD23	—	—	PINS4[27]	GPIO2_27	PINS2[7]	LCD0_BD3
A10	EB0_ADD24	—	—	PINS4[28]	GPIO2_28	PINS2[7]	LCD0_BD4
E11	EB0_ADD25	—	—	PINS4[29]	GPIO2_29	PINS2[7]	LCD0_BD5
D11	EB0_ADD26	—	—	PINS4[30]	GPIO2_30	PINS2[7]	LCD0_BD6
C11	EB0_AVD_N	—	—	PINS4[31]	GPIO2_31	PINS2[7]	LCD0_BD7
B11	EB0_DAT0	—	—	PINS5[0]	GPIO3_0	PINS2[8]	CAM0_CLK
A11	EB0_DAT1	—	—	PINS5[1]	GPIO3_1	PINS2[8]	CAM0_VSYNC
E12	EB0_DAT2	—	—	PINS5[2]	GPIO3_2	PINS2[8]	CAM0_HSYNC
D12	EB0_DAT3	—	—	PINS5[3]	GPIO3_3	PINS2[8]	CAM0_DATA0
B12	EB0_DAT4	—	—	PINS5[4]	GPIO3_4	PINS2[8]	CAM0_DATA1
A12	EB0_DAT5	—	—	PINS5[5]	GPIO3_5	PINS2[8]	CAM0_DATA2
C13	EB0_DAT6	—	—	PINS5[6]	GPIO3_6	PINS2[8]	CAM0_DATA3
D13	EB0_DAT7	—	—	PINS5[7]	GPIO3_7	PINS2[8]	CAM0_DATA4
B13	EB0_DAT8	—	—	PINS5[8]	GPIO3_8	PINS2[8]	CAM0_DATA5
A13	EB0_DAT9	—	—	PINS5[9]	GPIO3_9	PINS2[8]	CAM0_DATA6
A14	EB0_DAT10	—	—	PINS5[10]	GPIO3_10	PINS2[8]	CAM0_DATA7
A15	EB0_DAT11	PINS2[9]	ETH0_RXD0	PINS5[11]	GPIO3_11	—	—
B14	EB0_DAT12	PINS2[9]	ETH0_RXD1	PINS5[12]	GPIO3_12	—	—
A16	EB0_DAT13	PINS2[9]	ETH0_CRSDV	PINS5[13]	GPIO3_13	PINS2[12]	SD1_CD
A17	EB0_DAT14	PINS2[9]	ETH0_MDIO	PINS5[14]	GPIO3_14	PINS2[13]	SD1_WP
A18	EB0_DAT15	—	—	PINS5[15]	GPIO3_15	—	—
B15	EB0_DAT16	—	—	PINS5[16]	GPIO3_16	—	—
C14	EB0_DAT17	—	—	PINS5[17]	GPIO3_17	—	—
B16	EB0_DAT18	—	—	PINS5[18]	GPIO3_18	—	—
B17	EB0_DAT19	—	—	PINS5[19]	GPIO3_19	—	—
B18	EB0_DAT20	—	—	PINS5[20]	GPIO3_20	—	—
D14	EB0_DAT21	—	—	PINS5[21]	GPIO3_21	—	—
B19	EB0_DAT22	—	—	PINS5[22]	GPIO3_22	—	—
C15	EB0_DAT23	—	—	PINS5[23]	GPIO3_23	—	—
C16	EB0_DAT24	—	—	PINS5[24]	GPIO3_24	—	—
C17	EB0_DAT25	—	—	PINS5[25]	GPIO3_25	—	—
C18	EB0_DAT26	—	—	PINS5[26]	GPIO3_26	—	—
C19	EB0_DAT27	—	—	PINS5[27]	GPIO3_27	—	—
D15	EB0_DAT28	—	—	PINS5[28]	GPIO3_28	—	—
D17	EB0_DAT29	—	—	PINS5[29]	GPIO3_29	—	—
D16	EB0_DAT30	—	—	PINS5[30]	GPIO3_30	—	—
D18	EB0_DAT31	—	—	PINS5[31]	GPIO3_31	—	—
D19	EB0_WE_N	—	—	PINS4[6]	GPIO2_6	—	—
B5 *	EB0_OE_N	—	—	PINS4[7]	GPIO2_7	PINS2[10]	SD1_CMD
A5 *	EB0_CLKO	—	—	PINS4[8]	GPIO2_8	PINS2[10]	SD1_CLK
E4 *	EB0_CLKI	—	—	PINS4[9]	GPIO2_9	PINS2[10]	SD1_CLKB
D4 *	EB0_CE0_N	—	—	PINS4[10]	GPIO2_10	PINS2[10]	SD1_DAT0
C4 *	EB0_CE1_N	—	—	PINS4[11]	GPIO2_11	PINS2[11]	SD1_DAT1
B4 *	EB0_CE2_N	—	—	PINS4[12]	GPIO2_12	PINS2[11]	SD1_DAT2
A4 *	EB0_CE3_N	—	—	PINS4[13]	GPIO2_13	PINS2[11]	SD1_DAT3
E16	EB0_BE0_N	PINS2[9]	ETH0_TXD0	PINS4[14]	GPIO2_14	—	—
E18	EB0_BE1_N	PINS2[9]	ETH0_TXD1	PINS4[15]	GPIO2_15	—	—
E15	EB0_BE2_N	—	—	PINS4[16]	GPIO2_16	—	—
E19	EB0_BE3_N	—	—	PINS4[17]	GPIO2_17	—	—
F17	EB0_WAIT_N	PINS2[9]	ETH0_REFCLK	PINS4[18]	GPIO2_18	—	—
F16	GPIO1_0	PINS2[9]	ETH0_MDC	PINS3[0]	GPIO1_0	PINS2[15]	SD1_V18EN
F15	GPIO1_1	PINS2[9]	ETH0_TXEN	PINS3[1]	GPIO1_1	PINS2[14]	SD1_POWER
K3	SPIB0_CLK	PINS0[0]	SPITX0_CLK	PINS3[2]	GPIO1_2	—	—
K5	SPIB0_IO0	PINS0[1]	SPITX0_DO	PINS3[3]	GPIO1_3	—	—
K4	SPIB0_IO1	—	—	PINS3[4]	GPIO1_4	—	—
L1	SPIB0_IO2	PINS0[3]	SPITX1_CLK	PINS3[5]	GPIO1_5	—	—
L2	SPIB0_IO3	PINS0[4]	SPITX1_DO	PINS3[6]	GPIO1_6	—	—
L4	SPIB0_CS0_N	PINS0[2]	SPITX0_CS_N	PINS3[7]	GPIO1_7	—	—
L5	SPIB0_CS1_N	PINS0[5]	SPITX1_CS_N	PINS3[8]	GPIO1_8	—	—
F4 *	SD0_CLK	PINS0[6]	SPITX2_CLK	PINS3[9]	GPIO1_9	—	—

Ball num-ber	Default Signal name (Pin name)	Function 1		Function 2		Function 3	
		Control bit	Signal name	Control bit	Signal name	Control bit	Signal name
F3 *	SD0_CLKB	—	—	PINS3[10]	GPIO1_10	—	—
F2 *	SD0_CMD	PINS0[7]	SPITX2_DO	PINS3[11]	GPIO1_11	—	—
F1 *	SD0_DAT0	PINS0[8]	SPITX2_CS_N	PINS3[12]	GPIO1_12	—	—
E3 *	SD0_DAT1	PINS0[9]	SPITX3_CLK	PINS3[13]	GPIO1_13	—	—
E2 *	SD0_DAT2	PINS0[10]	SPITX3_DO	PINS3[14]	GPIO1_14	—	—
E1 *	SD0_DAT3	PINS0[11]	SPITX3_CS_N	PINS3[15]	GPIO1_15	—	—
B1 *	EMMC0_CLK	PINS0[12]	SPITX4_CLK	PINS3[16]	GPIO1_16	—	—
C1 *	EMMC0_CLKB	—	—	PINS3[17]	GPIO1_17	—	—
D1 *	EMMC0_CMD	PINS0[13]	SPITX4_DO	PINS3[18]	GPIO1_18	—	—
A2 *	EMMC0_DAT0	PINS0[14]	SPITX4_CS_N	PINS3[19]	GPIO1_19	—	—
B2 *	EMMC0_DAT1	PINS0[15]	SPITX5_CLK	PINS3[20]	GPIO1_20	—	—
C2 *	EMMC0_DAT2	PINS0[16]	SPITX5_DO	PINS3[21]	GPIO1_21	—	—
D2 *	EMMC0_DAT3	PINS0[17]	SPITX5_CS_N	PINS3[22]	GPIO1_22	—	—
A3 *	EMMC0_DAT4	PINS0[18]	SPITX6_CLK	PINS3[23]	GPIO1_23	—	—
B3 *	EMMC0_DAT5	PINS0[19]	SPITX6_DO	PINS3[24]	GPIO1_24	—	—
C3 *	EMMC0_DAT6	PINS0[20]	SPITX6_CS_N	PINS3[25]	GPIO1_25	—	—
D3 *	EMMC0_DAT7	—	—	PINS3[26]	GPIO1_26	—	—
R2 **	GPIO0_4	—	—	PINS0[25]	I2C1_SDA	—	—
R3 **	GPIO0_5	—	—	PINS0[25]	I2C1_SCL	—	—
R4 **	GPIO0_6	PINS0[21]	PPI0_DI0	PINS0[26]	I2C2_SDA	—	—
R5 **	GPIO0_7	PINS0[21]	PPI0_DI1	PINS0[26]	I2C2_SCL	—	—
T1 **	GPIO0_8	PINS0[21]	PPI0_DI2	PINS0[27]	I2C3_SDA	—	—
T2 **	GPIO0_9	PINS0[21]	PPI0_DI3	PINS0[27]	I2C3_SCL	—	—
N4	GPIO0_10	PINS0[21]	PPI0_DI4	PINS0[28]	UA1_RXD	—	—
N5	GPIO0_11	PINS0[21]	PPI0_DI5	PINS0[29]	UA1_TXD	—	—
P5	GPIO0_12	PINS0[21]	PPI0_DI6	PINS0[30]	UA1_CTS_N	—	—
P1	GPIO0_13	PINS0[21]	PPI0_DI7	PINS0[30]	UA1_RTS_N	—	—
P2	GPIO0_14	PINS0[21]	PPI0_STB_N	PINS0[31]	UA1_EXCLK	—	—
F5	GPIO0_15	—	—	PINS1[0]	UA2_RXD	PINS1[18]	SPIM0_DI
G1	GPIO0_16	—	—	PINS1[1]	UA2_TXD	PINS1[17]	SPIM0_DO
G2	GPIO0_17	—	—	PINS1[2]	UA2_CTS_N	PINS1[16]	SPIM0_CS_N
G5	GPIO0_18	—	—	PINS1[2]	UA2_RTS_N	PINS1[16]	SPIM0_CLK
G3	GPIO0_19	—	—	PINS1[4]	UA3_RXD	PINS1[24]	SPIS0_DI
G4	GPIO0_20	—	—	PINS1[5]	UA3_TXD	PINS1[23]	SPIS0_DO
H1	GPIO0_21	—	—	PINS1[6]	UA3_CTS_N	PINS1[22]	SPIS0_CLK
H2	GPIO0_22	—	—	PINS1[6]	UA3_RTS_N	PINS1[22]	SPIS0_CS_N
H5	GPIO0_23	—	—	PINS1[14]	I2S_MCKI	PINS1[15]	I2S_MCKO
H4	GPIO0_24	—	—	PINS1[8]	I2S0_BCK	PINS1[19]	SPIM1_CLK
J1	GPIO0_25	—	—	PINS1[8]	I2S0_LRCK	PINS1[19]	SPIM1_CS_N
J2	GPIO0_26	—	—	PINS1[9]	I2S0_DO	PINS1[20]	SPIM1_DO
J3	GPIO0_27	PINS0[22]	PPI0_ACK	PINS1[27]	SPIS0_DI	PINS1[31]	SD0_V18EN
J5	GPIO0_28	PINS1[25]	SPIS0_CLK	PINS1[11]	I2S1_BCK	PINS1[28]	SD0_CD
J4	GPIO0_29	PINS1[25]	SPIS0_CS_N	PINS1[11]	I2S1_LRCK	PINS1[29]	SD0_WP
K1	GPIO0_30	PINS1[26]	SPIS0_DO	PINS1[12]	I2S1_DO	PINS1[30]	SD0_POWER
K2	GPIO0_31	PINS0[23]	PPI0_WBUSY	PINS1[13]	I2S1_DI	PINS1[21]	SPIM1_DI

Note: The pin in which "*" is written in "ball number" is SD-IO structure (3.3 V or 1.8 V interface bidirectional multi-drive buffer).

The pin in which "**" is written in "ball number", and the I2C0_SDA pin, and the I2C0_SCL pin are open drain type structure.

4. Electrical characteristics

4.1. Absolute Maximum ratings

Item	Symbol	Maximum rating	Unit
Supply voltage	VDDMAX	-0.3 to (VDD+0.3) (Note 1)	V
Input voltage	V_{IN}MAX	-0.3 to (VDD+0.3) (Note 1)	V
Output voltage	V_{OUT}MAX	-0.3 to (VDD+0.3) (Note 1)	V
Input current	I_{IN}	±10	mA
Storage temperature	T_{stg}	-40 to 125	°C

Note 1: VDD is a supply voltage which is described in operating conditions of next section.

4.2. Recommended Operating Conditions

Operating conditions are divided in three types according to product types.

4.2.1. Operating Conditions of the TZ2100XBG

Item	Symbol (target power supply pin name)	Condition	Min	Typ.	Max	Unit
Supply Voltage Range	VDDC_PA	—	1.00	1.10	1.20	V
	VDDPLL0	—	1.00	1.10	1.20	V
	VDDPLL1	—	1.00	1.10	1.20	V
	VDDPLL2	—	1.00	1.10	1.20	V
	VDD1V1_DDR	—	1.00	1.10	1.20	V
	VDD1V1_DDRPLL	—	1.00	1.10	1.20	V
	VDD_DDRIO	When connected to DDR3	1.425	1.50	1.575	V
		When connected to DDR3L	1.283	1.35	1.45	
	VDD3V3_PA	—	3.00	3.30	3.60	V
	VDD3V3_PL_EBUS	—	3.00	3.30	3.60	V
	VDD3V3_PL_I2C	—	3.00	3.30	3.60	V
	VDD1V8_3V3_SD0	—	2.70	3.30	3.60	V
		(Note 1)	1.70	1.80	1.95	
	VDD1V8_3V3_SD1	(Note 2)	2.70	3.30	3.60	V
		(Note 1)	1.70	1.80	1.95	
	VDD1V8_3V3_EMMC	—	2.70	3.30	3.60	V
		(Note 1)	1.70	1.80	1.95	
	VDD3V3_USB	—	3.15	3.30	3.45	V
	VDD3V3_ADC	—	3.00	3.30	3.60	V
	VDD3V3_PB	(Note 4)	3.00	3.30	3.60	V
Operating Temperature Range	T_a (ambient temperature)	—	-20	—	80	°C
		(Note 3)	-40	—	85	

Note: A voltage difference between a minimum voltage and a maximum voltage in group of 1.1 V power supplies are required to be within 100 mV.

Note 1: When using as a 1.8 V interface mode.

Note 2: When using the VDD1V8_3V3_SD1 as EBUS, apply the same supply voltage as the VDD3V3_PL_EBUS to the VDD1V8_3V3_SD1. In this case, the minimum operating voltage is 3.0 V.

Note 3: Optional with the extended operating temperature products.

Note 4: The minimum operating voltage is 2.0 V when using SRAM data retention for the buck-up and RTC operation.

4.2.2. Operating Conditions of TZ2102XBG

Item	Symbol (target power supply pin name)	Condition	Min	Typ.	Max	Unit
Supply Voltage Range	VDDC_PA	—	1.06	1.135	1.21	V
	VDDPLL0	—	1.06	1.135	1.21	V
	VDDPLL1	—	1.06	1.135	1.21	V
	VDDPLL2	—	1.06	1.135	1.21	V
	VDD1V1_DDR	—	1.06	1.135	1.21	V
	VDD1V1_DDRPLL	—	1.06	1.135	1.21	V
	VDD_DDRIO	When connected to DDR3	1.425	1.50	1.575	V
		When connected to DDR3L	1.283	1.35	1.45	
	VDD3V3_PA	—	3.00	3.30	3.60	V
	VDD3V3_PL_EBUS	—	3.00	3.30	3.60	V
	VDD3V3_PL_I2C	—	3.00	3.30	3.60	V
	VDD1V8_3V3_SD0	—	2.70	3.30	3.60	V
		(Note 1)	1.70	1.80	1.95	
	VDD1V8_3V3_SD1	(Note 2)	2.70	3.30	3.60	V
		(Note 1)	1.70	1.80	1.95	
	VDD1V8_3V3_EMMC	—	2.70	3.30	3.60	V
		(Note 1)	1.70	1.80	1.95	
	VDD3V3_USB	—	3.15	3.30	3.45	V
	VDD3V3_ADC	—	3.00	3.30	3.60	V
	VDD3V3_PB	(Note 3)	3.00	3.30	3.60	V
Operating Temperature Range	T_a (ambient temperature)	—	-20	—	80	°C

Note: A voltage difference between a minimum voltage and a maximum voltage in group of 1.1 V power supplies are required to be within 100 mV

Note 1: When using as a 1.8 V interface mode.

Note 2: When using the VDD1V8_3V3_SD1 as EBUS, apply the supply voltage same as the VDD3V3_PL_EBUS to the VDD1V8_3V3_SD1. In this case, the minimum operating voltage is 3.0 V.

Note 3: The minimum operating voltage is 2.0 V when using SRAM data retention for the buck-up and RTC operation.

4.2.3. Operating Conditions of TZ2101XBG/TZ2102XBG (Extended Temperature Products)

Item	Symbol (target power supply pin name)	Condition	Min	Typ.	Max	Unit
Supply Voltage Range	VDDC_PA	—	1.10	1.15	1.20	V
	VDDPLL0	—	1.10	1.15	1.20	V
	VDDPLL1	—	1.10	1.15	1.20	V
	VDDPLL2	—	1.10	1.15	1.20	V
	VDD1V1_DDR	—	1.10	1.15	1.20	V
	VDD1V1_DDRPLL	—	1.10	1.15	1.20	V
	VDD_DDRIO	When connected to DDR3	1.425	1.50	1.575	V
		When connected to DDR3L	1.283	1.35	1.45	
	VDD3V3_PA	—	3.00	3.30	3.60	V
	VDD3V3_PL_EBUS	—	3.00	3.30	3.60	V
	VDD3V3_PL_I2C	—	3.00	3.30	3.60	V
	VDD1V8_3V3_SD0	—	2.70	3.30	3.60	V
		(Note 1)	1.70	1.80	1.95	
	VDD1V8_3V3_SD1	(Note 2)	2.70	3.30	3.60	V
		(Note 1)	1.70	1.80	1.95	
	VDD1V8_3V3_EMMC	—	2.70	3.30	3.60	V
		(Note 1)	1.70	1.80	1.95	
	VDD3V3_USB	—	3.15	3.30	3.45	V
	VDD3V3_ADC	—	3.00	3.30	3.60	V
	VDD3V3_PB	(Note 3)	2.70	3.30	3.60	V
Operating Temperature Range	T_a (ambient temperature)	—	-40	—	85	°C

Note 1: When using as a 1.8 V interface mode.

Note 2: When using the VDD1V8_3V3_SD1 as EBUS, apply the supply voltage same as the VDD3V3_PL_EBUS to the VDD1V8_3V3_SD1. In this case, the minimum operating voltage is 3.0 V.

Note 3: The minimum operating voltage is 2.0 V when using SRAM data retention for the buck-up and RTC operation.

4.3. Current Dissipations

Item	Symbol	Measurement of power supply terminal	Max	Unit
Current dissipation 1	IDDC	VDDC_PA, VDD1V1_DDR VDDPLL0, VDDPLL1, VDDPLL2, VDD1V1_DDRPLL	1.19 (Note 1)	A
Current dissipation 2	IDD_DDR	VDD1V1_DDR, VDD1V1_DDRPLL	74 (Note 2)	mA
Current dissipation 3	IDD_DDRIO	VDD_DDRIO	95 (Note 2)	mA
Current dissipation 4	IDD3V3_PB	VDD3V3_PB	10 (Note 3)	μA
Current dissipation 5	IDD1V8_3V3_SD0	VDD1V8_3V3_SD0	24 (Note 4)	mA
Current dissipation 6	IDD3V3_3V3_SD1	VDD1V8_3V3_SD1	24 (Note 4)	mA
Current dissipation 7	IDD1V8_3V3_EMMC	VDD1V8_3V3_EMMC	50 (Note 4)	mA
Current dissipation 8	IDD3V3_USB	VDD3V3_USB	35 (Note 5)	mA

Note: The maximum current values are calculated from the maximum value during the execution of the following software, in addition of each item such as device variation, power supply voltage, package temperature and internal operation conditions unless otherwise specified.

Note 1: Application software for demonstration with LCD panel display (made by Toshiba)

Note 2: Evaluation software for SDRAM (made by Toshiba), when supply voltage of VDD_DDRIO is 1.45 V

Note 3: Evaluation software for Back-up mode in power state (made by Toshiba). Data backup operating at the Back up SRAM and RTC operating are carried on this software. A ambient temperature is at 60 °C.

Note4: Evaluation software for eMMC or SD Card (made by Toshiba), when supply voltage of VDD1V8_3V3 is 1.95 V.

Note5: Evaluation software for USB (made by Toshiba).

4.4. DC Characteristics

4.4.1. Digital I/O pins

This table is specified Digital I/O pin, NOT included SD-IO type. The field "I/O cell attribute" shows "Open drain type" for the characteristics of open drain type.

(VDD3V3_PA, VDD3V3_PB, VDD3V3_PL_I2C, VDD3V3_PL_EBUS = 3.0 V to 3.6 V)

Item	Symbol	I/O cell attribution	Conditions	Min	Max	Unit
Low-level input voltage	V_{IL}	Input (without Schmitt-trigger) Input (with Schmitt-trigger)	—	VSS	0.8	V
		Input (Open drain)	—	VSS	VDD × 0.3	V
High-level input voltage	V_{IH}	Input (without Schmitt-trigger)	—	2.0	VDD	V
		Input (with Schmitt-trigger)	—	2.1	VDD	V
		Input (Open drain)	—	VDD × 0.7	5.5	V
Low-level input current	I_{IL}	Input (HiZ, PD)	V_{IN} = VSS	-10	10	μA
		Input (PU)	V_{IN} = VSS	-200	-10	μA
		Input (Open drain)	V_{IN} = VSS	-10	10	μA
High-level input current	I_{IH}	Input (HiZ, PU)	V_{IN} = VDD	-10	10	μA
		Input (PD)	V_{IN} = VDD	10	200	μA
		Input (Open drain)	V_{IN} = VDD	-10	10	μA
Low-level output voltage	V_{OL}	Output	I_{OL} = 4 mA	—	0.4	V
			I_{OL} = 8 mA	—	0.4	V
		Output (Open drain)	I_{OL} = 8 mA	—	0.4	V
High-level output voltage	V_{OH}	Output	I_{OH} = -4 mA	VDD-0.4	—	V
			I_{OH} = -8 mA	VDD-0.4	—	V

Note: HiZ, PD, and PU in the above table respectively indicate high-impedance, with a pull-down resistor, and with a pill-up resistor. Input direction and output direction can be set to be fixed or programmable for some I/O. Table 3.2 is described pins of the open drain type structure and the SD-IO structure.

4.4.2. eMMC/SD Card/SDIO pins

This section describes the pin characteristics the SD-IO type shown in Table 3.2.

(VDD1V8_3V3_EMMC, VDD1V8_3V3_SD0, VDD1V8_3V3_SD1 = 2.7 V to 3.6 V)

Item	Symbol	I/O attribution	Conditions	Min	Max	Unit
Low-level input voltage	V_{IL}	Input	—	VSS	VDD × 0.25	V
High-level input voltage	V_{IH}	Input	—	VDD × 0.625	VDD	V
Low-level input current	I_{IL}	Input (when high-impedance)	V_{IN} = VSS	-10	10	μA
		Input (with pull-up resistor)	V_{IN} = VSS	-360	-30	μA
High-level input current	I_{IH}	Input	V_{IN} = VDD	-10	10	μA
Low-level output voltage	V_{OL}	Output	I_{OL} = 2 mA	—	VDD × 0.125	V
High-level output voltage	V_{OH}	Output	I_{OH} = -2 mA	VDD × 0.75	—	V

(VDD1V8_3V3_EMMC, VDD1V8_3V3_SD0, VDD1V8_3V3_SD1 = 1.7 V to 1.95 V)

Item	Symbol	I/O attribution	Conditions	Min	Max	Unit
Low-level input voltage	V_{IL}	Input	—	VSS	0.58	V
High-level input voltage	V_{IH}	Input	—	1.27	VDD	V
Low-level input current	I_{IL}	Input (when high-impedance)	V_{IN} = VSS	-2	2	μA
		Input (with pull-up resistor)	V_{IN} = VSS	-195	-18	μA
High-level input current	I_{IH}	Input	V_{IN} = VDD	-2	2	μA
Low-level output voltage	V_{OL}	Output	I_{OL} = 2 mA	—	0.45	V
High-level output voltage	V_{OH}	Output	I_{OH} = -2 mA	1.40	—	V

4.5. AC Characteristics

4.5.1. Clock Inputs

Oscillation frequency with a crystal resonator

Item	Symbol	Conditions	Min	Typ.	Max	Unit
Oscillator Frequency	fOSC24M	—	—	24	—	MHz

Tolerance**:** ±100 ppm

Oscillation frequency with an external oscillator

Item	Symbol	Conditions	Min	Typ.	Max	Unit
External Clock Source Frequency	fEXT24M	—	—	24	—	MHz

Tolerance**:** ±100 ppm

Oscillation frequency with a crystal resonator

Item	Symbol	Conditions	Min	Typ.	Max	Unit
Oscillator Frequency	fOSC32K	—	—	32.768	—	kHz

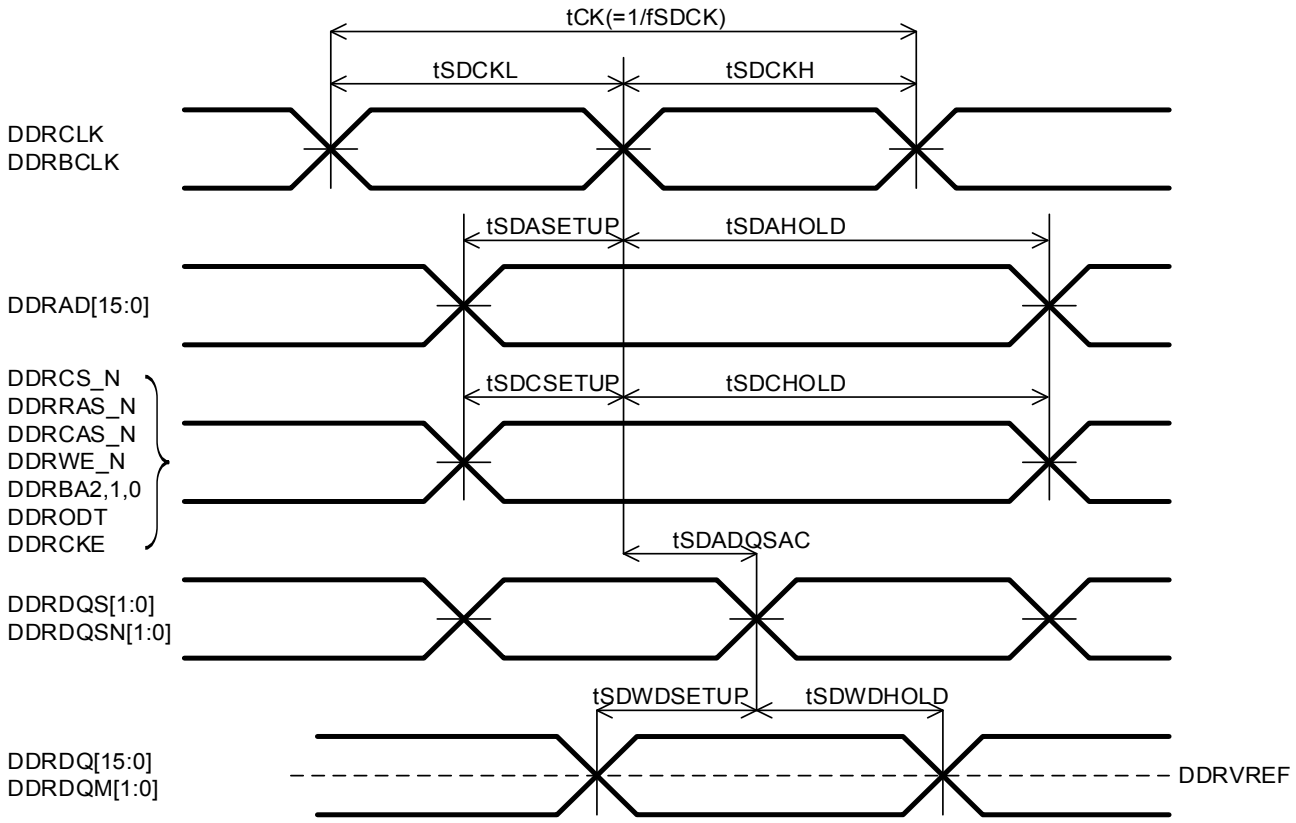
Tolerance**:** ±20 ppm
However, it depends on the accuracy required for the RTC.

Oscillation frequency with an external oscillator

Item	Symbol	Conditions	Min	Typ.	Max	Unit
External Clock Source Frequency	fEXT32K	—	—	32.768	—	kHz

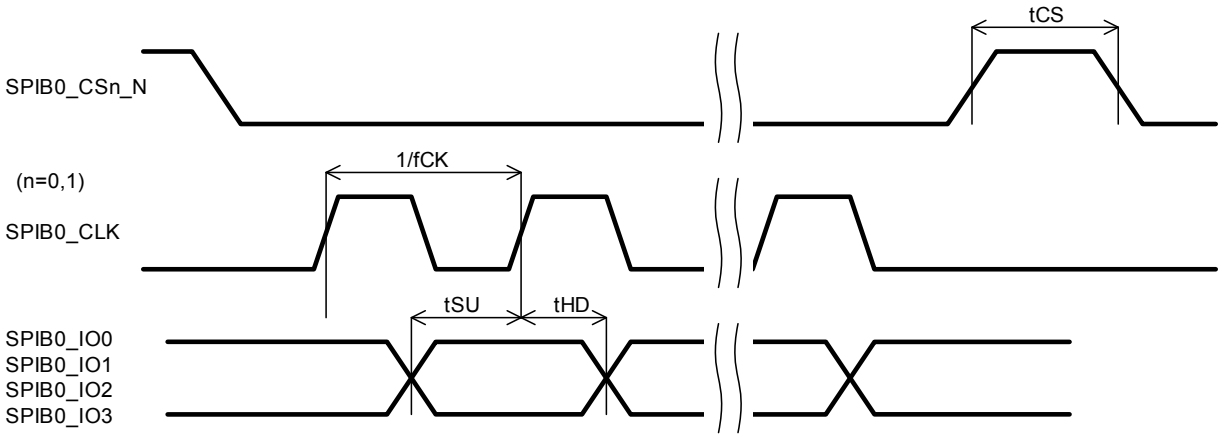
Tolerance**:** ±20 ppm
However, it depends on the accuracy required for the RTC.

4.5.2. DDR3/DDR3L Memory Interface

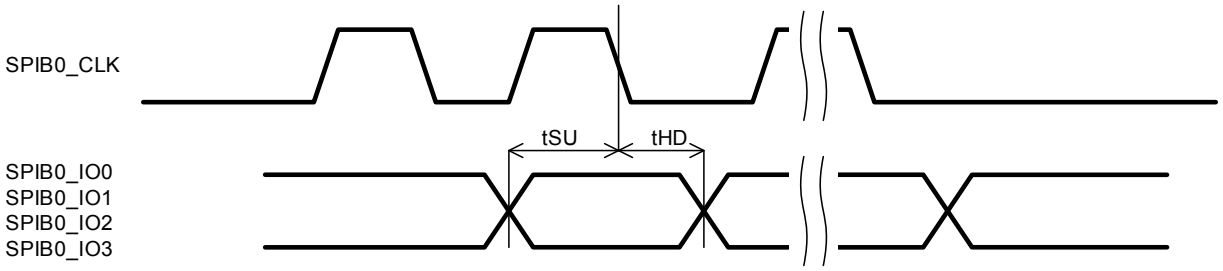


Item	Symbol	Conditions	800 Mbps		Unit
			Min	Max	
DDRCLK frequency	fSDCK	—	—	400	MHz
DDRCLK clock period	tCK	—	2.5	—	ns
DDRCLK H level width	tSDCKH	—	0.47	0.53	tCK
DDRCLK L level width	tSDCKL	—	0.47	0.53	tCK
Address/Command output setup time	tSDASETUP tSDCSETUP	—	200	—	ps
Address/Command output hold time	tSDAHOLD tSDCHOLD	—	275	—	ps
DDRDQS output delay time	tSDADQSAC	—	-0.25	0.25	tCK
Data output setup time	tSDWDSETUP	—	75	—	ps
Data output hold time	tSDWDHOLD	—	150	—	ps

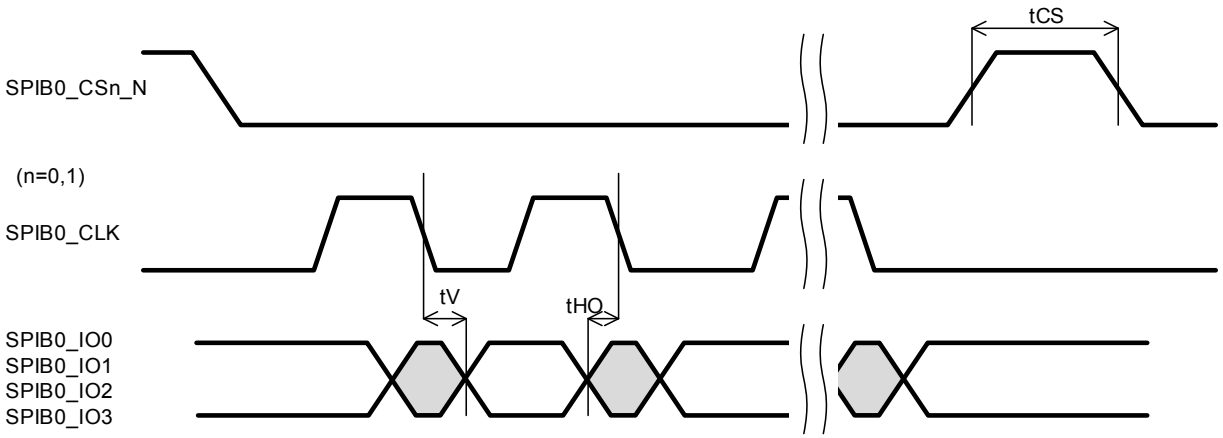
4.5.3. SPI Flash Memory Controller Interface



Input Timing (SDCE: rising edge) (Note 1)



Input Timing (SDCE: falling edge) (Note 1)



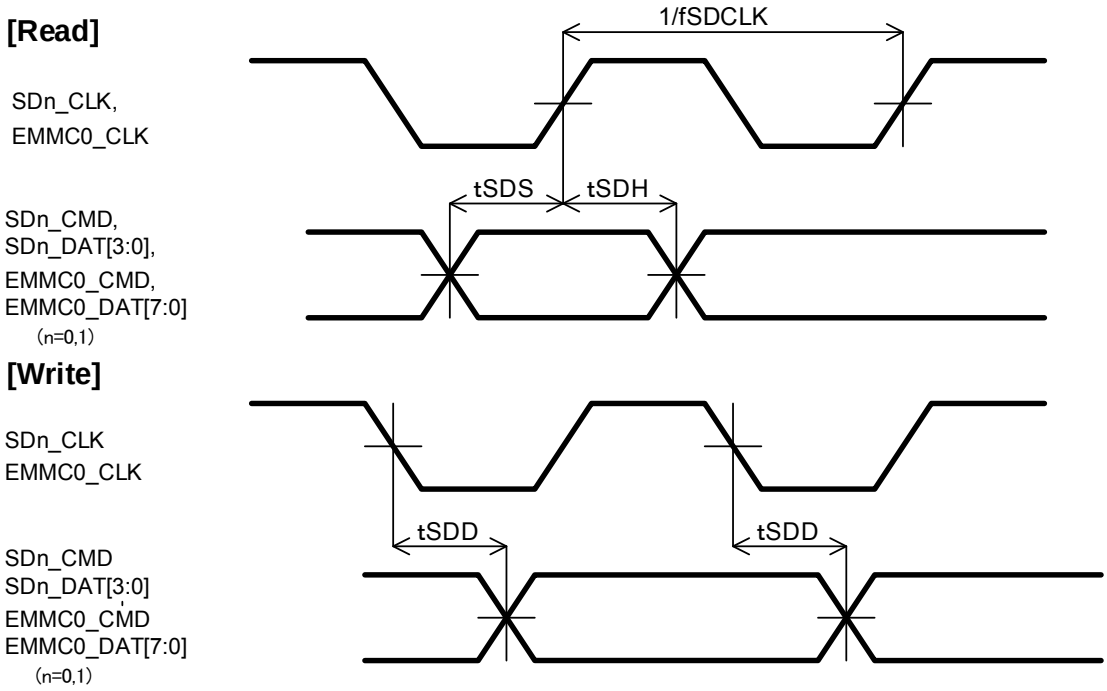
Output Timing

Item	Symbol	Conditions	Min	Typ.	Max	Unit
SPI_CLK Clock Frequency	fCK	—	18.75	—	50	MHz
Data in Setup Time	tSU	—	3	—	—	ns
Data in Hold Time	tHD	—	10	—	—	ns
Output Valid	tV	—	—	—	4.5	ns
Output Hold Time	tHO	—	2.5	—	—	ns
Chip Select High Time	tCS	—	(Note 2)			ns

Note 1: The input timing can be selected the following two modes, SDCE; Rising edge and SDCE Falling edge.

Note 2: The tCS can be set up 5100 ns by SCSD.

4.5.4. eMMC / SD Card / SDIO Interface



SD Card Default Speed

Item	Symbol	Conditions	Min	Typ.	Max	Unit
Clock frequency	fSDCLK	—	—	—	25	MHz
CMD/DATA output delay time	tSDD	C_L < 40pF (Note 1)	0	—	11	ns
CMD/DATA setup time	tSDS	—	5.5	—	—	ns
CMD/DATA hold time	tSDH	—	7.8	—	—	ns

Legacy MMC

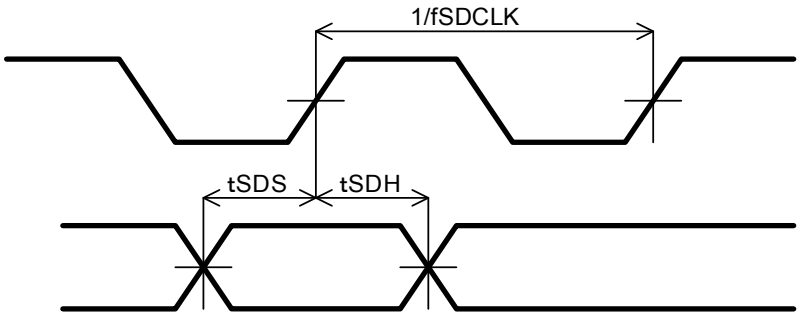
Item	Symbol	Conditions	Min	Typ.	Max	Unit
Clock frequency	fSDCLK	—	—	—	25	MHz
CMD/DATA output delay time	tSDD	C_L < 40pF (Note 1)	0	—	11	ns
CMD/DATA setup time	tSDS	—	5.5	—	—	ns
CMD/DATA hold time	tSDH	—	7.8	—	—	ns

Note 1: External load capacity (C_L)

[Read]

SDn_CLK
EMMC0_CLK

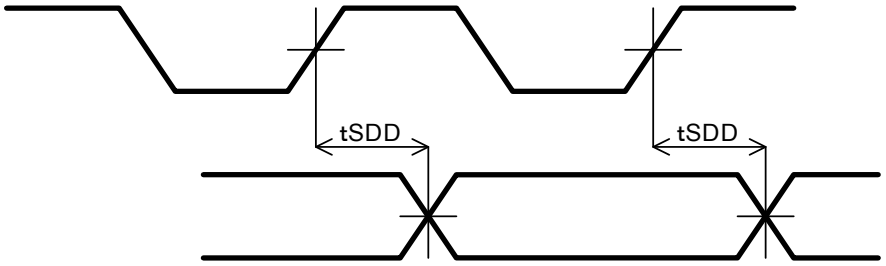
SDn_CMD,
SDn_DAT[3:0],
EMMC0_CMD,
EMMC0_DAT[7:0]
(n=0,1)



[Write]

SDn_CLK
EMMC0_CLK

SDn_CMD,
SDn_DAT[3:0]
EMMC0_CMD,
EMMC0_DAT[7:0]
(n=0,1)



SD Card High Speed

Item	Symbol	Conditions	Min	Typ.	Max	Unit
Clock frequency	fSDCLK	—	—	—	50	MHz
CMD/DATA output delay time	tSDD	C_L < 40pF (Note 1)	3.5	—	13.5	ns
CMD/DATA setup time	tSDS	—	5.5	—	—	ns
CMD/DATA hold time	tSDH	—	2.0	—	—	ns

SD Card SDR12

Item	Symbol	Conditions	Min	Typ.	Max	Unit
Clock frequency	fSDCLK	—	—	—	25	MHz
CMD/DATA output delay time	tSDD	C_L < 40pF (Note 1)	3.5	—	13.5	ns
CMD/DATA setup time	tSDS	—	5.5	—	—	ns
CMD/DATA hold time	tSDH	—	2.0	—	—	ns

SD Card SDR25

Item	Symbol	Conditions	Min	Typ.	Max	Unit
Clock frequency	fSDCLK	—	—	—	50	MHz
CMD/DATA output delay time	tSDD	C_L < 40pF (Note 1)	3.5	—	13.5	ns
CMD/DATA setup time	tSDS	—	5.5	—	—	ns
CMD/DATA hold time	tSDH	—	2.0	—	—	ns

Note 1: External load capacity (C_L)

SD Card SDR50

Item	Symbol	Conditions	Min	Typ.	Max	Unit
Clock frequency	fSDCLK	—	—	—	100	MHz
CMD/DATA output delay time	tSDD	C_L < 30pF (Note 1)	1.3	—	6.5	ns
CMD/DATA setup time	tSDS	—	2.0	—	—	ns
CMD/DATA hold time	tSDH	—	1.0	—	—	ns

SD Card SDR104

Item	Symbol	Conditions	Min	Typ.	Max	Unit
Clock frequency	fSDCLK	—	—	—	150	MHz
CMD/DATA output delay time	tSDD	C_L < 15pF (Note 1)	1.30	—	4.77	ns
CMD/DATA setup time	tSDS	—	1.42	—	—	ns
CMD/DATA hold time	tSDH	—	1.42	—	—	ns

eMMC High Speed SDR

Item	Symbol	Conditions	Min	Typ.	Max	Unit
Clock frequency	fSDCLK	—	—	—	50	MHz
CMD/DATA output delay time	tSDD	C_L < 40pF (Note 1)	3.5	—	13.5	ns
CMD/DATA setup time	tSDS	—	5.5	—	—	ns
CMD/DATA hold time	tSDH	—	2.0	—	—	ns

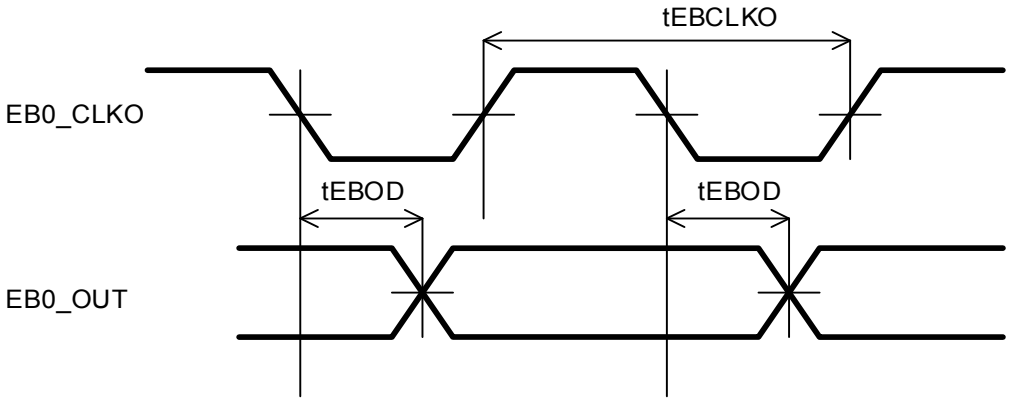
eMMC HS200

Item	Symbol	Conditions	Min	Typ.	Max	Unit
Clock frequency	fSDCLK	—	—	—	150	MHz
CMD/DATA output delay time	tSDD	C_L < 15pF (Note 1)	1.30	—	4.77	ns
CMD/DATA setup time	tSDS	—	1.42	—	—	ns
CMD/DATA hold time	tSDH	—	1.42	—	—	ns

Note 1: External load capacity (C_L)

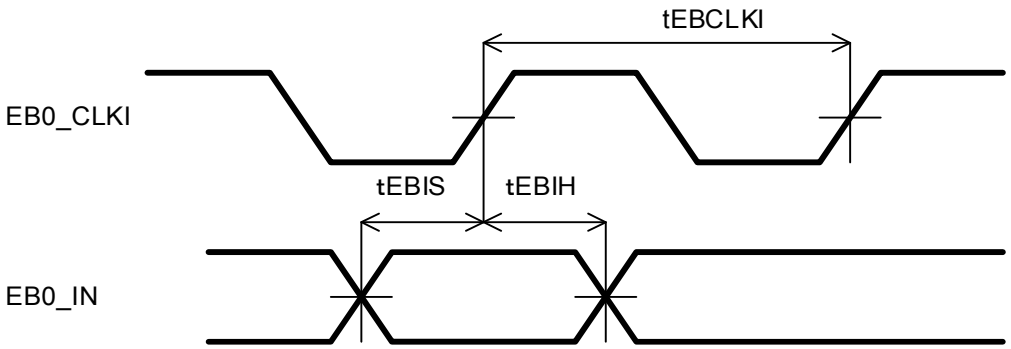
4.5.5. External Bus Interface

4.5.5.1. Synchronous mode



Output Signal

Item	Symbol	Conditions	Min	Typ.	Max	Unit
Clock Cycle Time	fEBCLKO	(Note 1)	—	40	—	ns
Output Data Delay Time	tEBOD	(Note 1)	0.5	—	10	ns



Input Signal

Item	Symbol	Conditions	Min	Typ.	Max	Unit
Clock Cycle Time	tEBCLKI	(Note 2)	—	40	—	ns
Input Data Setup Time	tEBIS	(Note 3)	10	—	—	ns
Input Data Hold Time	tEBIH	(Note 3)	0.5	—	—	ns

Note 1: External load capacity (C_L)

$$C_L = \begin{cases} 40\ (\max) \\ 6\ (\min) \end{cases} [\mathrm{pF}]$$

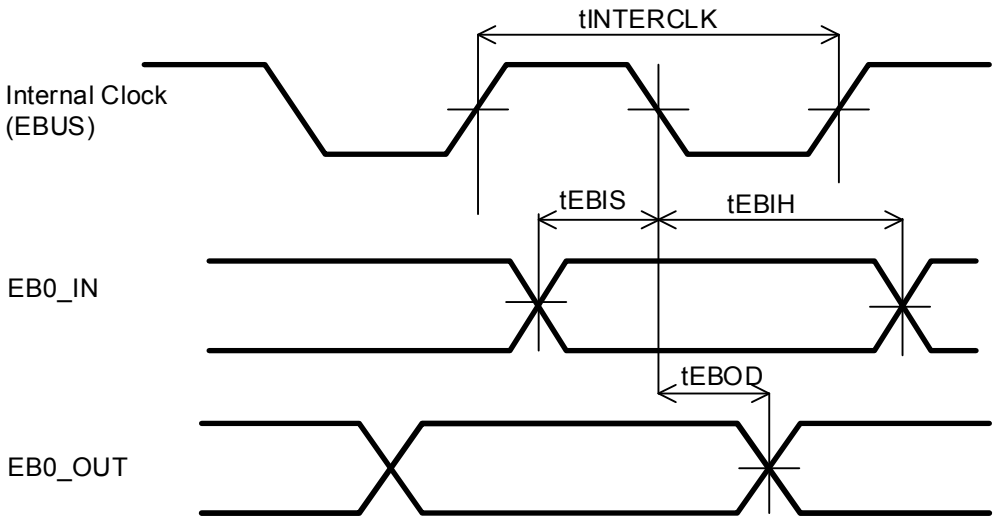
Note 2: Connect to the dummy line of pattern layout between EB0_CLKI and EB0_CLKO on board, and locate the end point of this line to be close to an external peripheral device in layout. Design signal delay 2 ns or less on board.

Note 3: Transition Time (20% - 80%)

$$\text{Transition Time} = \begin{cases} 1.0\ (\max) \\ 0\ (\min) \end{cases} [\mathrm{ns}]$$

Refer to the timing chart in the Chapter 27 of the reference manual of the External BUS Interface. These show the operation is based on the clock timing of EB0_CLKO.

4.5.5.2. Asynchronous Mode



Item	Symbol	Conditions	Min	Typ.	Max	Unit
Clock Cycle Time	tINTERCLK	(Note 1) (Note 2)	10	—	40	ns
Output Data Delay Time	tEBOD	(Note 1)	0	—	15	ns
Input Data Setup Time	tEBIS	(Note 3)	10	—	—	ns
Input Data Hold Time	tEBIH	(Note 3)	1	—	—	ns

Note 1: External load capacity (C_L)

$$C_L = \begin{cases} 40\ (\max) \\ 6\ (\min) \end{cases} [\mathrm{pF}]$$

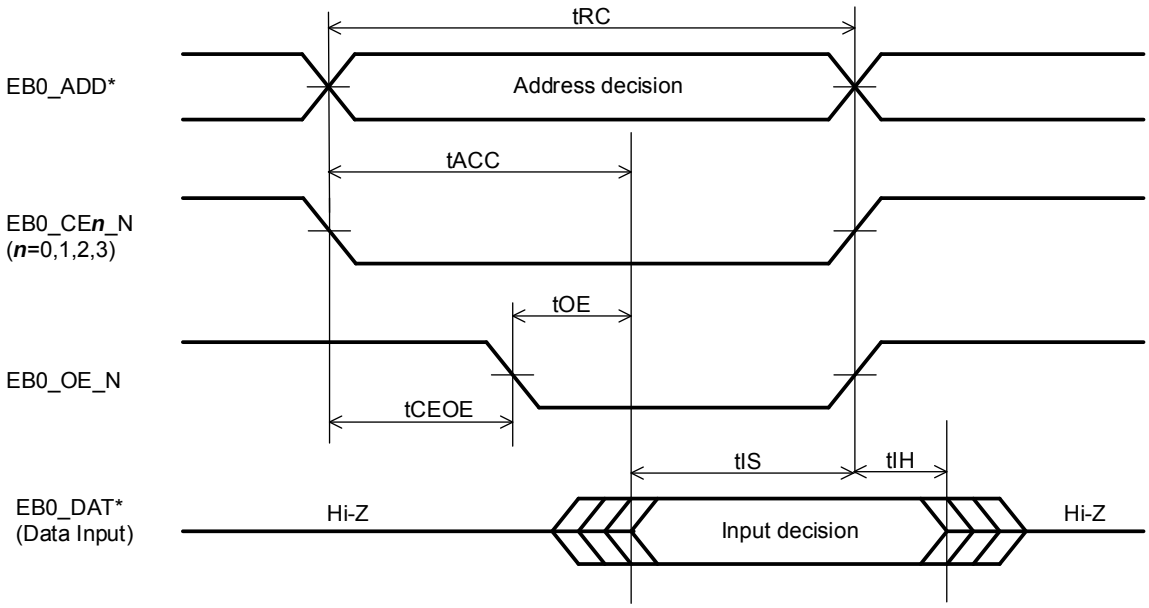
Note 2: The clock cycle time can be set to 40 ns (default value), 20 ns or 10 ns.

Note 3: Rising Transition Time (20% - 80%)

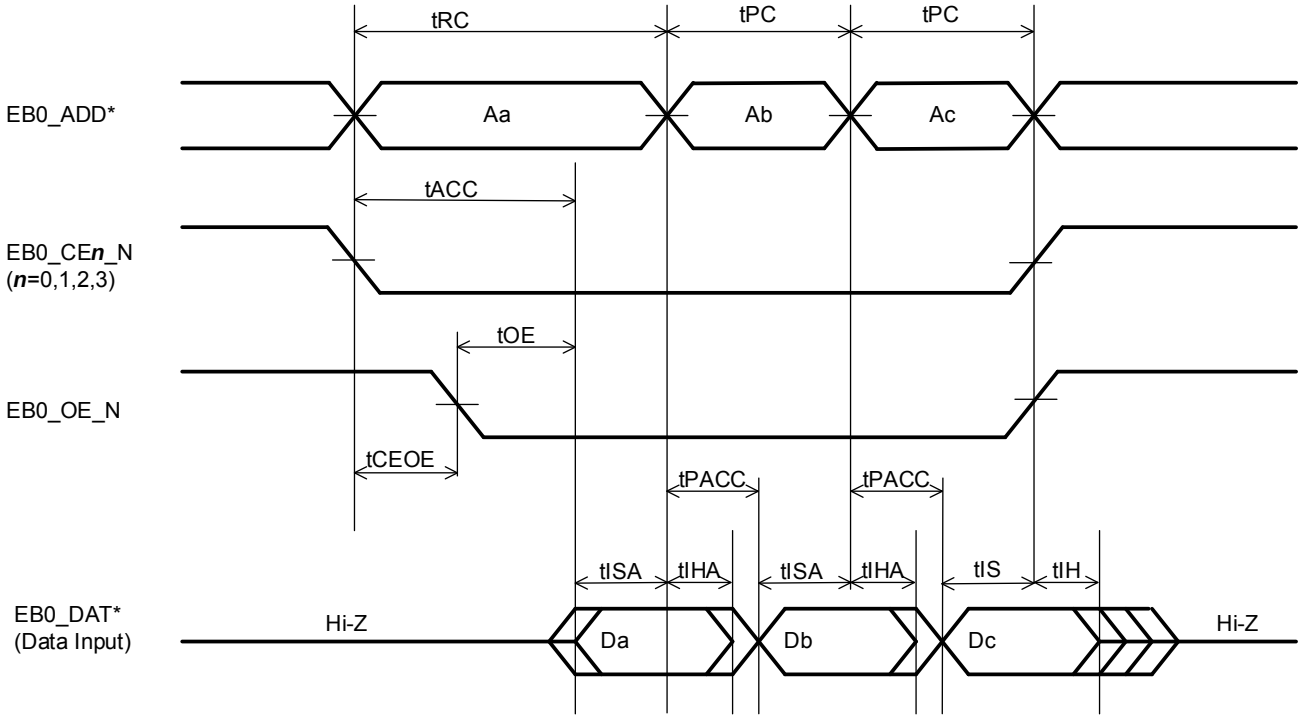
$$\text{Transition Time} = \begin{cases} 1.0\ (\max) \\ 0\ (\min) \end{cases} [\mathrm{ns}]$$

Read cycle

Read



Page read



Item	Symbol	Conditions	Min	Typ.	Max	Unit
Clock Cycle Time	tINTERCLK	(Note 2)	10	—	40	ns
Read Cycle Time	tRC	(Note 1)	TRC * tINTERCLK - 15	—	—	ns
Address Access Time	tACC	(Note 1) (Note 3) (Note 4)	—	—	TRC * tINTERCLK -25	ns
Period from EB0_CE_N(fall) to EB0_OE_N(fall)	tCEOE	(Note 1)	TCEOE * tINTERCLK - 15	—	—	ns
Period from EB0_OE_N(fall) to Data Input	tOE	(Note 1) (Note 3)	—	—	(TRC – TCEOE)* tINTERCLK -25	ns
Data Input Setup Time for Last Data	tIS	(Note 1) (Note 3) (Note 5)	25	—	—	ns
Data Input Hold Time for Last Data	tIH	(Note 1) (Note 3) (Note 6)	0	—	—	ns
Data Input Setup Time	tISA	(Note 1) (Note 3) (Note 7)	25	—	—	ns
Data Input Hold Time	tIHA	(Note 1) (Note 3) (Note 8)	0	—	—	ns
Page Cycle Time	tPC	(Note 1)	TPC * tINTERCLK - 15	—	—	ns
Page Access Time	tPACC	(Note 1) (Note 3)	—	—	TPC * tINTERCLK - 25	ns

TRC, TCEOE, TPC mean setting values of each register field ***[EBIFx_CYCLESn]***.TRC, ***[EBIFx_CYCLESn]***.TCEOE, ***[EBIFx_CYCLESn]***.TPC.

Note 1: External load capacity (C_L)

$$C_L = \begin{cases} 40\ (\max) \\ 6\ (\min) \end{cases} [\mathrm{pF}]$$

Note 2: The clock cycle time can be set to 40 ns (default value), 20 ns or 10 ns.

Note 3: Rising Transition Time (20% - 80%)

$$\text{Transition Time} = \begin{cases} 1.0\ (\max) \\ 0\ (\min) \end{cases} [\mathrm{ns}]$$

Note 4: The starting point is the latest changing of the timing in falling CE and changing ADD.

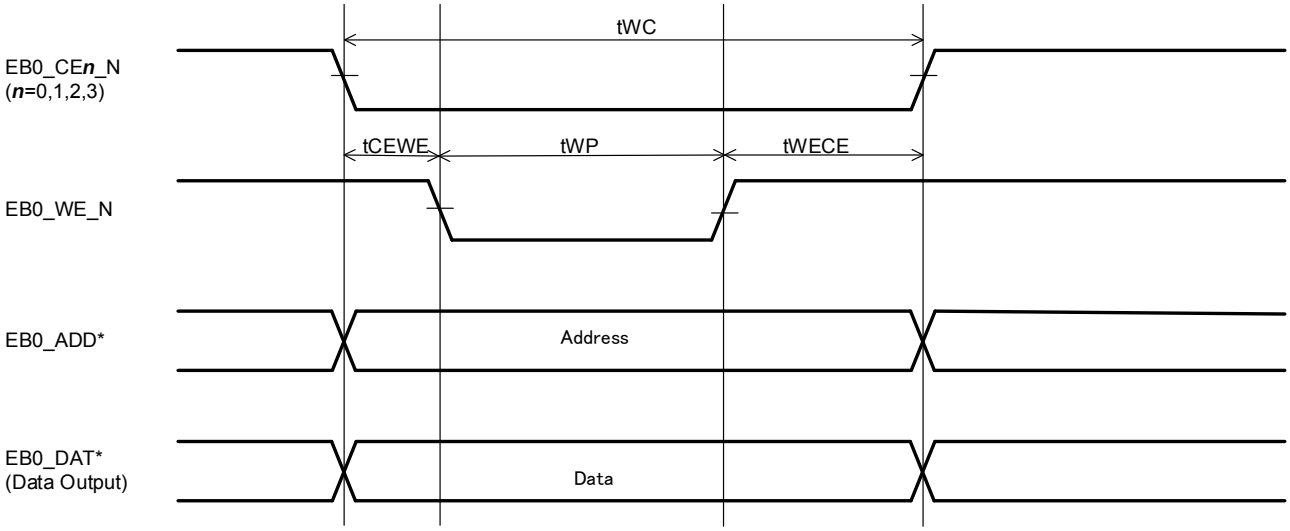
Note 5: The starting point is the latest changing of the timing in rising CE, rising OE and changing ADD.

Note 6: The starting point is the earlist changing of the timing in rising CE, rising OE and changing ADD.

Note 7: The starting point is the latest changing of the timing in changing ADD.

Note 8: The starting point is the earlist changing of the timing in changing ADD.

Write cycle



Item	Symbol	Conditions	Min	Typ.	Max	Unit
Clock Cycle Time	tINTERCLK	(Note 2)	10	—	40	ns
Write Cycle Time	tWC	(Note 1)	TWC * tINTERCLK - 15	—	—	ns
Write Pulse Width	tWP	(Note 1)	TWP * tINTERCLK - 15	—	—	ns
Period from EB0_CE_N(fall) to EB0_WE_N(fall)	tCEWE	(Note 1)	1 * tINTERCLK - 15	—	—	ns
Period from EB0_WE_N(rise) to EB0_CE_N(rise)	tWECE	(Note 1)	(TWC - TWP -1) * tINTERCLK - 15	—	—	ns

TWC, TWP mean setting values of each register field ***[EBIFx_CYCLESn]***.TWC, ***[EBIFx_CYCLESn]***.TWP.

Note 1**:** External load capacity (C_L)

$$C_L = \begin{cases} 40\ (\max) \\ 6\ (\min) \end{cases} [\mathrm{pF}]$$

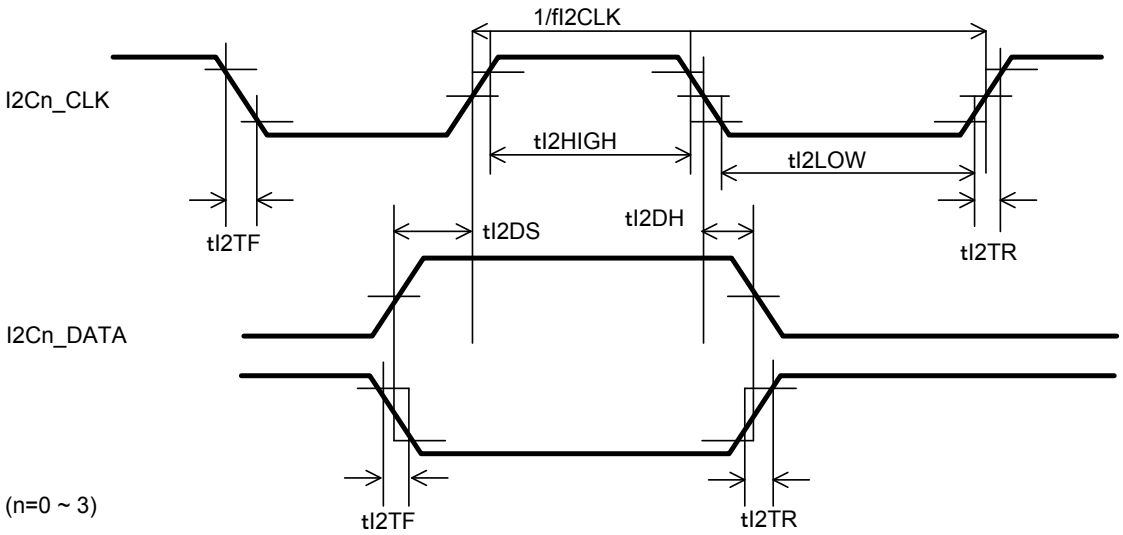
Note 2**:** The clock cycle time can be set to 40 ns (default value), 20 ns or 10 ns.

For the cycle base timing chart in external bus, refer to the timing chart of the section 5.4.3, 5.4.4 and 5.4.5 in the Chapter 27 of the reference manual External BUS interface.

These AC specifications are not included wiring delay time on the board and skew. It is needed to consider not only AC specifications of this product and connected device but also wiring delay time on the board and skew when designing the board or using the delay adjustment register (***[EBIFx_CYCLESn]***).

The setting value by register in above specification table should be needed the positive value.

4.5.6. I²C Bus Interface



Standard Speed (100 kHz)

Item	Symbol	Conditions	Min	Typ.	Max	Unit
Clock frequency	fI2CLK	—	0	—	100	kHz
LOW period of the SCL clock	tI2LOW	—	4.7	—	—	μs
HIGH period of the SCL clock	tI2HIGH	—	4.0	—	—	μs
rise time of both SDA and SCL signals	tI2TR	—	—	—	1000	ns
fall time of both SDA and SCL signals	tI2TF	—	—	—	300	ns
Input Data setup time	tI2DS	—	250	—	—	ns
Input Data hold time	tI2DH	(Note 1) (Note 2)	0	—	3.45	μs
capacitive load for each bus line	Cb	(Note 4)	—	—	400	pF

Fast Speed (400 kHz)

Item	Symbol	Conditions	Min	Typ.	Max	Unit
Clock frequency	fI2CLK	—	0	—	400	kHz
LOW period of the SCL clock	tI2LOW	—	1.3	—	—	μs
HIGH period of the SCL clock	tI2HIGH	—	0.6	—	—	μs
rise time of both SDA and SCL signals	tI2TR	(Note 4)	20 + 0.1Cb	—	300	ns
fall time of both SDA and SCL signals	tI2TF	(Note 4)	20 + 0.1Cb	—	300	ns
Input Data setup time	tI2DS	(Note 3)	100	—	—	ns
Input Data hold time	tI2DH	(Note 1) (Note 2)	0	—	0.9	μs
capacitive load for each bus line	Cb	(Note 4)	—	—	400	pF

Fast mode Plus Speed (1 MHz)

Item	Symbol	Conditions	Min	Typ.	Max	Unit
Clock frequency	fI2CLK	—	0	—	1000	kHz
LOW period of the SCL clock	tI2LOW	—	0.5	—	—	μs
HIGH period of the SCL clock	tI2HIGH	—	0.26	—	—	μs
rise time of both SDA and SCL signals	tI2TR	—	—	—	120	ns
fall time of both SDA and SCL signals	tI2TF	—	—	—	120	ns
Input Data setup time	tI2DS	—	50	—	—	ns
Input Data hold time	tI2DH	(Note 1) (Note 2)	0	—	—	μs
capacitive load for each bus line	Cb	(Note 4)	—	—	550	pF

Note 1: The I^2C interface should have the minimum hold time of 300 ns internally (from the VIH min point of SCL signal) in order to prevent from instability at the falling edge of SCL.

Note 2: The max value of tI2DH is valid as long as the low period of SCL (tLow) is not extended.

Note 3: Fast Speed mode of I^2C interface can be used in Standard Speed mode, if the condition of tI2DS ≥ 250 ns is satisfied. This means the interface does not extend the low period of the SCL. In this case the next data should be output to SDA before the following time;

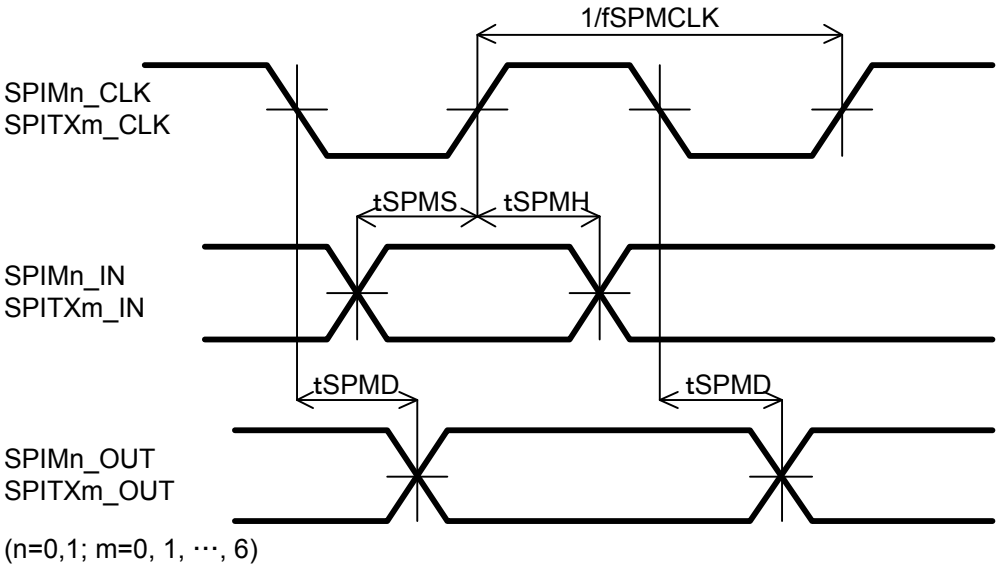
tI2TR(Max) + tI2DS = 1000 + 250 = 1250 ns

(maximum rise time of Standard Speed mode + the setup time of the next data)

Note 4: Cb is a total capacitance of one bus line (unit: pF).

4.5.7. SPI Interface (for Master Controller and Transmission)

SPIM0 and SPIM1 for master controller, SPITX0 to SPITX6 for dedicated transmission.



Item	Symbol	Conditions	Min	Typ.	Max	Unit
Clock frequency	fSPMCLK	(Note 1)	—	—	25	MHz
Output Data delay time	tSPMD	(Note 1)	0.5	—	10	ns
Input Data setup time	tSPMS	(Note 2)	8	—	—	ns
Input Data hold time	tSPMH	(Note 2)	0	—	—	ns

Note 1: External load capacity (C_L)

$$C_L = \begin{cases} 30\ (\max) \\ 0\ (\min) \end{cases} [\mathrm{pF}]$$

Note 2: Transition Time (20% - 80%)

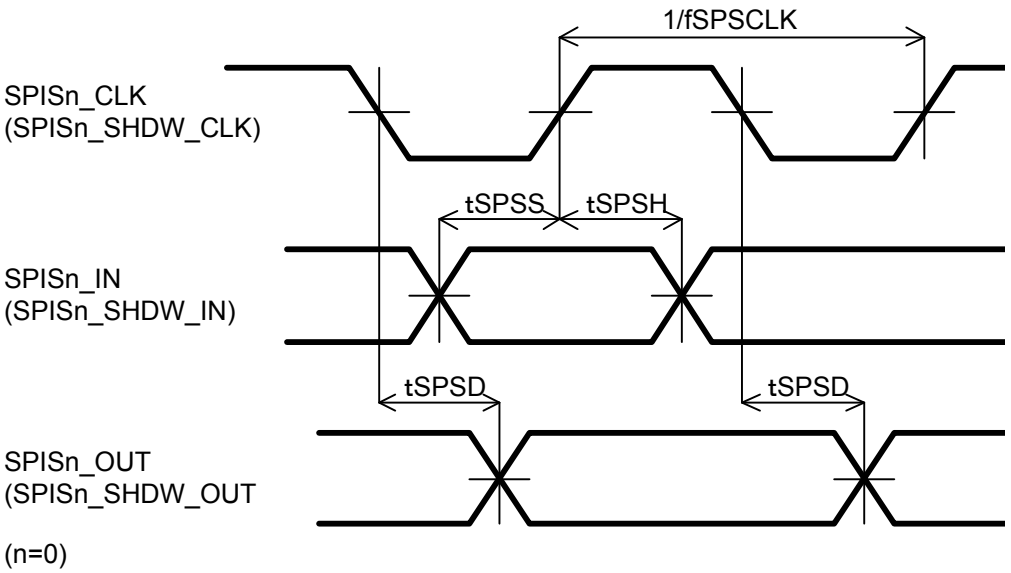
$$\text{Transition Time} = \begin{cases} 1.0\ (\max) \\ 0\ (\min) \end{cases} [\mathrm{ns}]$$

The maximum value of fSPMCLK may be reduced by the load on board layout, and an external device.

The above timing chart is in case of SCPH = 0. In case of SCPH = 1, the signal of SPIMn_Out synchronizes to the rising edge of SPIMn_CLK, the specification of tSPMD is same as the value in case of SCPH = 0.

There is no specifications about SPITXm (m = 0, 1, … , 6) input signals.

4.5.8. SPI Interface (for Slave Controller)



Item	Symbol	Conditions	Min	Typ.	Max	Unit
Clock frequency	fSPSCLK	—	—	—	5	MHz
Output Data delay time	tSPSD	(Note 1)	0.5	—	50	ns
Input Data setup time	tSPSS	(Note 2)	40	—	—	ns
Input Data hold time	tSPSH	(Note 2)	25	—	—	ns

Note 1: External load capacity (C_L)

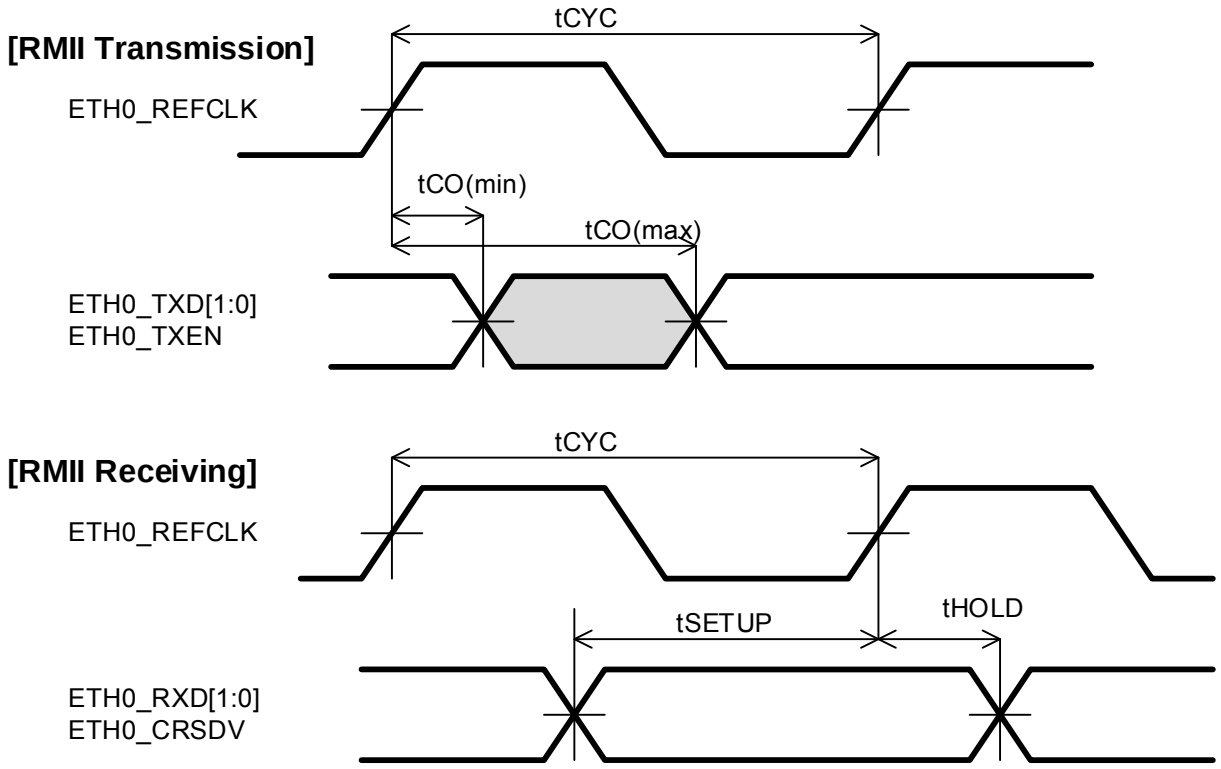
$$C_L = \begin{cases} 30\ (\max) \\ 0\ (\min) \end{cases} [\mathrm{pF}]$$

Note 2: Transition Time (20% - 80%)

$$\text{Transition Time} = \begin{cases} 1.0\ (\max) \\ 0\ (\min) \end{cases} [\mathrm{ns}]$$

The above timing chart is in case of SCPH = 0. In case of SCPH = 1, the signal of SPISn_Out (SPISn_SHDW_Out) synchronizes to the rising edge of SPISn_CLK (SPISn_SHDW_CLK), the specification of tSPSD is same as the value in case of SCPH = 0.

4.5.9. Ethernet MAC interface



Item	Symbol	Conditions	Min	Typ.	Max	Unit
ETH_REFCLK clock cycle time	tCYC	(Note 2)	—	20	—	ns
ETH_TXD1 to 0/ETH_TXEN output delay time	tCO	(Note 1)	2	—	12.5	ns
ETH_RXD1 to 0/ETH_CRSDV setup time	tSETUP	(Note 2)	4	—	—	ns
ETH_RXD1 to 0/ETH_CRSDV hold time	tHOLD	(Note 2)	2	—	—	ns

Note 1: External load capacity (C_L)

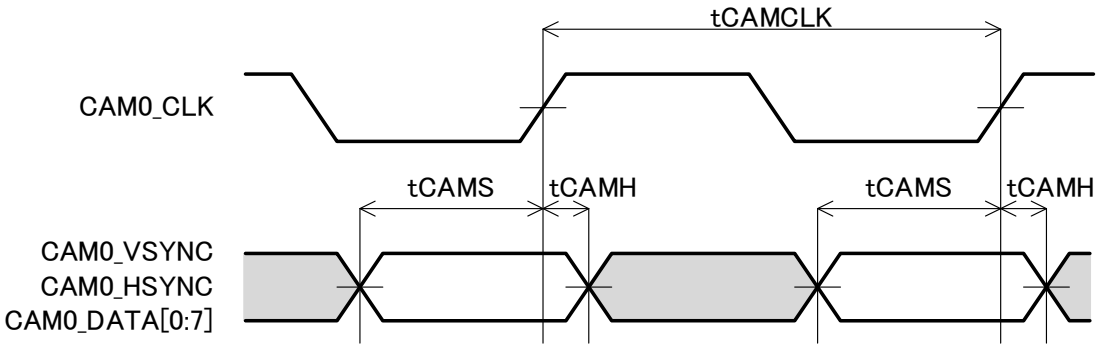
$$C_L = \begin{cases} 25\ (\max) \\ 0\ (\min) \end{cases} [\mathrm{pF}]$$

Note 2: Skew against reference clock of PHY device must be 0.5 ns or less.

Transition Time (20% - 80%)

$$\text{Transition Time} = \begin{cases} 1.0\ (\max) \\ 0\ (\min) \end{cases} [\mathrm{ns}]$$

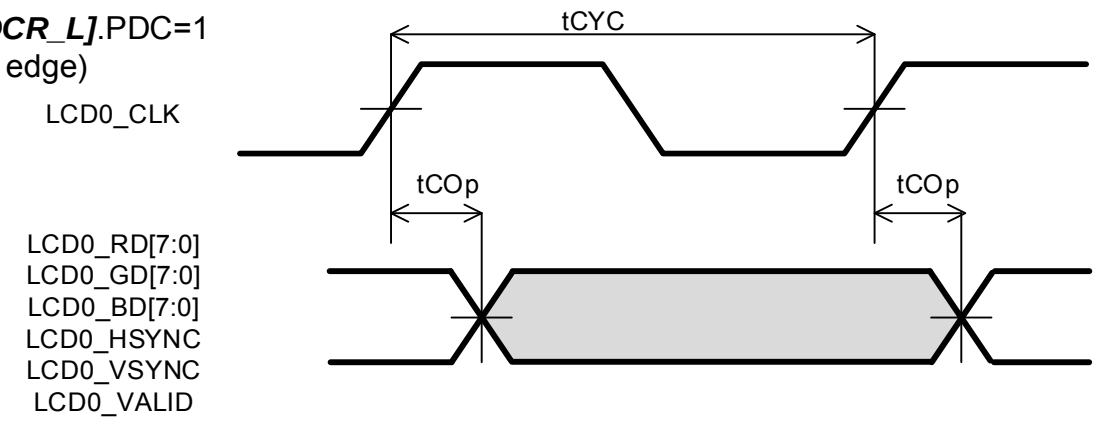
4.5.10. Camera Input



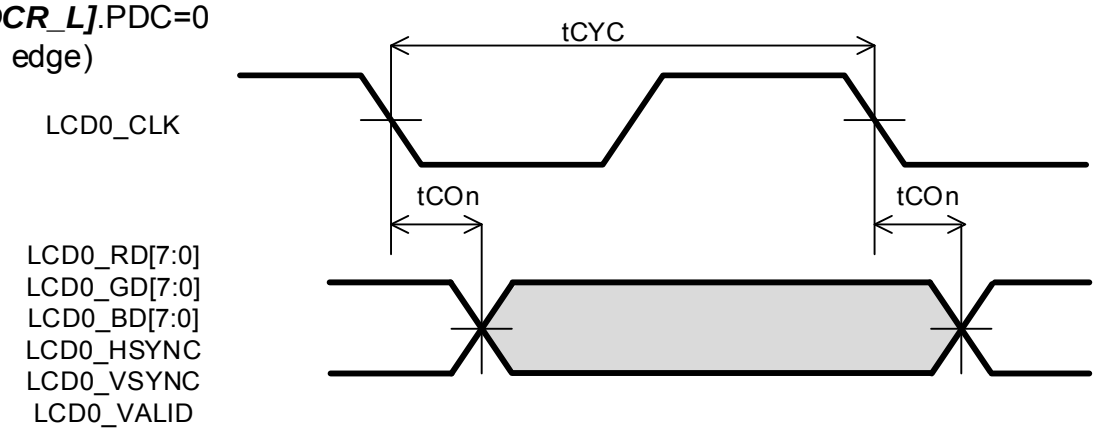
Item	Symbol	Conditions	Min	Typ.	Max	Unit
CAM0_CLK clock cycle time	tCAMCLK	—	10	—	—	ns
CAM0_VSYNC/CAM0_HSYNC/ CAM0_DATA[7:0] setup time	tCAMS	—	4	—	—	ns
CAM0_VSYNC/CAM0_HSYNC/ CAM0_DATA[7:0] hold time	tCAMH	—	1	—	—	ns

4.5.11. LCD Output

[GDCDCR_L].PDC=1
(Rising edge)



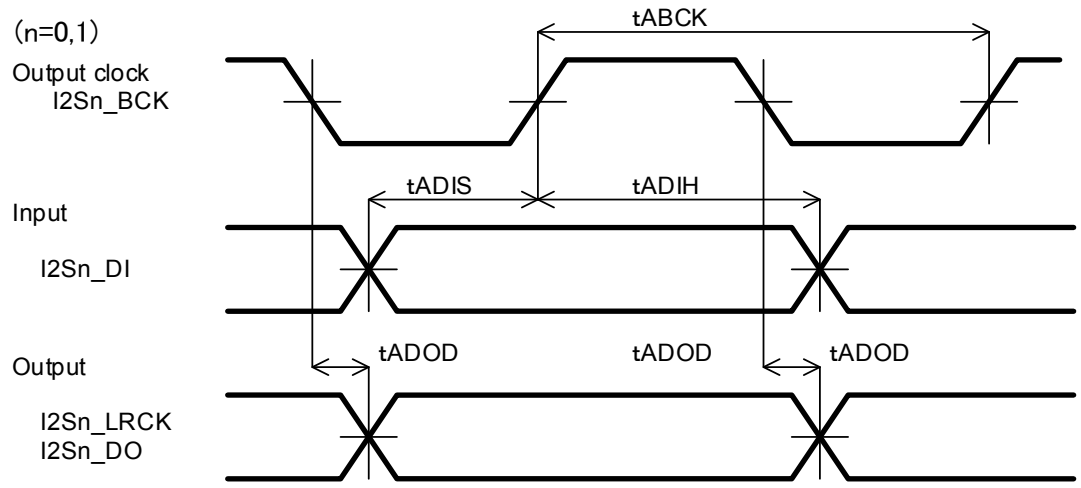
[GDCDCR_L].PDC=0
(Falling edge)



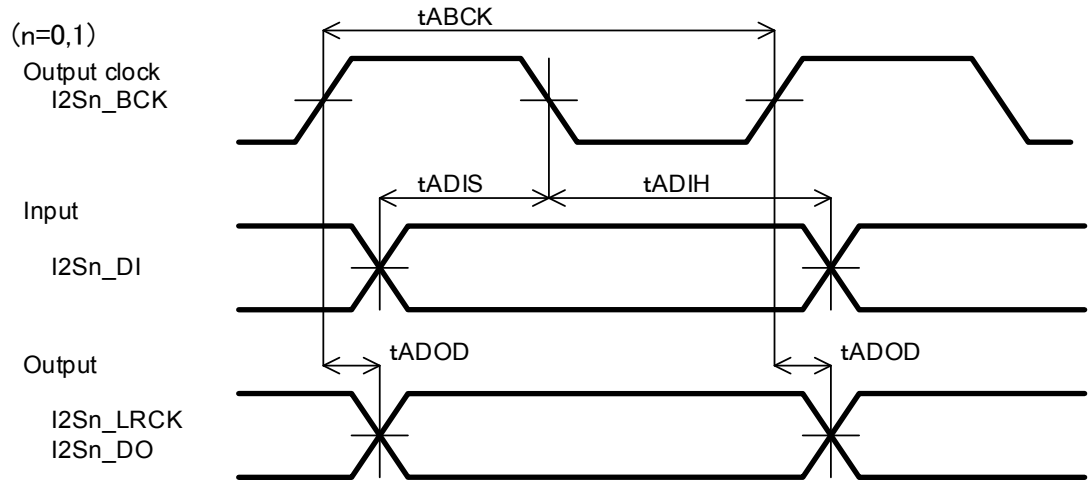
Item	Symbol	Conditions	Min	Typ.	Max	Unit
clock cycle time	tCYC	—	23	—	—	ns
output delay time	tCOp	***[GDCDCR_L]***.PDC = 1 (Rising edge)	0	—	5	ns
	tCOn	***[GDCDCR_L]***.PDC = 0 (Falling edge)	0	—	5	ns

4.5.12. Audio Interface

Bit clock output (1): Falling edge data output, Rising edge input data sampling



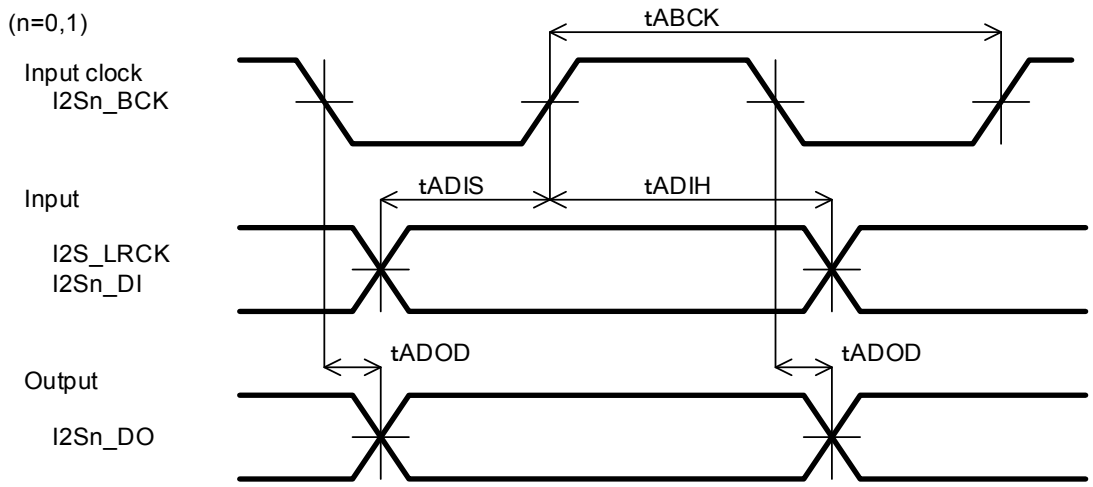
Bit clock output (2)：Rising edge date output、Falling edge input data sampling



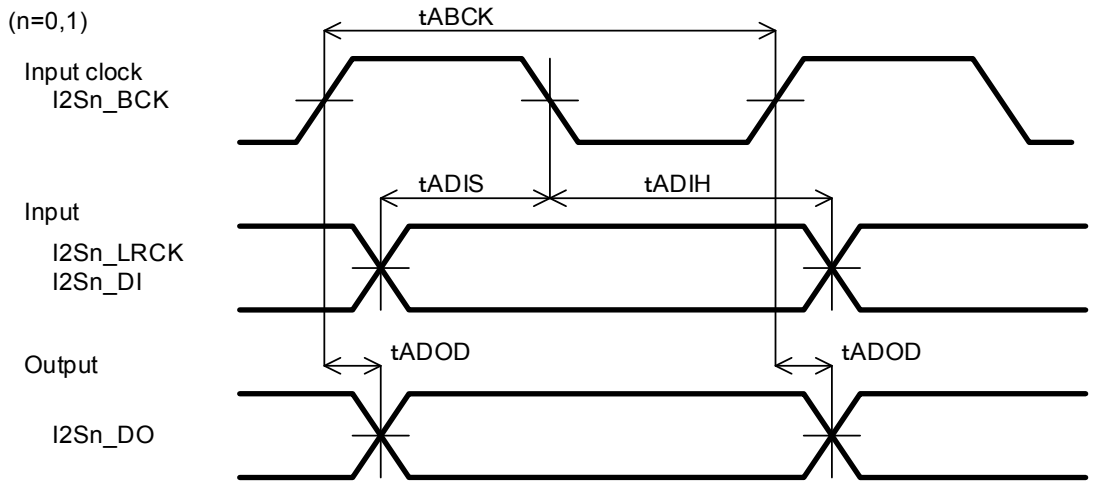
Item	Symbol	Conditions	Min	Typ.	Max	Unit
I2S Output Clock Period	tABCK	—	81.38 (Note 1)	—	—	ns
I2S Input Data Setup Time	tADIS	—	10	—	—	ns
I2S Input Data Hold Time	tADIH	—	10	—	—	ns
I2S Output Delay Time	tADOD	—	0	—	10	ns

Note 1: Max 12.288 MHz

Bit clock input (1): Falling edge data output, Rising edge input data sampling



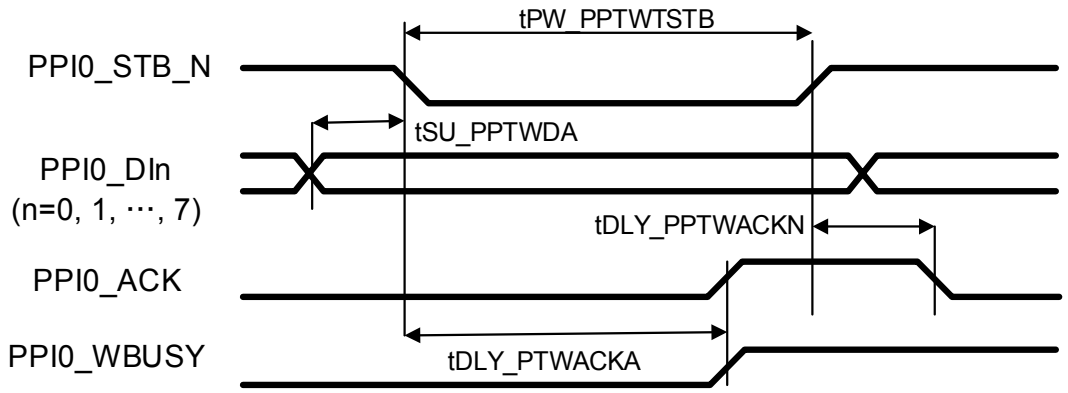
Bit clock input (2): Rising edge data output, Falling edge input data sampling



Item	Symbol	Conditions	Min	Typ.	Max	Unit
I2S Input Clock Period	tABCK	—	81.38 (Note 1)	—	—	ns
I2S Input Data Setup Time	tADIS	—	10	—	—	ns
I2S Input Data Hold Time	tADIH	—	10	—	—	ns
I2S Output Delay Time	tADOD	—	0	—	10	ns

Note 1: Max 12.288 MHz

4.5.13. Parallel Data Input



Item	Symbol	Conditions	Min	Typ.	Max	Unit
Strobe Pulse Width	tPW_PPTWSTB	(Note 1)	50	—	—	ns
Write Data Setup Time	tSU_PPTWDA	(Note 1)	30	—	—	ns
Output Delay of Asserting Acknowledge and Write-Busy Signals	tDLY_PTWACKA	(Note 2)	—	—	70	ns
Output Delay of De-asserting Acknowledge Signal	tDLY_PPTWACKN	(Note 2)	—	—	70	ns

Note 1: Transition Time (20% - 80%)

$$\text{Transition Time} = \begin{cases} 1.0\ (\text{max}) \\ 0\ (\text{min}) \end{cases} [\text{ns}]$$

Note 2: External load capacity (C_L)

$$C_L = \begin{cases} 30\ (\text{max}) \\ 0\ (\text{min}) \end{cases} [\text{pF}]$$

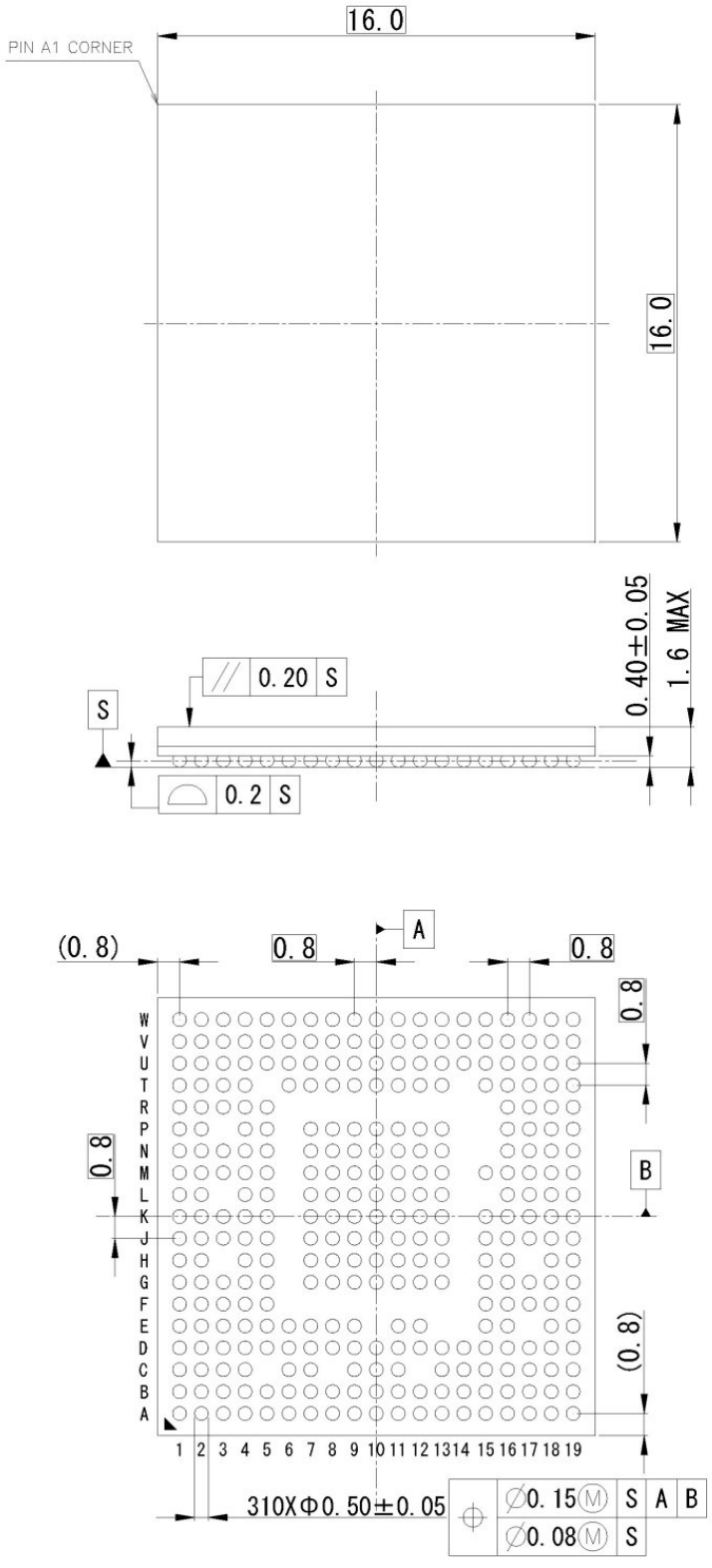
4.5.14. AD Conversion Input

Item	Symbol	Conditions	Min	Typ.	Max	Unit
Sampling Frequency	fs	Input on 1 channel	—	—	1.07	MHz
Analog Input Voltage Range	V_{IN}	—	0	—	VDD3V3_ADC	V
ADC Differential Error	DNL	There is no AC noise in the power supply and the GND.	-2	—	+4	LSB
ADC Integrated Error	INL		-6	—	+6	LSB

5. Package

5.1. Package outline

Package name: P-LFBGA310-1616-0.80-001 **Unit: mm**



Weight: 0.75 g (Typ.)

Figure 5.1 Package Outline

6. Revision history

Table 6.1 Revision History

Revision	Date	Description
0.1	2015-03-11	Initial release in English version
1.0	2015-07-15	Official version 3.3 Added the explanation of attribute, instead of the table 3.3.2 Added the notice 3.3.19 Added the notice 3.3.22 Deleted P7 of column 3.4.1 Added the note of pin-type in Table 3.2 4.2 Added Operating Conditions 4.3 Added Current dissipations 4.4 Added DC characteristics 4.5 Added AC characteristics
1.1	2015-10-02	3.3.22 Correct IDX16 column
1.2	2015-11-30	Modify C_F to CL symbol
1.3	2016-01-05	Modified Figure 2.1. Changed RTC clock frequency to 32.768 kHz in 3.3.1. Added note description in Table 3.2.
1.4	2016-01-14	Modified 3.3.1 XOUT_32K to In/Out.
1.5	2016-05-30	Changed description from SPI interface to SPI Flash Memory Controller Interface. Changed note description in 1.1.CPU Note 1. Changed description in 1.7.(1) Added 1.7.(3) WVGA resolution (800 × 480) Changed description of 3.3.1.DBG_SRST_N. Changed title name 3.3.17 and 4.5.13. Modified from CL to C_L and Note description in 4.5 (4.5.5.1, 4.5.5.2, 4.5.7, 4.5.8, 4.5.9, 4.5.13). Changed description in 1.11.(2) Added IDX6 DBG_SRST_N in 3.3.20.JTAG interface for debugging. Modified description in 3.4.1. Added SPI_CLK Clock Frequency minimum specification 18.75 MHz in 4.5.3. Added Note description in 3.3.11. Added Fast mode Plus Speed (1 MHz) specification. Changed VDD3V3_PB minimum value and added Note description in 4.2.1 and 4.2.2, 4.2.3.
1.6	2016-07-19	Added products (ADD codes) and Operating Temperature, Internal Voltage Range, USB 2.0 Function in List of Products. Added etc. in 1.1.CPU Operation frequency. Delete Note in 3.3.20. JTAG interface for debugging. Modified description in 3.4.1. Changed 4.2.2 title name (TZ2101XBG/TZ2102XBG→TZ2102XBG). Modified Conditions of “High-level output voltage” in 4.4.1. Modified Unit of “Strobe Pulse Width” in 4.5.13.
1.7	2017-05-16	Modified some words in 1.1. CPU. Deleted secure boot descriptions in cover page and section 1.2, 2. Added a word in 3.3.20. IDX 6 description. Added timing charts, tables, notes, descriptions in 4.5.5.2.
1.8	2017-08-07	Changed header, footer and the last page. Changed corporate name and descriptions.

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