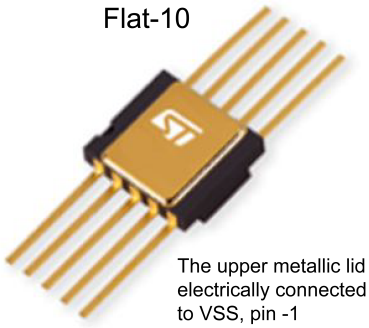
RH-OSC04

Datasheet

Rad-hard, 4-stage ripple-carry binary counter/divider

Flat-10



The upper metallic lid is electrically connected to VSS, pin -1

Features

- 2.3 V to 3.6 V supply (4.8 V AMR)
- High speed:
  - Characterized from 16 MHz to 120 MHz
- CMOS output, meets JEDEC
- Divided-frequency single output
- Low power
- TTL compatible
- Enable/disable function
- Targeted immunity to radiations:
  - 300 krad(Si) TID
  - 120 MeV.cm²/mg SEL free

Applications

- Oscillators for space systems

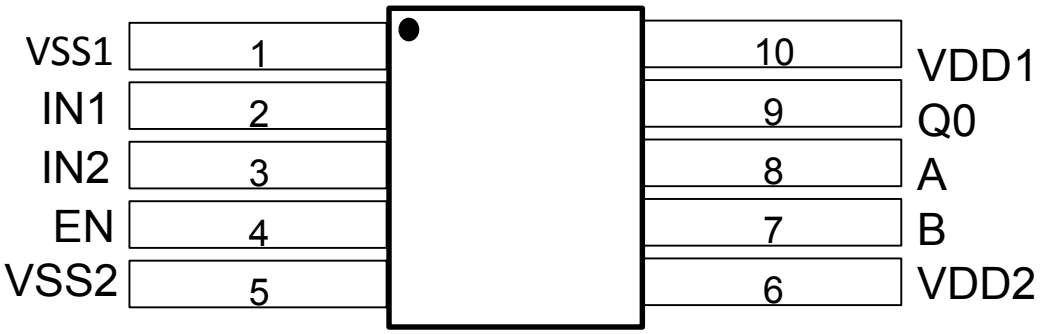
Description

The RH-OSC04 consists of an oscillator section and 4-stage ripple-carry binary counter. The oscillator section allows the implementation of crystal oscillator circuits. The output is buffered and it is controlled by a 2-bit digital cell to deliver one among four divided frequency, from F to F/2, F/4 and F/8 frequencies. A disable function is available to set the circuit in power-down mode while keeping a high impedance output. It comes in hermetic ceramic Flat 10-lead, and can operate from -55 °C to +125 °C ambient temperature.

Product status link
RH-OSC04

1 General overview

Figure 1. **Pin connection**



VDD1 and VDD2 are internally connected to the die and must be externally connected to the same voltage.
VSS1 and VSS2 are internally connected to the die and must be externally connected to the same voltage.

Figure 2. **Schematic**

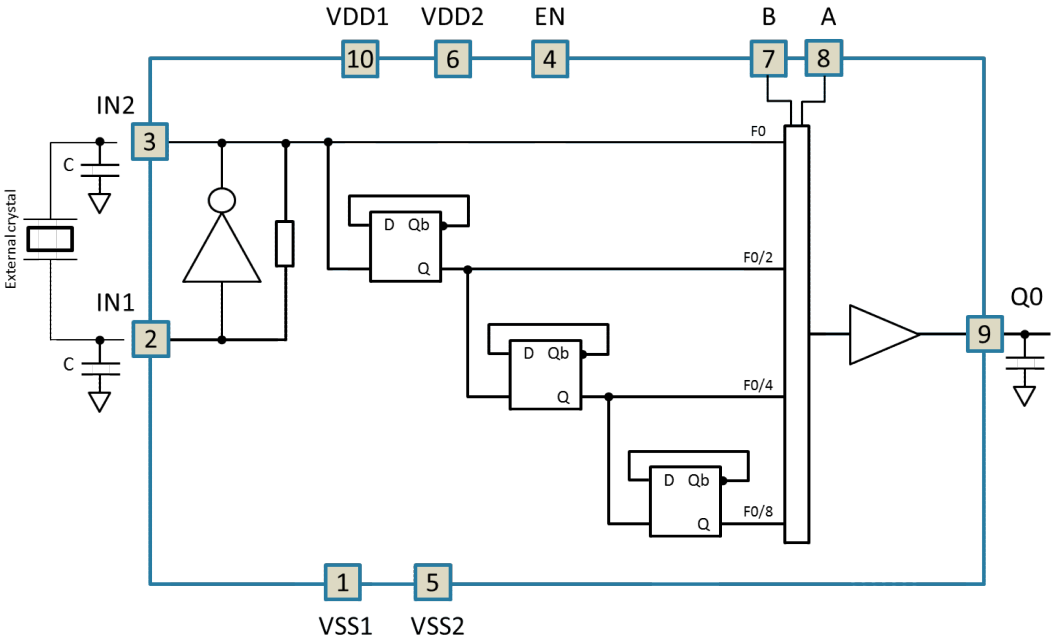


Table 1. **Truth table**

B	A	EN	Q0
0	0	1	F0
0	1	1	F0/2
1	0	1	F0/4
1	1	1	F0/8
X	X	0	High impedance

2 Maximum ratings and operating conditions

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 2. Absolute maximum ratings

Symbol	Parameters	Value	Units
VDD(1)	Maximum power supply between VDD and VSS	4.8	V
T_{stg}	Maximum temperature storage	-65 to +150	°C
T_j	Maximum junction temperature	+150	°C
R_{thjc}	Junction-to-case thermal resistance (Flat-10 package)(2)	22	°C/W
R_{thja}	Junction-to-ambient thermal resistance (Flat-10 package) (2)	125	°C/W
Vi	Max. voltage on any pin	-0.3 V to VDD+0.3 V	V
Ii	Max. input current at any pin	±10	mA
ESD	HBM on all pins (human body model)	2 k	V
	CDM on all pins (charged device model)	1 k	V

1. *All voltages are with respect to the network ground terminal .*
2. *Short-circuits can cause excessive heating. Destructive dissipation can result from short-circuits on outputs.*

Table 3. Operating conditions

Symbol	Parameters	Min.	Max.	Units
VDD	Supply voltage (VDD1 and VDD2 must be connected to the same voltage)	2.3	3.6	V
VIN	Input voltage IN1 and IN2	0	VDD	V
	A, B and EN inputs	0	VDD	
T_A	Ambient temperature range	-55	+125	°C

3 Electrical characteristics

VDD = +3.3 V, VSS = GND, enabled (EN=VDD), T_{amb} = -55 °C to +125 °C, unless otherwise specified.

Table 4. DC electrical characteristics

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Unit
I_{DD}	Quiescent current	IN1 and IN2 floating I_{out} = 0 (no load)		3.4	3.8	mA
I_Z	Quiescent current in disable	EN = 0 V			300	nA
I_{outZ}	Output current in disable on Q0	EN = 0 V		7	30	nA
V_{OL}	Low level output voltage on Q0	IOL = +100 µA, VDD = 2.3 V			200	mV
		IOL = +100 µA, VDD = 3.6 V			200	mV
V_{OH}	High level output voltage on Q0	IO L= +100 µA, VDD = 2.3 V	2.1			V
		IOL = +100 µA, VDD = 3.6 V	2.8			V
V_{IL}	Low level input voltage on A, B, EN inputs	VDD = 2.3 V			0.8	V
		VDD = 3.6 V			0.8	V
V_{IH}	High level input voltage on A, B, EN inputs	VDD = 2.3 V	2			V
		VDD = 3.6 V	2			V
I_{IL}	Input leakage current low on A, B, EN inputs	V_{in} = 0 V VDD= 2.3 V to 3.6 V			-0.1	µA
I_{IH}	Input leakage current high on A, B, EN inputs	V_{in} = VDD VDD = 2.3 V to 3.6 V			0.1	µA
I_{sink}	Short-circuit output current	V_{out} = VDD VDD = 2.3 V to 3.6 V		50	80	mA
I_{source}	Short-circuit output current	V_{out} = 0 V VDD = 2.3 V to 3.6 V	-80	-50		mA

VDD = +3.3 V, VSS = GND, C-load = 18 pF (see figure 3), enabled (EN = VDD), Tamb = -55 °C to +125 °C, unless otherwise specified.

Table 5. AC electrical characteristics

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Unit
T_r	Output rise time	90%/10%, CL = 18 pF		2.2		ns
		90%/10%, CL = 2 pF		0.4		
T_f	Output fall time	90%/10%, CL = 18 pF		2.2		
		90%/10%, CL = 2 pF		0.4		
PhN	Phase noise on Q0	at 250 Hz Fclk = 16 MHz		-110		dBc /Hz
		at 170 Hz F_{clk} = 120 MHz		-100		
J_t	RMS Jitter	At 1 MHz F_{clk} = 16 MHz		4		ps
DL1	Drive level	Crystal using H1, F_{clk} = 16 MHz to 25 MHz			100	µW
DL3		Crystal using H3, F_{clk} = 25 MHz to 120 MHz			200	
D_{tc}	Duty- cycle on Q0	F_{clk} = 16 MHz	45	50	55	%

Figure 3. Phase noise, F_{clk} = 120 MHz, V_{cc} = 3.3 V

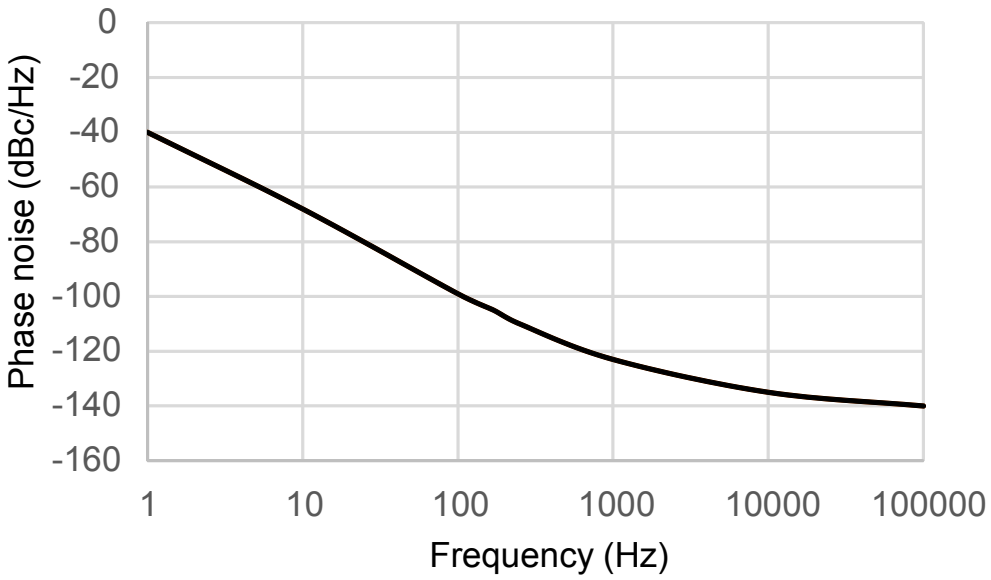


Figure 4. **Phase noise, F_{clk} = 60 MHz, V_{cc} = 3.3 V**

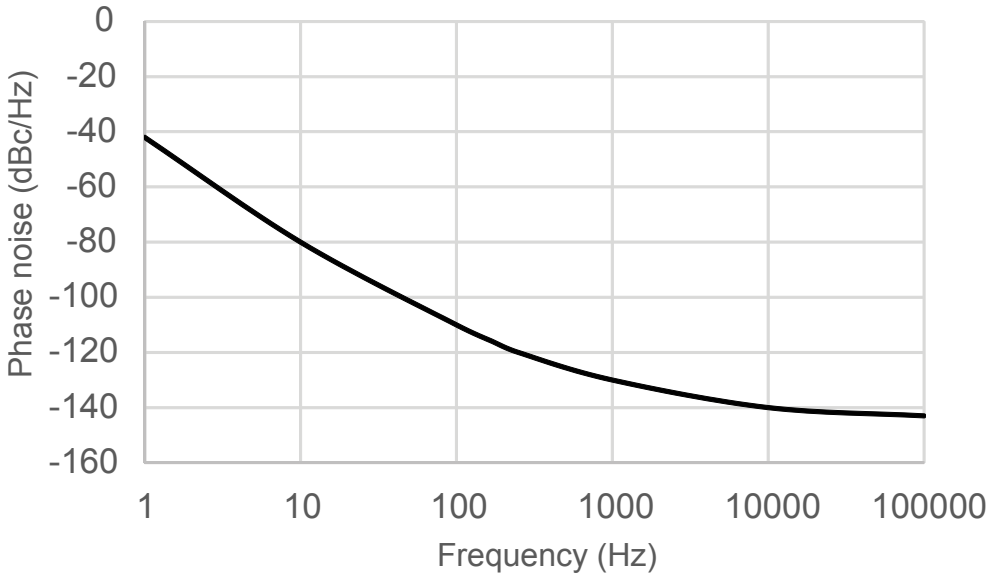


Figure 5. **Phase noise, F_{clk} = 16 MHz, V_{cc} = 3.3 V**

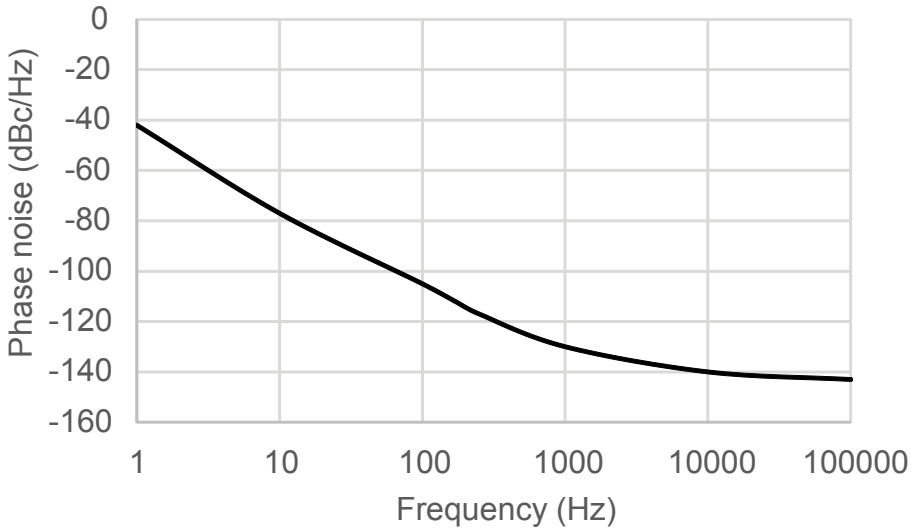
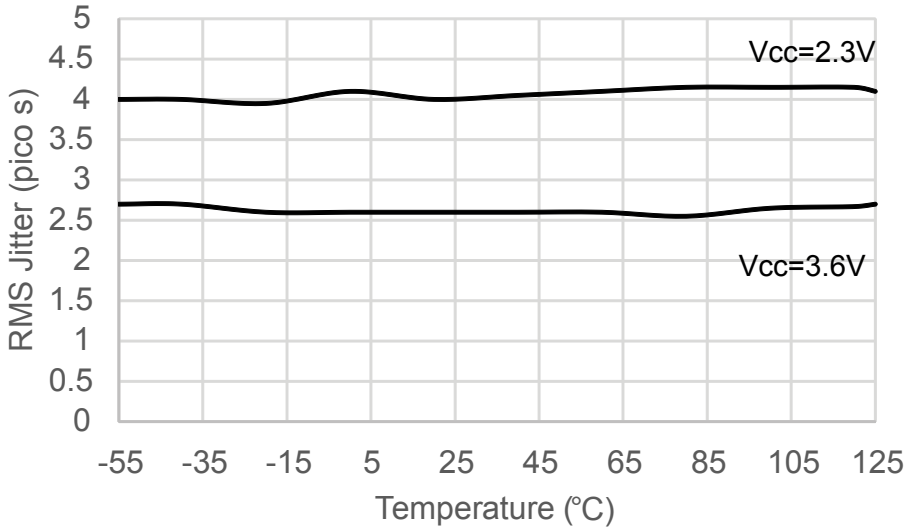


Figure 6. **RMS jitter, F_{clk} = 16 MHz**



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 Flat-10 package information

Figure 7. Flat-10 package outline

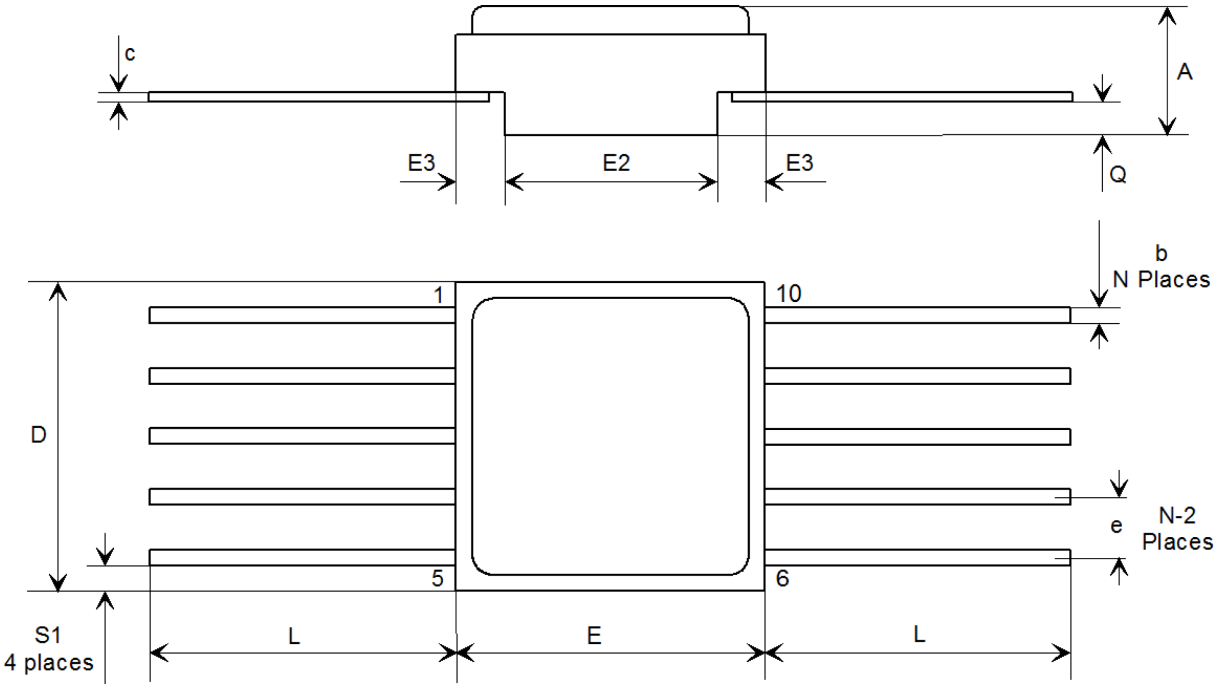


Table 6. Flat-10 mechanical data

Symbol	mm			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.26	2.44	2.62	.089	.096	.103
b	0.38	0.43	0.48	.015	.017	.019
c	0.102	0.127	0.152	.004	.005	.006
D	6.35	6.48	6.60	.250	.255	.260
E	6.35	6.48	6.60	.250	.255	.260
E2	4.32	4.45	4.58	.170	.175	.180
E3	0.88	1.01	1.14	.035	.040	.045
e		1.27			.050	
L	6.35		9.40	.250		.370
Q	0.66	0.79	0.92	.026	.031	.036
S1	0.16	0.485	0.81	.006	.019	.032
N		10			10	

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*

5 Ordering information

Order code	SMD [1]	Qualification level	Mass	Package	Lead finish	Marking [2]	Packing
RH-OSC04K1	-	Engineering model	0.42 g	Flat-10	Gold	RH-OSC04K1	Conductive strip pack

1. *Standard microcircuit drawing*
2. *Specific marking only. Complete marking includes the following:*
   - *ST logo*
   - *Date code (date the package was sealed) in YYWWA (year, week, and lot index of week)*
   - *Country of origin (FR = France)*

6 Other information

6.1 Date code

The date code (date the package was sealed) is structured as follows:

- Engineering model: 3yywwz
- Flight model: yywwz

Where:

yy = last two digits of the year, ww = week digits, z = lot index of the week

6.1.1 Date code

The date code (date the package was sealed) is structured as follows:

- Engineering model: 3yywwz
- Flight model: yywwz

Where:

yy = last two digits of the year, ww = week digits, z = lot index of the week

6.1.2 Product documentation

Each product shipment includes a set of associated documentation within the shipment box. This documentation depends on the quality level of the products, as detailed in the table below.

The certificate of conformance is provided on paper whatever the quality level. For QML parts, complete documentation, including the certificate of conformance, is provided on a CDROM.

Table 7. Product documentation

Quality level	Item
Engineering model	Certificate of conformance including : • Customer name • Customer purchase order number • ST sales order number and item • ST part number • Quantity delivered • Date code • Reference to ST datasheet • Reference to TN1181 on engineering models • ST Rennes assembly lot ID

Quality level	Item
QML-V Flight	Certificate of Conformance including: • Customer name • Customer purchase order number • ST sales order number and item • ST part number • Quantity delivered • Date code • Serial numbers • Group C reference • Group D reference • Reference to applicable SMD • ST Rennes assembly lot ID
	Quality control inspection (groups A, B, C, D, E)
	Screening electrical data in/out summary
	Precap report
	PIND (particle impact noise detection) test
	SEM (scanning electronic microscope) inspection report
	X-ray plates

Revision history

Table 8. **Document revision history**

Date	Version	Changes
19-Jul-2019	1	Initial release.

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