

## Main features

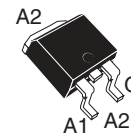
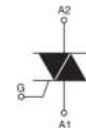
Symbol	Value	Unit
$I_{T(RMS)}$	16	A
$V_{DRM}/V_{RRM}$	600	V
$I_{GT(Q1)}$	35	mA

## Description

Specifically designed to operate at 150° C, the new 16 A CIQ1680D Triacs provide an enhanced performance in terms of power loss and thermal dissipation. This facilitates the optimization of heatsink dimensioning, leading to improved space and cost effectiveness when compared to electro-mechanical solutions.

The CIQ1680D series facilitates the optimization of the control of universal motors and inductive loads found in appliances such as vacuum cleaners, and washing machines.

The CIQ1680D Triacs are also suitable for use in high temperature environment found in hot appliances such as cookers, ovens, hobs, electric heaters, and coffee machines.



**D<sup>2</sup>PAK**

# 1 Characteristics

**Table 1. Absolute maximum ratings**

Symbol	Parameter			Value	Unit
$I_{T(RMS)}$	RMS on-state current (full sine wave)	D <sup>2</sup> PAK	$T_c = 130^\circ\text{C}$	16	A
$I_{TSM}$	Non repetitive surge peak on-state current (full cycle sine wave, $T_j$ initial = $25^\circ\text{C}$ )	F = 60 Hz	t = 16.7 ms	170	A
		F = 50 Hz	t = 20 ms	160	
$I^2t$	$I^2t$ Value for fusing	tp = 10 ms		128	A <sup>2</sup> s
dI/dt	Critical rate of rise of on-state current $I_G = 2 \times I_{GT}$ , tr ≤ 100 ns	F = 120 Hz	$T_j = 150^\circ\text{C}$	50	A/μs
$V_{DSM}/V_{RSM}$	Non repetitive surge peak off state voltage		$T_j = 25^\circ\text{C}$	700	V
$I_{GM}$	Peak gate current	t <sub>p</sub> = 20 μs	$T_j = 150^\circ\text{C}$	4	A
$P_{G(AV)}$	Average gate power dissipation		$T_j = 150^\circ\text{C}$	1	W
$T_{stg}$ $T_j$	Storage junction temperature range Operating junction temperature range			-40 to +150 -40 to +150	°C

**Table 2. Electrical characteristics ( $T_j = 25^\circ\text{C}$ , unless otherwise specified)**

Symbol	Test conditions	Quadrant		Value	Unit
$I_{GT}^{(1)}$	$V_D = 12\text{ V}$ , $R_L = 33\ \Omega$	II - III	MAX	35	mA
$V_{GT}$		II - III	MAX	1.3	V
$V_{GD}$	$V_D = V_{DRM}$ , $R_L = 3.3\ \text{k}\Omega$	II - III	MIN	0.15	V
$I_H^{(2)}$	$I_T = 100\ \text{mA}$		MAX	35	mA
$I_L$	$I_G = 1.2 \times I_{GT}$	I - III	MAX	50	mA
		II		80	
dV/dt <sup>(2)</sup>	$V_D = 67\% V_{DRM}$ , gate open, $T_j = 150^\circ\text{C}$		MIN	300	V/μs
(dI/dt) <sub>c</sub> <sup>(2)</sup>	Without snubber, $T_j = 150^\circ\text{C}$		MIN	7.1	A/ms

1. minimum  $I_{GT}$  is guaranteed at 5% of  $I_{GT}$  max
2. for both polarities of A2 referenced to A1

**Table 3. Static electrical characteristics**

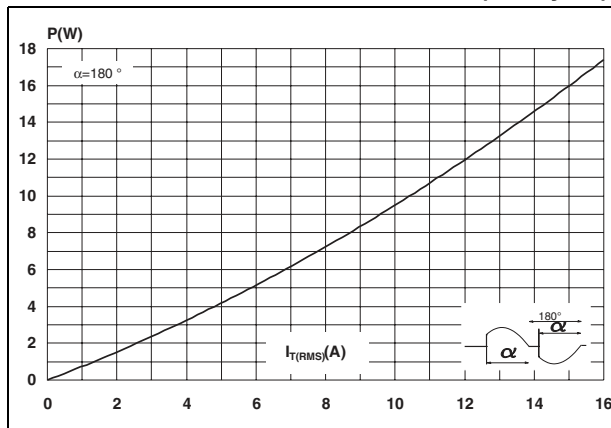
Symbol	Test conditions			Value	Unit
$V_{TM}^{(1)}$	$I_{TM} = 22.5 \text{ A}$ , $t_p = 380 \mu\text{s}$	$T_j = 25^\circ \text{ C}$	MAX	1.5	V
$V_{TO}^{(1)}$		$T_j = 150^\circ \text{ C}$	MAX	0.80	V
$R_D^{(1)}$		$T_j = 150^\circ \text{ C}$	MAX	23	$m\Omega$
$I_{DRM}$ $I_{RRM}$	$V_{DRM} = V_{RRM}$	$T_j = 25^\circ \text{ C}$	MAX	5	$\mu\text{A}$
		$T_j = 150^\circ \text{ C}$		6.4	mA
	$V_D/V_R = 400 \text{ V}$ (at peak mains voltage)	$T_j = 150^\circ \text{ C}$		4.2	

1. for both polarities of A2 referenced to A1

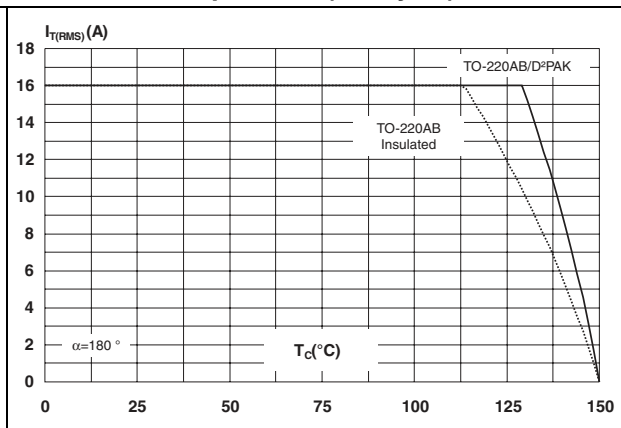
**Table 4. Thermal resistance**

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	Junction to case (AC)	D <sup>2</sup> PAK	1.2	$^\circ\text{C/W}$
$R_{th(j-a)}$	Junction to ambient		45	

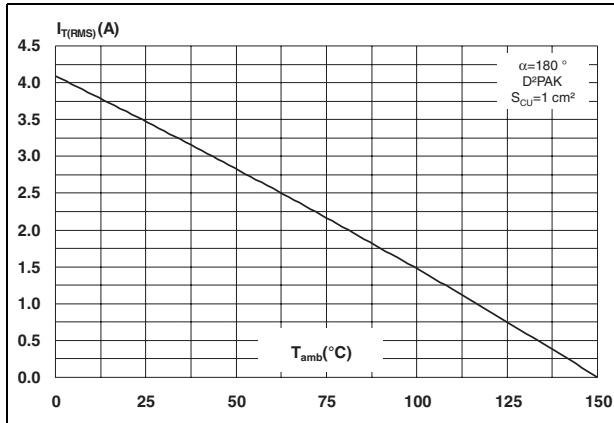
**Figure 1. Maximum power dissipation vs RMS on-state current (full cycle)**



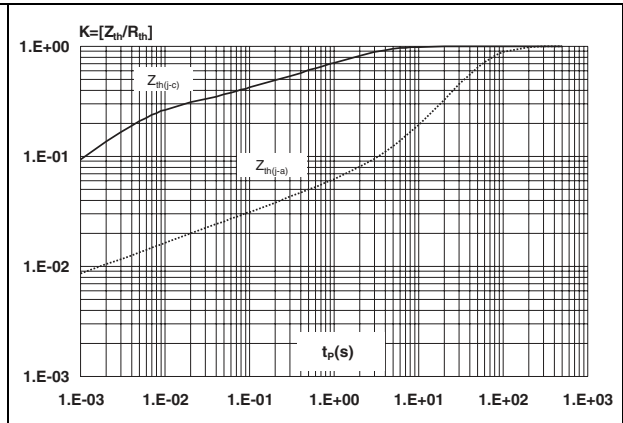
**Figure 2. RMS on-state current vs case temperature (full cycle)**



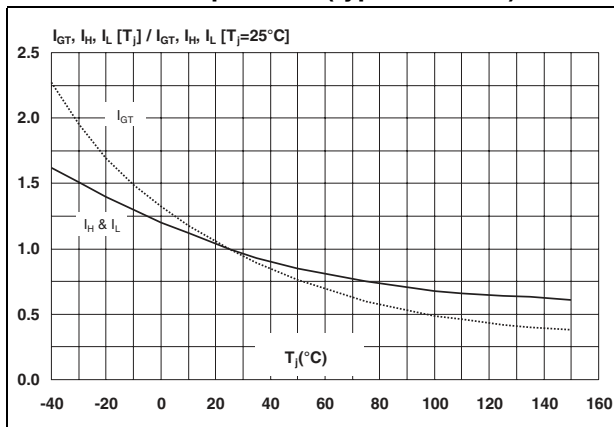
**Figure 3. RMS on-state current vs ambient temperature, PCB FR4,  $e_{CU} = 35 \mu\text{m}$**



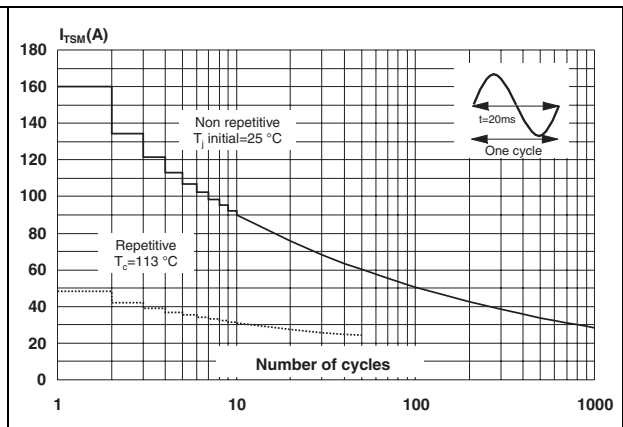
**Figure 4. Relative variation of thermal impedance vs pulse duration**



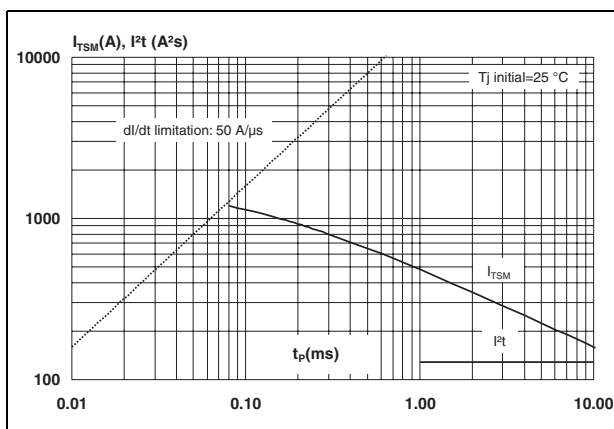
**Figure 5. Relative variation of gate trigger current, holding current and latching current vs junction temperature (typical values)**



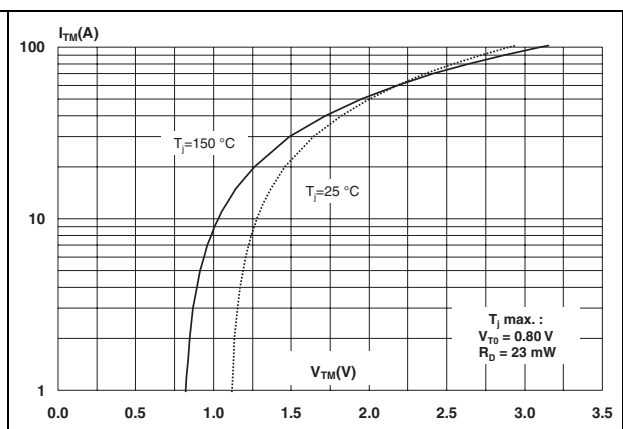
**Figure 6. Surge peak on-state current vs number of cycles**



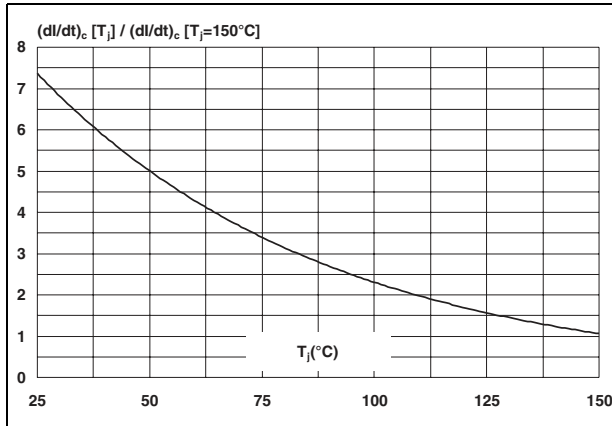
**Figure 7. Non repetitive surge peak on-state current (sinusoidal pulse width  $t_p < 10 \text{ ms}$ ) and corresponding value of  $I^2t$**



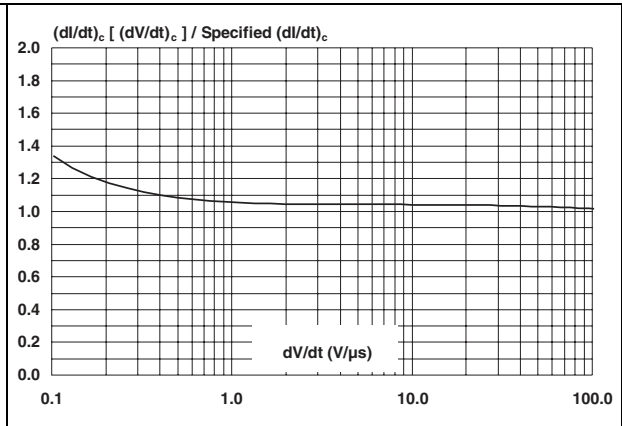
**Figure 8. On-state characteristics (maximum values)**



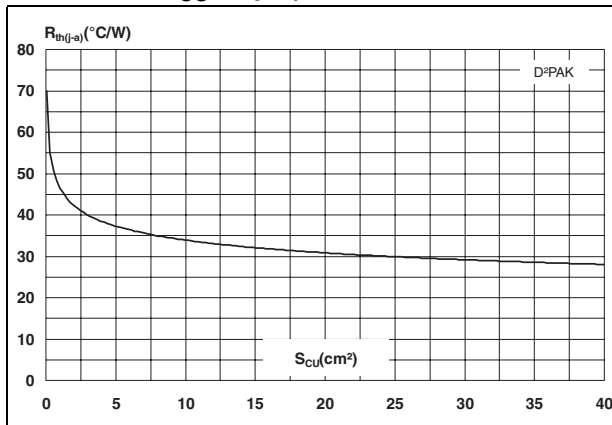
**Figure 9. Relative variation of critical rate of decrease of main current  $(di/dt)_c$  versus junction temperature**



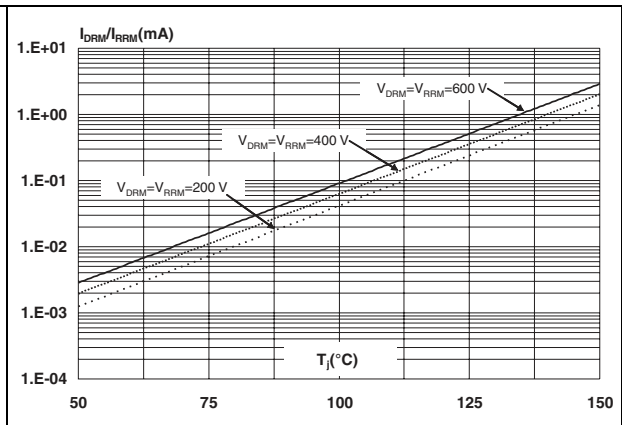
**Figure 10. Relative variation of critical rate of decrease of main current  $(di/dt)_c$  versus reapplied  $dV/dt$  (typical values)**



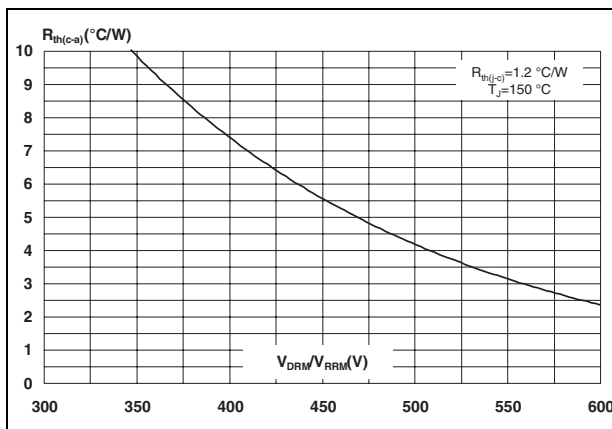
**Figure 11. Variation of thermal resistance, junction to ambient versus copper surface under tab (PCB FR4,  $e_{Cu}$  35  $\mu$ m)**



**Figure 12. Leakage current versus junction temperature for different values of blocking voltage (typical values)**



**Figure 13. Acceptable repetitive peak off-state voltage versus case-ambient thermal resistance**



**Table 6. D<sup>2</sup>PAK Mechanical data**

REF.	DIMENSIONS			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	4.40	4.60	0.173	0.181
A1	2.49	2.69	0.098	0.106
A2	0.03	0.23	0.001	0.009
B	0.70	0.93	0.027	0.037
B2	1.14	1.70	0.045	0.067
C	0.45	0.60	0.017	0.024
C2	1.23	1.36	0.048	0.054
D	8.95	9.35	0.352	0.368
E	10.00	10.40	0.393	0.409
G	4.88	5.28	0.192	0.208
L	15.00	15.85	0.590	0.624
L2	1.27	1.40	0.050	0.055
L3	1.40	1.75	0.055	0.069
M	2.40	3.20	0.094	0.126
R	0.40 typ.		0.016 typ.	
V2	0°	8°	0°	8°

**Figure 14. D<sup>2</sup>PAK Footprint (dimensions in mm)**

