0.5Ω Low-Voltage Dual SPDT Analog Switch

UM4684H *CSP10 2.0×1.5*
UM4684EEUE *MSOP10*

General Description

The UM4684 is a sub 1Ω (0.5Ω at 2.7V) dual SPDT analog switch designed for low voltage applications.
The UM4684 has on-resistance matching(less than 0.05Ω at 2.7V) and flatness (less than 0.2Ω at 2.7V) that are guaranteed over the entire voltage range. Additionally, low logic thresholds make the UM4684 an ideal interface to low voltage DSP control signals.
The UM4684 has fast switching speed with break-before-make guaranteed. In the ON condition, all switching elements conduct equally in both directions. OFF-isolation and crosstalk is -69dB at 100kHz.
The UM4684 is built on high-density low voltage CMOS process, and contains the additional benefit of 2000V ESD protection.
As a committed partner to the community and the environment, Union manufactures this product with lead (Pb)-free device terminations.

Applications

- Cellular Phones
- Speaker Headset Switching
- Audio and Video Signal Routing
- PCMCIA Cards
- Battery Operated Systems
- Relay Replacement
- Power Routing
- Communication Circuits

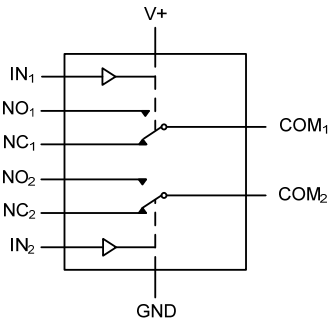
Features

- CSP10 & MSOP10 Packages
- ESD Protection >2000V
- +1.8V to +5.5V Single Supply Operation
- NC Switch R_{ON}: 0.5Ω (+2.7V Supply)
- NO Switch R_{ON}: 0.6Ω (+2.7V Supply)
- R_{ON} Match between Channels: 0.05Ω Max (+2.7V Supply)
- R_{ON} Flatness over Signal Range: 0.2Ω Max (+2.7V Supply)
- 1.8V Logic Compatibility
- Low Crosstalk: -69dB (100kHz)
- High Off-Isolation: -69dB (100kHz)

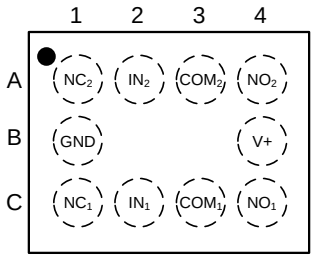
Ordering Information

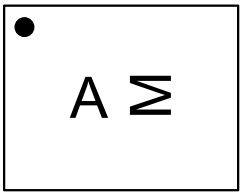
Part Number	Temp. Range	Packaging Type	Marking Code	Shipping Qty
UM4684H	-40°C to 85°C	CSP10 2.0×1.5	A	3000pcs/7 Inch Tape & Reel
UM4684EEUE	-40°C to 85°C	MSOP10	UM4684EEUE	3000pcs/13 Inch Tape & Reel

Pin Configurations **Top View**



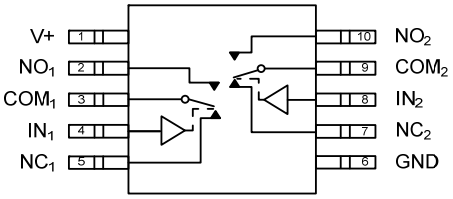
(Top View)

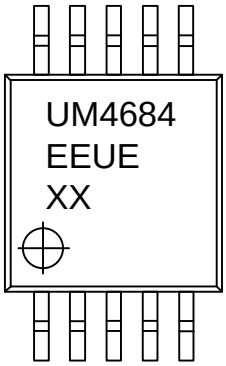




M: Month Code
UM4684H
CSP10 2.0×1.5

(Top View)





XX: Week Code
UM4684EEUE
MSOP10

Ball Mapping for UM4684H

	1	2	3	4
A	NC_2	IN_2	COM_2	NO_2
B	GND			V+
C	NC_1	IN_1	COM_1	NO_1

Transparent Top View

Pin Description

Pin Name	Pin Number		Function
	CSP10 2.0×1.5	MSOP10	
NC_	A1, C1	5, 7	Analog Switch—Normally Closed Terminal
IN_	A2, C2	4, 8	Digital Control Input
COM_	A3, C3	3, 9	Analog Switch—Common Terminal
NO_	A4, C4	2, 10	Analog Switch—Normally Open Terminal
V+	B4	1	Positive Supply Voltage Input
GND	B1	6	Ground

Function Table

IN_	NO_	NC_
0	OFF	ON
1	ON	OFF

Absolute Maximum Ratings (Note 1)

Parameter		Value	Unit
Voltage on V+ Pin (Reference to GND)		-0.3 to +6	V
Voltage on IN_, COM_, NC_, NO_ Pins (Note 2) (Reference to GND)		-0.3 to (V_++0.3)	V
Continuous Current (NO_, NC_, COM_)		±300	mA
Peak Current (Pulsed at 1 ms, 10% Duty Cycle)		±500	mA
Storage Temperature		-65 to 150	°C
Package Solder Reflow Conditions (Note 3)	IR/Convection	250	°C
	ESD per Method 3015.7	>2	kV
Power Dissipation (Packages) (Note 4)	CSP10 (Note 5)	457	mW

Note 1: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Signals on NC_, NO_, or COM_ or IN_ exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

Note 3: Refer to IPC/JEDEC (J-STD-020B).

Note 4: All bumps welded or soldered to PC Board.

Note 5: Derate 5.7mW/°C above 70°C.

Electrical Characteristics (V_+=3V, ±10% deviation, V_{IN}=0.5 or 1.4V (Note 6))

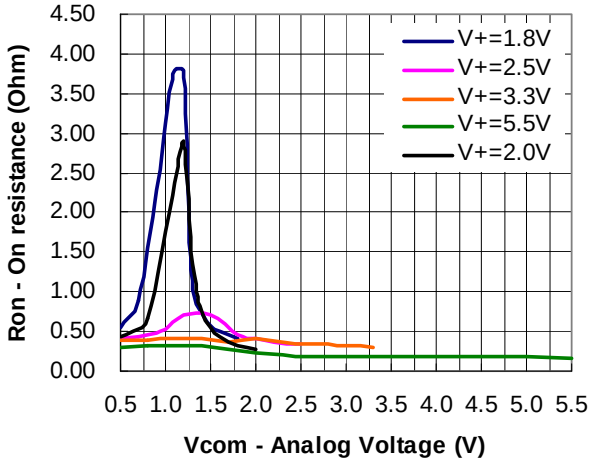
Parameter	Symbol	Test Conditions Otherwise Unless Specified	Temp (Note 7)	Limits (-40°C to 85°C)			Unit
				Min (Note 9)	Typ (Note 8)	Max (Note 9)	
Analog Switch							
Analog Signal Range (Note 10)	V_{NO} V_{NC} V_{COM}		Full	0		V_+	V
On-Resistance (Note 10)	R_{on}	V_+=2.7V, V_{COM}=0.6/1.5V, I_{NO}, I_{NC}=100mA	Room Full		0.5	0.8 1.0	Ω
R_{ON} Flatness (Note 10)	R_{on} Flatness		Room			0.15	
On-Resistance Match Between Channels (Note 10)	$\Delta R_{DS(on)}$		Room			0.05	
Switch Off Leakage Current	$I_{NO(off)}$, $I_{NC(off)}$	V_+=3.3V, V_{NO},V_{NC}=0.3V/3V, V_{COM}=3V/0.3V	Room Full	-2 -20		2 20	nA
	$I_{COM(off)}$		Room Full	-2 -20		2 20	
Channel-On Leakage Current	$I_{COM(on)}$	V_+=3.3V, V_{NO}, V_{NC}=V_{COM} =0.3V/3V	Room Full	-2 -20		2 20	
Digital Control							
Input High Voltage (Note 10)	V_{INH}		Full	1.4			V
Input Low Voltage	V_{INL}		Full			0.5	
Input Capacitance	C_{IN}		Full		10		pF
Input Current	I_{INL} or I_{INH}	V_{IN}=0 or V_+	Full	-1		1	μA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC}=2.0V, R_L=50Ω, C_L=35pF	Room Full		52	82 90	ns
Turn-Off Time	t_{OFF}		Room Full		43	73 78	
Break-Before-Make Time	t_d	V_{NO} or V_{NC}=2.0V, R_L=50Ω, C_L=35pF	Full	1	6		ns
Charge Injection (Note 10)	Q_{INJ}	C_L=1nF, V_{GEN}=1.5V, R_{GEN}=0Ω	Room		21		pC
Off-Isolation (Note 10)	O_{IRR}	R_L=50Ω, C_L=5pF, f=100kHz	Room		-69		dB
Crosstalk (Note 10)	X_{TALK}		Room		-69		
-3dB Bandwidth	BW	R_L=50Ω, C_L=5pF	Room		20		MHz

NO NC Off Capacitance (Note 10)	$C_{NO(off)}$ $C_{NC(off)}$	V_{IN}=0 or V_+, f=1MHz	Room Room		145 145		pF
Channel On Capacitance (Note 10)	$C_{NO(on)}$ $C_{NC(on)}$		Room Room		406 406		
Power Supply							
Power Supply Range	V_+		Full	1.8		5.5	V
Power Supply Current	I_+	V_{IN}=0 or V_+	Room Full		0.001	1.0 1.0	μA

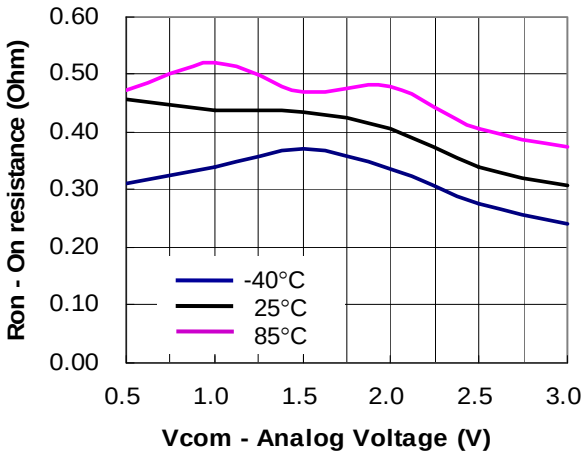
Note 6. V_{IN}=input voltage to perform proper function.
Note 7. Room=25°C, Full=as determined by the operating suffix.
Note 8. Typical values are for design aid only, not guaranteed nor subjected to production testing.
Note 9. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum，is used in this datasheet.
Note 10. Guaranteed by design, nor subjected to production testing.

Typical Operating Characteristics

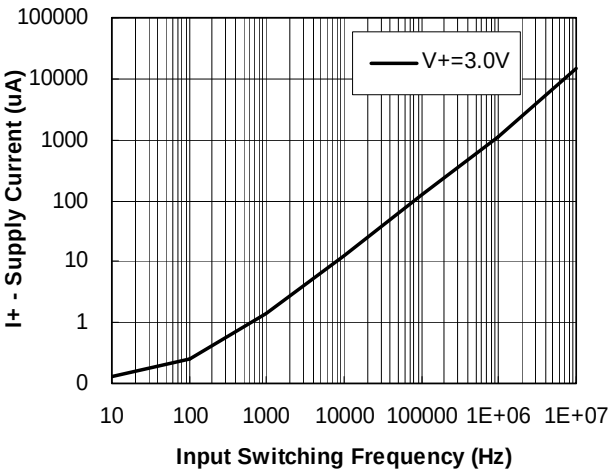
Ron vs.Vcom and Supply Voltage



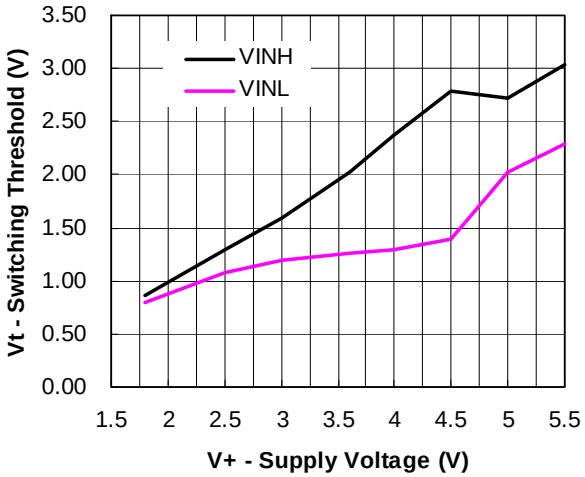
Ron vs.Vcom and Temperature (NC1)



Supply Current vs. Input Switching Frequency

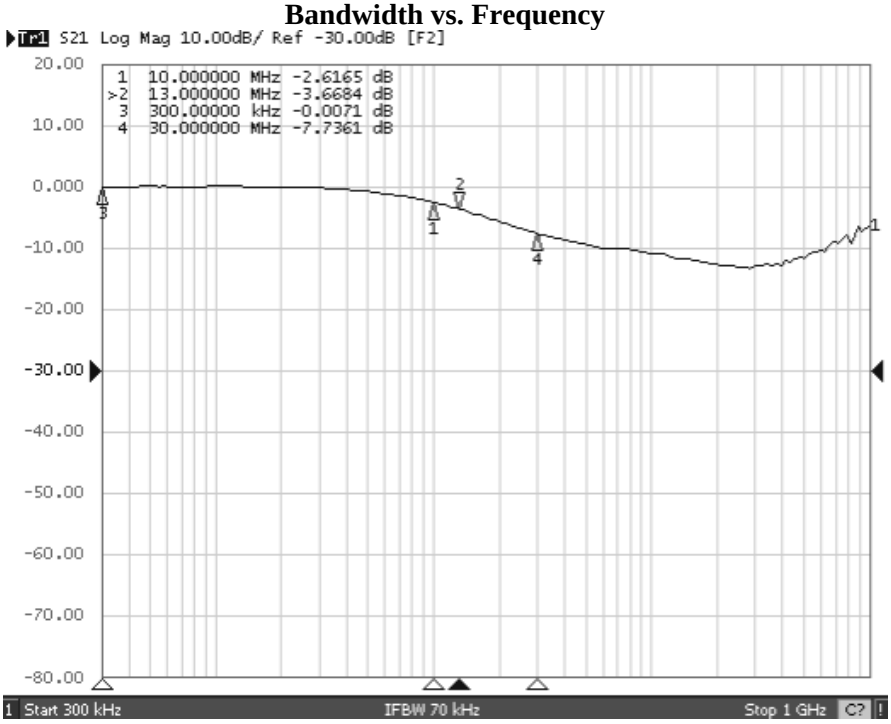


Switching Threshold vs. Supply Voltage (V)

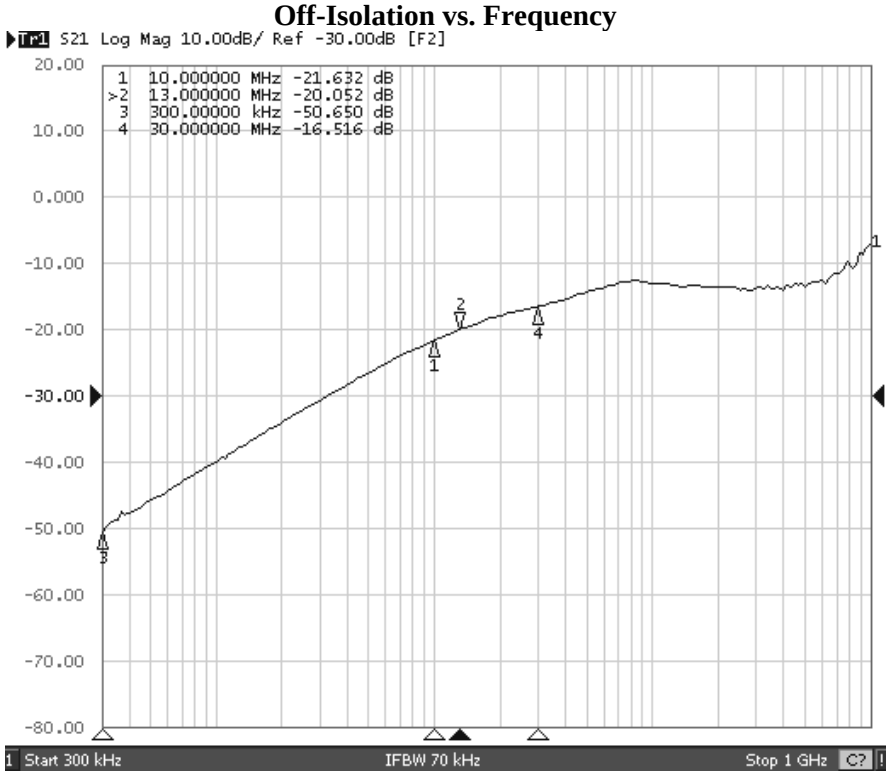


Typical Operating Characteristics (Continued)

Bandwidth vs. Frequency



Off-Isolation vs. Frequency



Test Circuits/Timing Diagrams

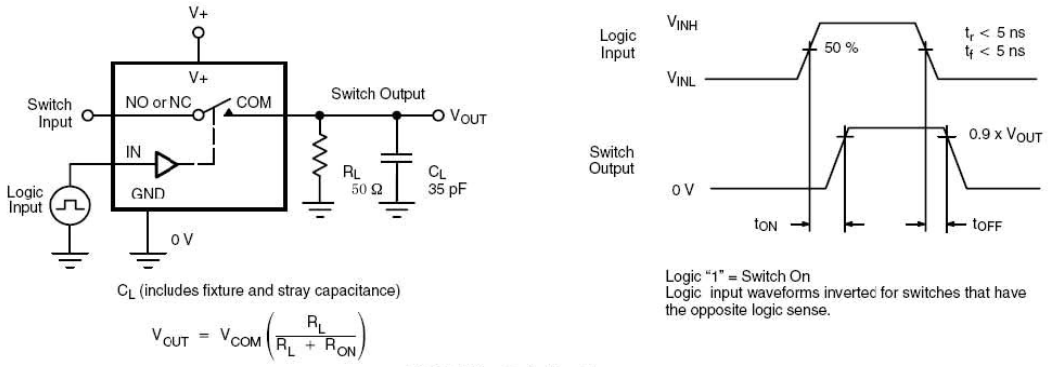


FIGURE 1. Switching Time

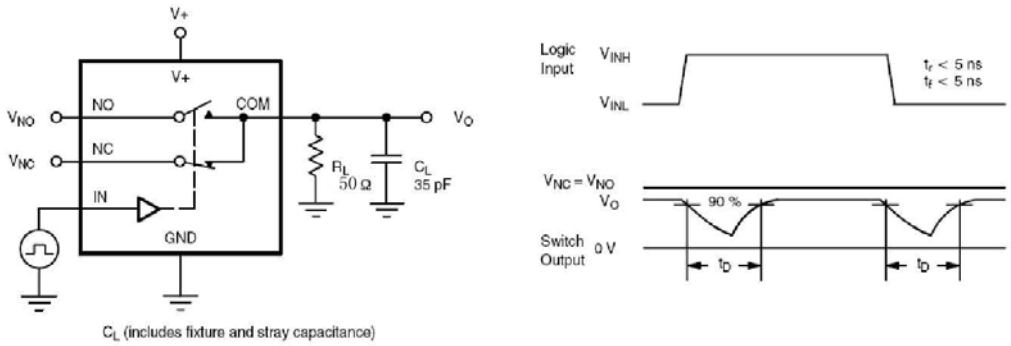


FIGURE 2. Break-Before-Make Interval

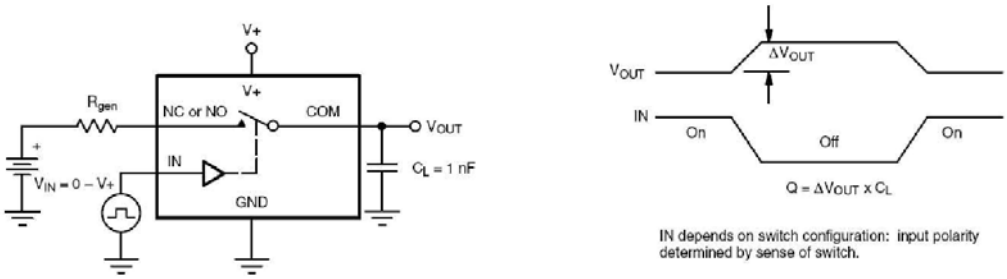


FIGURE 3. Charge Injection

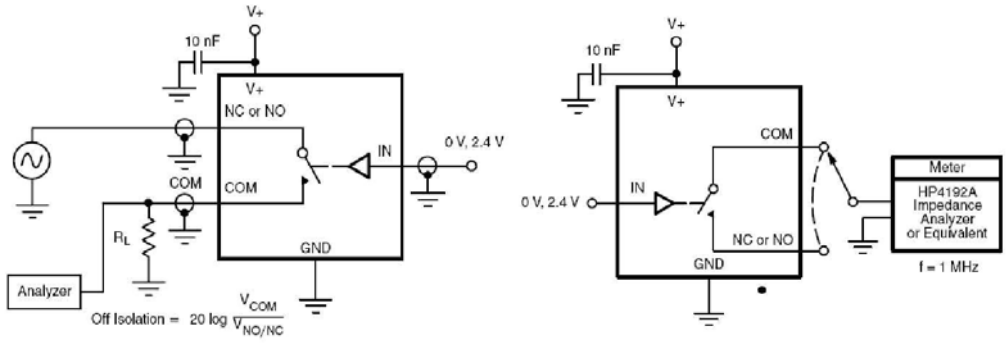


FIGURE 4. Off-Isolation

FIGURE 5. Channel Off/On Capacitance

Applications Information

Digital Control Inputs

The UM4684 logic inputs accept up to +5.5V regardless of supply voltage. For example, with a +3.3V supply, IN_ may be driven low to GND and high to 5.5V. Driving IN_ rail-to-rail minimizes power consumption. Logic levels for a +1.8V supply are 0.5V (low) and 1.4V (high).

Analog Signal Levels

Analog signals that range over the entire supply voltage (V+ to GND) is passed with very little change in on-resistance (see Typical Operating Characteristics). The switches are bidirectional, so the NO_, NC_, and COM_ pins can be either inputs or outputs.

Caution

Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to devices.
Proper power-supply sequencing is recommended for all CMOS devices. Always apply V+ before applying analog signals, especially if the analog signal is not current limited. If this sequencing is not possible, and if the analog inputs are not current limited to <20mA, add a small signal diode (D1) as shown in Figure 6. Adding a protection diode reduces the analog range to a diode drop (about 0.7V) below V+ (for D1). RON increases slightly at low supply voltages. Maximum supply voltage (V+) must not exceed +6V. Protection diode D1 also protects against some over voltage situations. No damage will result on Figure 6's circuit if the supply voltage is below the absolute maximum rating applied to an analog signal pin.

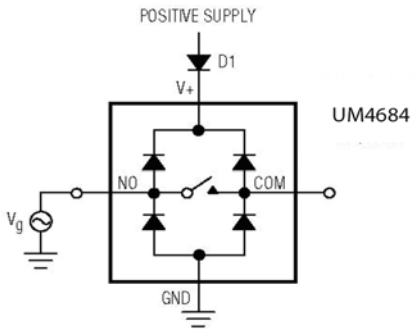
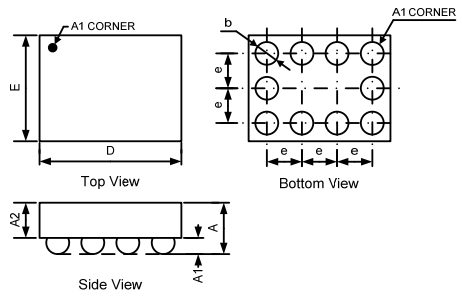


Figure 6

Package Information

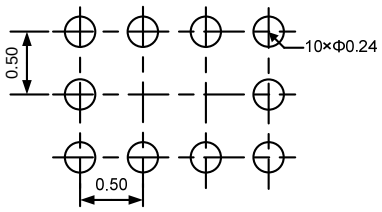
UM4684H CSP10 2.0×1.5

Outline Drawing



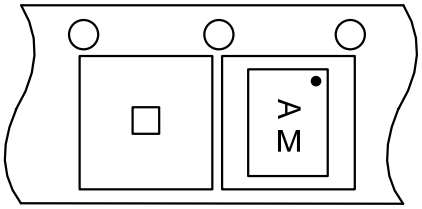
Symbol	DIMENSIONS					
	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	0.68	0.72	0.76	0.027	0.028	0.030
A1	0.21	0.231	0.24	0.0083	0.0091	0.0094
A2	0.47	0.49	0.52	0.0185	0.0193	0.0205
b	0.27	0.31	0.34	0.011	0.012	0.013
D	2.00	-	2.10	0.079	-	0.083
E	1.50	-	1.60	0.059	-	0.063
e	0.50BSC			0.020BSC		

Land Pattern



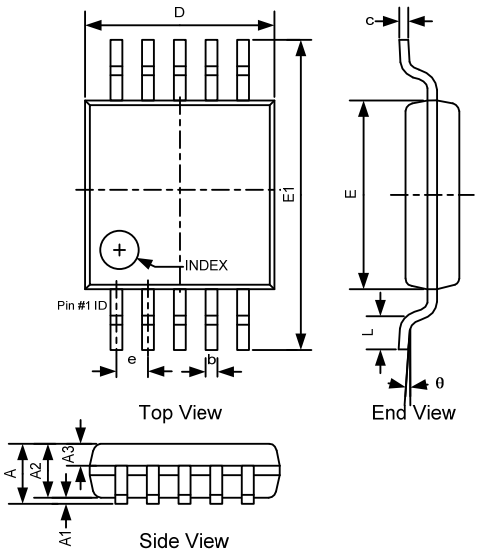
NOTES:
1. Bump is Lead Free Sn/Ag/Cu;
2. Unit: mm;
3. Non-solder mask defined copper landing pad;
4. Laser Mark on silicon die back; back-lapped.

Tape and Reel Orientation



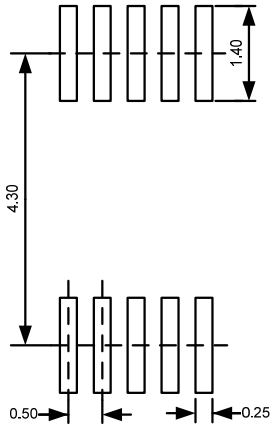
UM4684EEUE MSOP10

Outline Drawing



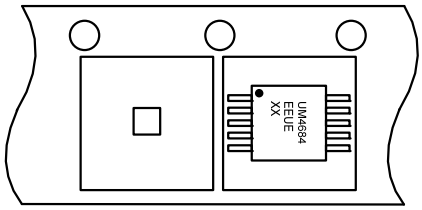
DIMENSIONS						
Symbol	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.10	-	-	0.043
A1	0.00	-	0.15	0.000	-	0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
A3	0.25	0.35	0.39	0.010	0.014	0.015
b	0.18	-	0.28	0.007	-	0.011
c	0.09	-	0.23	0.004	-	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	4.70	4.90	5.10	0.185	0.193	0.201
e	0.50BSC			0.020BSC		
L	0.40	0.60	0.80	0.016	0.024	0.031
θ	0°	-	8°	0°	-	8°

Land Pattern



NOTES:
1. Compound dimension: 3.00×3.00;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

Tape and Reel Orientation



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