Numonyx^{TM} Axcell^{TM} P33/P30

256-Mbit, 256-Mbit/256-Mbit stack
Specification Update

NOV 2009

Contents

Revision History

Date	Version	Description
01/30/09	1.0	Initial Release
03/12/09	1.1	Added Errata #2, #3, #4
07/14/09	2.0	Added Errata #5
11/02/09	3.0	Combine Errata #2 and #5 into Errata #2
11/19/09	4.0	Update Errata #2, #3 and remove #4 Include 256-Mbit/256-Mbit in this Errata

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata and specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published

Affected Documents/Related Documents

Title	Order
Numonyx™ Axcell™ Flash Memory (P30 65nm) 256-Mbit, 256-Mbit/256-Mbit Datasheet	320002
Numonyx™ Axcell™ Flash Memory (P33 65nm) 256-Mbit, 256-Mbit/256-Mbit Datasheet	320003

Nomenclature

Errata are design defects or errors. These may cause the Numonyx™ Axcell™ memory behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Numonyx™ Axcell™ memory components. Numonyx may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box)	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document

Errata

Number	Stepping(s) Affected	Page	Status	Errata
1	A1	8	No Fix	Erase Suspend Latency Erratum
2	A1	8	Plan Fix	Flexlock Write Timing Erratum
3	A1	9	Fixed	Password Access Erratum

Specification Changes

Number	Page	Specification Changes
-	-	-

Specification Clarifications

Number	Page	Specification Clarifications
-	-	-

Documentation Changes

Number	Document Revision	Section	Document Changes
-	-	-	-

Errata

1.   **Erase Suspend Latency**

Problem: Erase suspend latency does not meet the current spec. New spec is 25μs typical and 30μs max.

Implication: The time required to enter suspend from the erase suspend command exceeds the data sheet spec of 20μs typical and 25μs max at the worst-case suspend point. Depending on the software implementation, the impact could be nothing (if software polls status register) to a timeout error (if a separate timer is used).

Workaround: Extend timer to account for worst-case condition. If polling status register for suspend condition, no work around is needed.

Status: No fix.

2.   **Flexlock Write Timing**

Problem: When customer uses command sets starting with 60h, including RCR set, block Lock, and block unlock, the block lock status might be altered inadvertently.

Implication: The table below describes the implications in different scenarios.

WP#	Operation	Command Sequence	Implication
Low	Unlock	60h + D0h	Lock status might be set to either 01h or 03h unexpectedly (00h as expected data), which leads to program/erase failure on certain blocks.
	Lock	60h + 01h	Lock status might be set to 03h unexpectedly (01h as expected data), which means the block is locked-down.
	RCR Configuration	60h + 03h	Lock status might be altered unexpectedly.
High	Unlock	60h + D0h	Lock status might be set to 02h unexpectedly (00h as expected data); while the block can be erased or programmed.
	Lock	60h + 01h	Lock status might be set to 03h unexpectedly (01h as expected data); which means the block is protected.
	RCR Configuration	60h + 03h	Lock status might be altered inadvertently.

Workaround: If the interval between 60h and its subsequent command can be guaranteed within 20μs, Option I is recommended, otherwise Option II should be selected.

               Option I: The table below lists the detail command sequences:

Command Sequence	Data bus	Address bus	Remarks
1	90h	Block Address	Read Lock Status
2	Read	Block Address + 02h	
3[2][3]	60h	Block Address[1]	Lock/Unlock/RCR Configuration
4[2][3]	D0h/01h/03h	Block Address[1]	

               Notes:
                  (1) Block Address refers to RCR configuration data only when the 60h command sequence is used to set RCR register combined with 03h subsequent command.
                  (2) For the third and fourth command sequences, the Block Address must be the same.
                  (3) The interval between 60h command and its subsequent D0h/01h/2Fh/03h commands should be less than 20μs.

               Option II:
               a)   Always tie WP# pin to VCC or drive WP# > V_{IH}
               b)   Unlock/lock blocks every time after setting RCR register.
               c)   Don't check lock status DQ1 after block lock/unlock operation.

Status: Will be fixed in the next stepping.

3.   **Password Access de-featured for top boot devices**
Problem: Password Access is de-featured for top-boot devices on this stepping.

Implication: Customer will not be able to use the new Password Access feature on P33/P30.

Workaround: None.

Status: Fixed on materials shipped since ww12'10 (marking "x012xxxx" and later).

Specification Changes

Not Applicable

Specification Clarifications

Not Applicable

Documentation Changes

Not Applicable