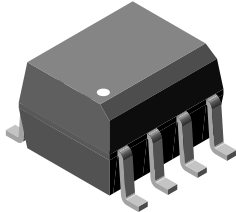
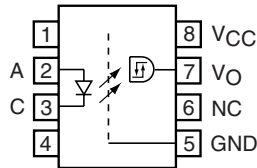


## High Speed Optocoupler, 5 MBd, in SOIC-8 Package



I179074



### DESCRIPTION

The single channel 5.0 Mb/s SFH6720T and SFH6721T high speed optocoupler consists of a GaAlAs infrared emitting diode, optically coupled with an integrated photo diode. The detector incorporates a Schmitt-Trigger stage for improved noise immunity. A Faraday shield provides a common mode transient immunity of 1000 V/ $\mu$ s at  $V_{CM} = 50$  V for SFH6720T and 2500 V/ $\mu$ s at  $V_{CM} = 400$  V for SFH6721T.

The SFH6720T and SFH6721T uses an industry standard SOIC-8A package.

### FEATURES

- Data Rate 5.0 Mb/s (2.5 Mb/s over Temperature)
- Buffer
- Isolation Test Voltage, 4000 V<sub>RMS</sub>
- TTL, LSTTL and CMOS Compatible
- Internal Shield for Very High Common Mode Transient Immunity
- Wide Supply Voltage Range (4.5 to 15 V)
- Low Input Current (1.6 mA to 5.0 mA)
- Lead (Pb)-free component
- Component in accordance to RoHS 2002/95/EC and WEEE 2002/96/EC


**RoHS**  
COMPLIANT

### AGENCY APPROVALS

- UL1577, File No. E52744 System Code Y
- DIN EN 60747-5-2 (VDE0884)
- DIN EN 60747-5-5 pending
- Available with Option 1

### APPLICATIONS

- Industrial Control
- Replace Pulse Transformers
- Routine Logic Interfacing
- Motion/Power Control
- High Speed Line Receiver
- Microprocessor System Interfaces
- Computer Peripheral Interfaces

### ORDER INFORMATION

PART	REMARKS
SFH6720T	$ CM_H  > 1000$ , at $ V_{CM}  = 50$ V, SOIC-8
SFH6721T	$ CM_H  > 2500$ , at $ V_{CM}  = 400$ V, SOIC-8

Note:

Available only on tape and reel.

For additional information on the available options refer to Option Information.

### TRUTH TABLE (POSITIVE LOGIC)

PARTNUMBER	IR DIODE	OUTPUT
SFH6720T	on	H
	off	L
SFH6721T	on	H
	off	L

ABSOLUTE MAXIMUM RATINGS <sup>1)</sup>				
PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
<b>INPUT</b>				
Reverse voltage		$V_R$	3.0	V
DC Forward current		$I_F$	10	mA
Surge forward	$t_p \leq 1.0 \mu\text{s}$ , 300 pulses/s	$I_{FSM}$	1.0	mA
Power dissipation		$P_{diss}$	20	mW
<b>OUTPUT</b>				
Supply voltage		$V_{CC}$	- 0.5 to + 15	V
Output voltage		$V_O$	- 0.5 to + 15	V
Average output current		$I_O$	25	mA
Power dissipation		$P_{diss}$	100	mW
<b>COUPLER</b>				
Storage temperature range		$T_{stg}$	- 55 to + 125	°C
Ambient temperature range		$T_{amb}$	+ 85	°C
Lead soldering temperature	$t = 10 \text{ s}$		260	°C
Isolation test voltage	$t = 1.0 \text{ s}$	$V_{ISO}$	4000	$V_{RMS}$
Pollution degree			2	
Creepage distance and clearance			4.0	mm
Comperative tracking index per DIN IEC112/VDE 0303, part 1			175	
Isolation resistance	$V_{IO} = 500 \text{ V}$ , $T_{amb} = 25 \text{ °C}$	$R_{IO}$	$10^{12}$	$\Omega$
	$V_{IO} = 500 \text{ V}$ , $T_{amb} = 100 \text{ °C}$	$R_{IO}$	$10^{11}$	$\Omega$

Note:

<sup>1)</sup>  $T_{amb} = 25 \text{ °C}$  unless otherwise specified.

Stresses in excess of the absolute Maximum Ratings can cause permanent damage to the device. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this document. Exposure to absolute Maximum Rating for extended periods of the time can adversely affect reliability.

RECOMMENDED OPERATING CONDITIONS <sup>1)</sup>						
PARAMETER	TEST CONDITION	SYMBOL	MIN	TYP.	MAX	UNIT
Supply voltage		$V_{CC}$	4.5		15	V
Forward input current		$I_{Fon}$	1.6 <sup>2)</sup>		5.0	mA
		$I_{Foff}$			0.1	mA
Operating temperature		$T_A$	- 40		85	°C

Note:

<sup>1)</sup> A 0.1  $\mu\text{F}$  bypass capacitor connected between pins 5 and 8 must be used.

<sup>2)</sup> We recommended using a 2.2 mA if to permit at least 20 % CTR degradation guard band.



<b>ELECTRICAL CHARACTERISTICS<sup>1)</sup></b>						
PARAMETER	TEST CONDITION	SYMBOL	MIN	TYP.	MAX	UNIT
<b>INPUT</b>						
Forward voltage	$I_F = 5.0 \text{ mA}$	$V_F$		1.6	1.75	V
		$V_F$			1.9	V
Input current hysteresis	$V_{CC} = 5.0 \text{ V}, I_{HYS} = I_{Fon} - I_{Foff}$	$I_{HYS}$	0.1			V
Reverse current	$V_R = 3.0 \text{ V}$	$I_R$		0.5	10	$\mu\text{A}$
Capacitance	$V_R = 0 \text{ V}, f = 1.0 \text{ MHz}$	$C_O$		60		pF
Thermal resistance		$R_{thja}$		700		K/W
<b>OUTPUT</b>						
Logic low output voltage	$I_{OL} = 6.4 \text{ mA}$	$V_{OL}$			0.5	V
Logic high output voltage	$I_{OH} = -2.6 \text{ mA},$ $* V_{OH} = V_{CC} - 1.8 \text{ V}$	$V_{OH}$	2.4			V
Output leakage current ( $V_{UT} > V_{CC}$ )	$V_O = 5.5 \text{ V}, V_{CC} = 4.5 \text{ V},$ $I_F = 5.0 \text{ mA}$	$I_{OHH}$		0.5	100	$\mu\text{A}$
Output leakage current ( $V_{OUT} > V_{CC}$ )	$V_O = 15 \text{ V}, V_{CC} = 4.5 \text{ V},$ $I_F = 5.0 \text{ mA}$	$I_{OHH}$		1.0	500	$\mu\text{A}$
Logic low supply current	$V_{CC} = 5.5 \text{ V}, I_F = 0$	$I_{CCL}$		3.7	6.0	mA
	$V_{CC} = 15 \text{ V}, I = 0$	$I_{CCL}$		4.1	6.5	mA
Logic high supply current	$V_{CC} = 5.5 \text{ V}, I_F = 5.0 \text{ mA}$	$I_{CCH}$		3.4	4.0	mA
	$V_{CC} = 15 \text{ V}, I_F = 5.0 \text{ mA}$	$I_{CCH}$		3.7	5.0	mA
Logic low short circuit output current (output short circuit time $\leq 10 \text{ ms}$ )	$V_O = V_{CC} = 5.5 \text{ V}, I_F = 0$	$I_{OSL}$	25			mA
	$V_O = V_{CC} = 15 \text{ V}, I_F = 0$	$I_{OSL}$	40			mA
Logic high short circuit output current (output short circuit time $\leq 10 \text{ ms}$ )	$V_{CC} = 5.5 \text{ V}, V_O = 0 \text{ V},$ $I_F = 5.0 \text{ mA}$	$I_{OSH}$			- 10	mA
	$V_{CC} = 15 \text{ V}, V_O = 0 \text{ V}, I_F = 5.0 \text{ mA}$	$I_{OSH}$			- 25	mA
Thermal resistance		$R_{thja}$		300		K/W
<b>COUPLER</b>						
Capacitance (input-output)	$f = 1.0 \text{ MHz},$ pins 1-4 and 5-8 shorted together	$C_{IO}$		0.6		pF
Isolation resistance	$V_{IO} = 500 \text{ V}, T_{amb} = 25 \text{ }^\circ\text{C}$		$10^{12}$			$\Omega$
	$V_{IO} = 500 \text{ V}, T_{amb} = 100 \text{ }^\circ\text{C}$		$10^{11}$			$\Omega$

Note:

<sup>1)</sup> -  $-40 \text{ }^\circ\text{C} \leq T_{amb} \leq 85 \text{ }^\circ\text{C}; 4.5 \text{ V} \leq V_{CC} \leq 15 \text{ V}; 1.6 \text{ mA} \leq I_{Fon} \leq 5.0 \text{ mA}; 2.0 \leq V_{EH} \leq 15 \text{ V}; 0 \leq V_{EL} \leq 0.8 \text{ V}; 0 \text{ mA} \leq I_{Foff} \leq 0.1 \text{ mA}.$

Typical values:  $T_{amb} = 25 \text{ }^\circ\text{C}; V_{CC} = 5.0 \text{ V}; I_{Fon} = 3.0 \text{ mA}$  unless otherwise specified.

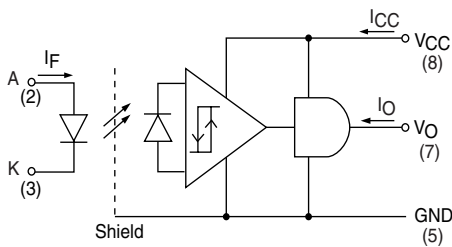
Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluation. Typical values are for information only and are not part of the testing requirements.

SWITCHING CHARACTERISTICS <sup>1)</sup>						
PARAMETER	TEST CONDITION	SYMBOL	MIN	TYP.	MAX	UNIT
Propagation delay time to logic low output level	Without peaking capacitor	$t_{PHL}$		120		ns
	With peaking capacitor	$t_{PHL}$		115	300	ns
Propagation delay time to logic high output level	Without peaking capacitor	$t_{PLH}$		125		ns
	With peaking capacitor	$t_{PLH}$		90	300	ns
Output rise time	10 % to 90 %	$t_r$		40		ns
Output fall time	90 % to 10 %	$t_f$		10		ns

Note:

<sup>1)</sup>  $0\text{ }^\circ\text{C} \leq T_{amb} \leq 85\text{ }^\circ\text{C}$ ;  $4.5\text{ V} \leq V_{CC} \leq 15\text{ V}$ ;  $1.6\text{ mA} \leq I_{Fon} \leq 5.0\text{ mA}$ ;  $0\text{ mA} \leq I_{Foff} \leq 0.1\text{ mA}$ .

Typical values:  $T_{amb} = 25\text{ }^\circ\text{C}$ ;  $V_{CC} = 5.0\text{ V}$ ;  $I_{Fon} = 3.0\text{ mA}$  unless otherwise specified (a  $0.1\text{ }\mu\text{F}$  bypass capacitor connected between pins 5 and 8 must be used).



sfh6720\_00

COMMON MODE TRANSIENT IMMUNITY <sup>1)</sup>							
PARAMETER	TEST CONDITION	PART	SYMBOL	MIN	TYP.	MAX	UNIT
Logic High Common Mode Transient Immunity <sup>2)</sup>	$ V_{CM}  = 50\text{ V}$ , $I_F = 1.6\text{ mA}$	SFH6720T	$ CM_H $	1000			V/ $\mu\text{s}$
	$ V_{CM}  = 400\text{ V}$ , $I_F = 1.6\text{ mA}$	SFH6721T	$ CM_H $	2500			V/ $\mu\text{s}$
Logic Low Common Mode Transient Immunity <sup>2)</sup>	$ V_{CM}  = 50\text{ V}$ , $I_F = 0\text{ mA}$	SFH6720T	$ CM_L $	1000			V/ $\mu\text{s}$
	$ V_{CM}  = 400\text{ V}$ , $I_F = 0\text{ mA}$	SFH6721T	$CM_L $	2500			V/ $\mu\text{s}$

Note:

<sup>1)</sup>  $T_{amb} = 25\text{ }^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V}$ .<sup>2)</sup>

<sup>2)</sup>  $CM_H$  is the maximum slew rate of a common mode voltage  $V_{CM}$  at which the output voltage remains at logic high level ( $V_O > 2.0\text{ V}$ ).  $CM_L$  is the maximum slew rate of a common mode voltage  $V_{CM}$  at which the output voltage remains at logic high level ( $V_O < 0.8\text{ V}$ ).

SAFETY AND INSULATION RATINGS <sup>1)</sup>						
PARAMETER	TEST CONDITION	SYMBOL	MIN	TYP.	MAX	UNIT
Climatic Classification (according to IEC 68 part 1)				55/100/21		
Comparative Tracking Index		CTI	175		399	
$V_{IOTM}$			6000			V
$V_{IORM}$			560			V
$P_{SO}$					350	mW
$I_{SI}$					150	mA
$T_{SI}$					165	$^\circ\text{C}$
Creepage			4			mm
Clearance			4			mm
Insulation thickness, reinforced rated	per IEC60950 2.10.5.1		0.2			mm

Note:

<sup>1)</sup> As per IEC60747-5-2, §7.4.3.8.1, this optocoupler is suitable for "safe electrical insulation" only within the safety ratings. Compliance with the safety ratings shall be ensured by means of protective circuits.

## TYPICAL CHARACTERISTICS

$T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified

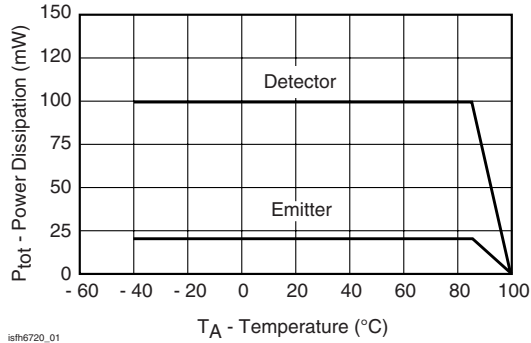


Figure 1. Permissible Total Power Dissipation vs. Temperature

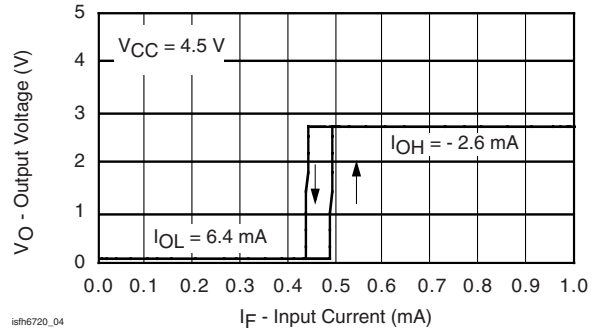


Figure 4. Typical Output Voltage vs. Forward Input Current

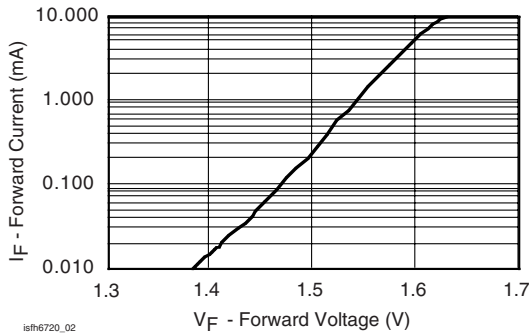


Figure 2. Typical Input Diode Forward Current vs. Forward Voltage

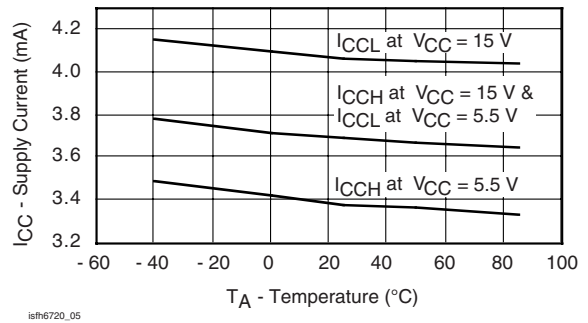


Figure 5. Typical Supply Current vs. Temperature

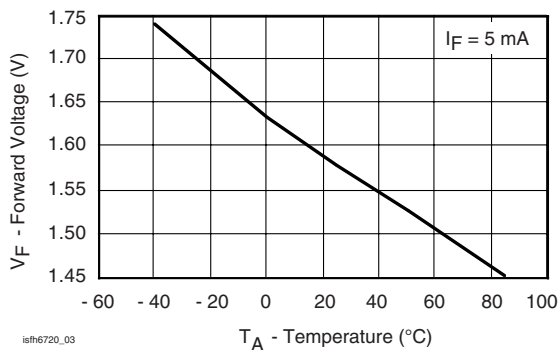


Figure 3. Typical Forward Input Voltage vs. Temperature

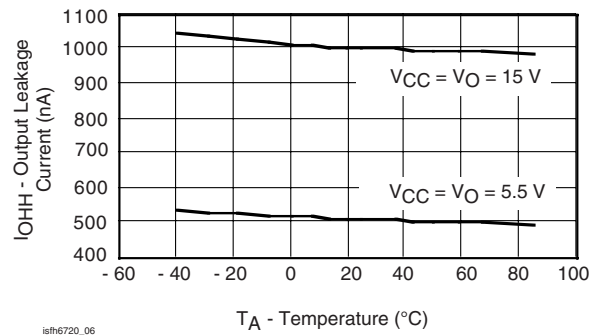


Figure 6. Typical Output Leakage Current vs. Temperature

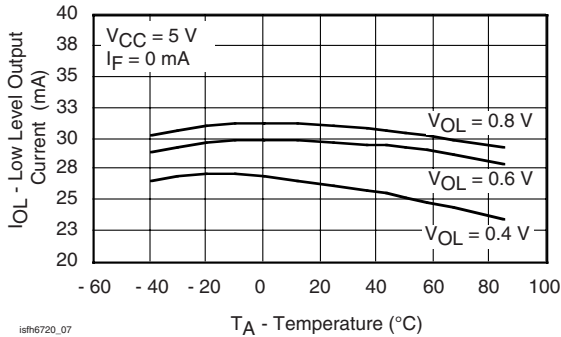


Figure 7. Typical Low Level Output Current vs. Temperature

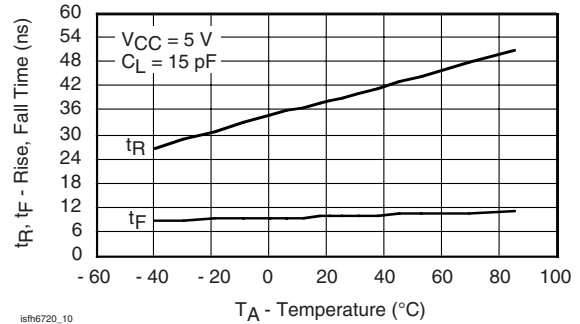


Figure 10. Rise and Fall Time vs. Ambient Temperature

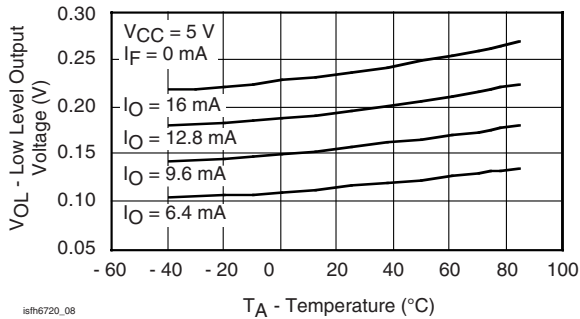


Figure 8. Typical Low Level Output Voltage vs. Temperature

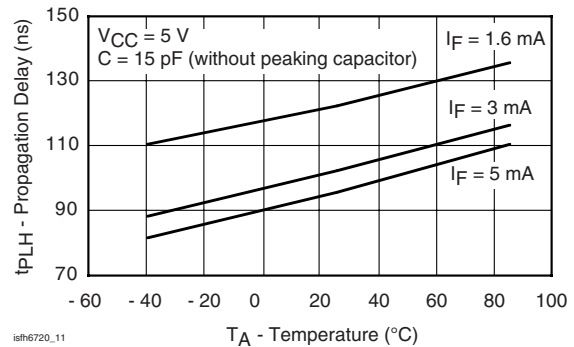


Figure 11. Typical Propagation Delays to Logic High vs. Temperature

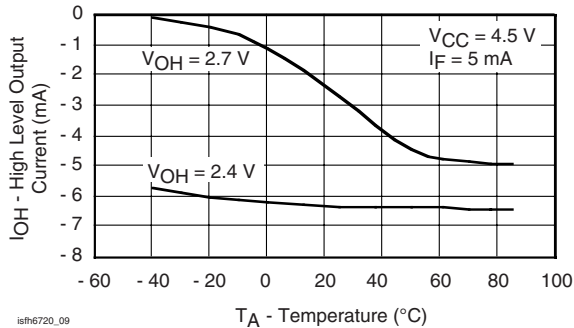


Figure 9. Typical High Level Output Current vs. Temperature

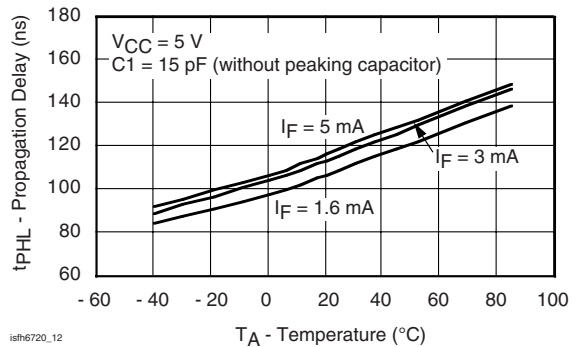


Figure 12. Typical Propagation Delays to Logic Low vs. Temperature

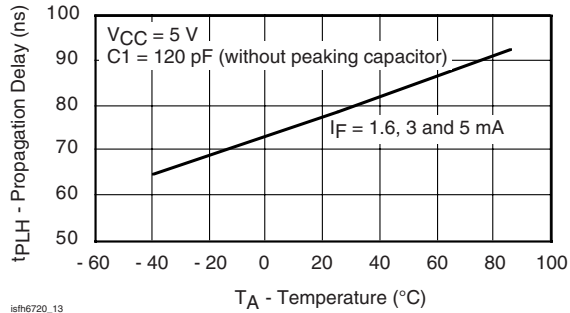


Figure 13. Typical Propagation Delays to Logic High vs. Temperature

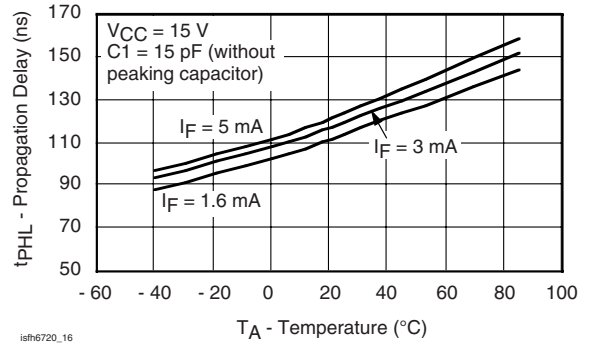


Figure 16. Typical Propagation Delays to Logic Low vs. Temperature

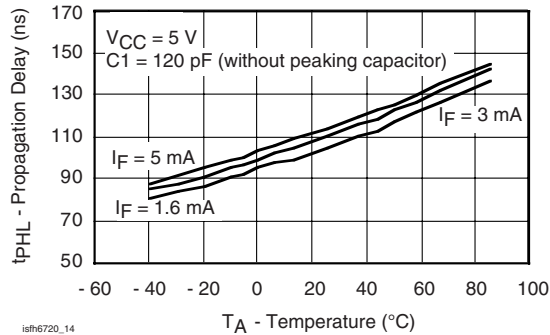


Figure 14. Typical Propagation Delays to Logic Low vs. Temperature

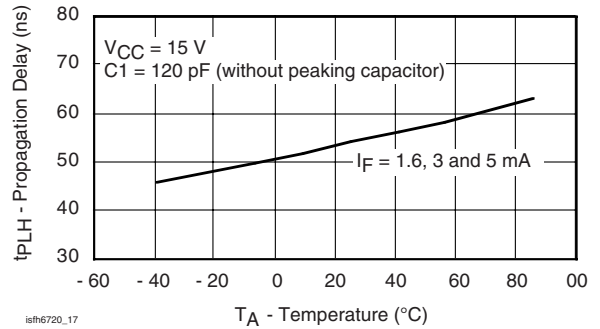


Figure 17. Typical Propagation Delays to Logic High vs. Temperature

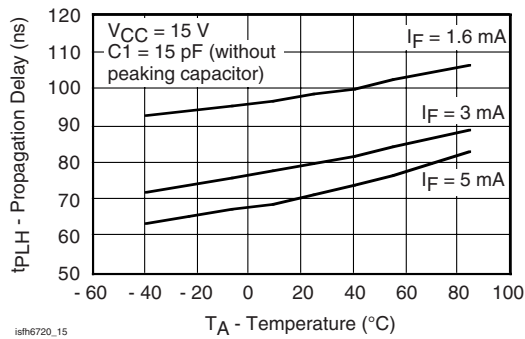


Figure 15. Typical Propagation Delays to Logic High vs. Temperature

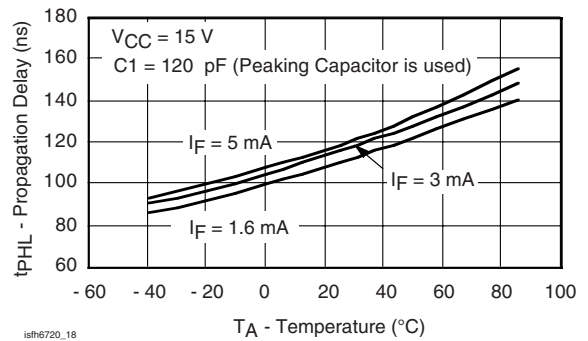


Figure 18. Typical Propagation Delays to Logic Low vs. Temperature

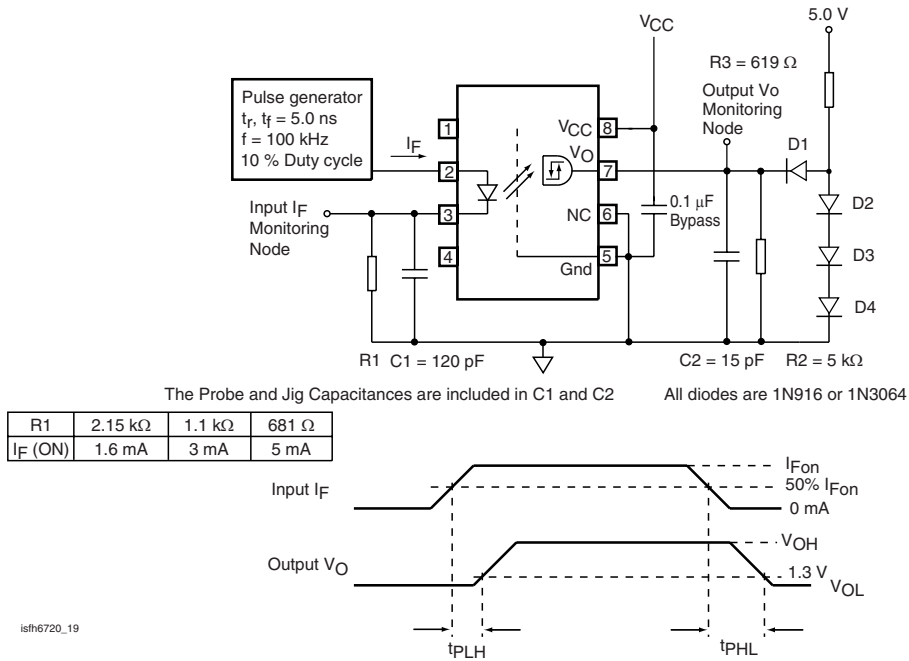


Figure 19. Test Circuit for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_r$  and  $t_f$

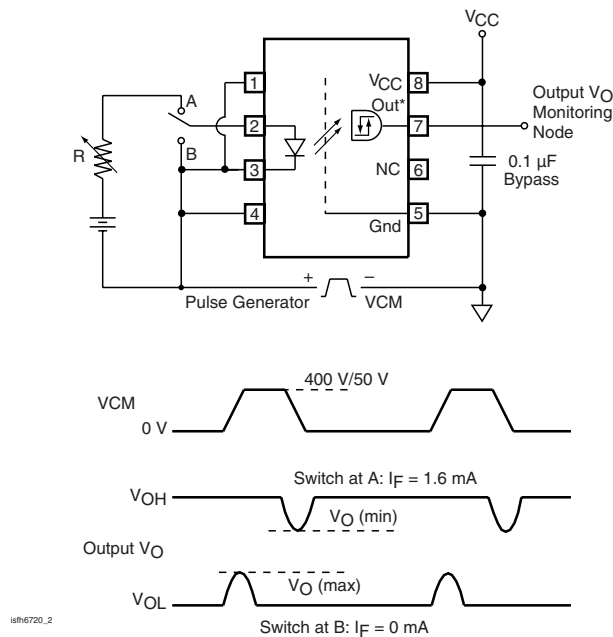
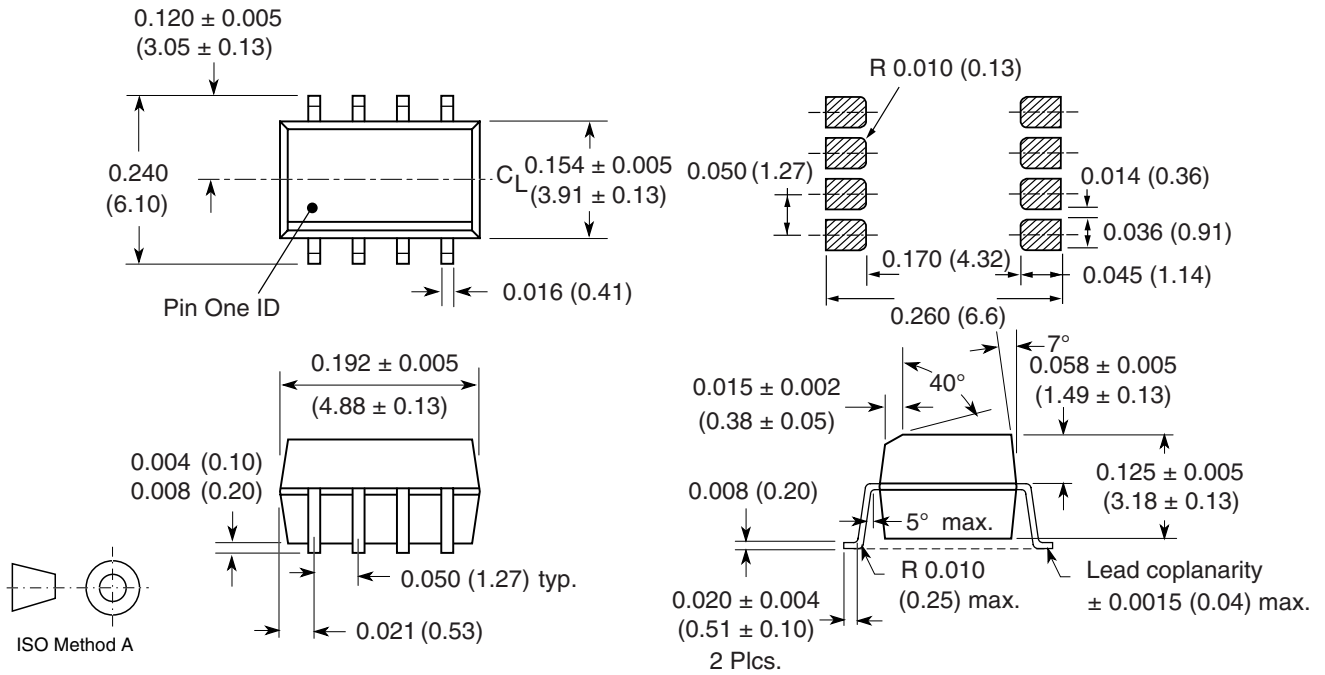


Figure 20. Test Circuit for Common Mode Transient Immunity and Typical Waveforms





**PACKAGE DIMENSIONS** in inches (millimeters)



i178003

### Ozone Depleting Substances Policy Statement

It is the policy of Vishay Semiconductor GmbH to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Vishay Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Vishay Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

We reserve the right to make changes to improve technical design  
and may do so without further notice.

Parameters can vary in different applications. All operating parameters must be validated for each customer application by the customer. Should the buyer use Vishay Semiconductors products for any unintended or unauthorized application, the buyer shall indemnify Vishay Semiconductors against all claims, costs, damages, and expenses, arising out of, directly or indirectly, any claim of personal damage, injury or death associated with such unintended or unauthorized use.

Vishay Semiconductor GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany



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