300mA, Low Iq, LDO with foldback current

Features

- Low Dropout Voltage:
  - 170mV at 200mA
  - 230mV at 300mA
- Maximum Output Current: 300mA
- Input Voltage Range: 2.1V to 5.5V
- ±2% Accuracy Overall Operating Conditions
- Low Quiescent and Shutdown Current
- Foldback Current Limit and Overheat Protection
- Stable with Effective Capacitance of 1 μF
- Soft-start Limits Input Current Surge During Enable
- Available in Fixed-Output Voltages 1.8V/2.8V/3.0V/3.3V
- Temperature range: −40°C ~ +85°C
- Available in 3-mm × 3-mm SOT23-5 package and SC70-5 package

Applications

- POS
- Handheld Devices Including Medical Handhelds
- U-Key
- Lower Cost Industrial and Instrumentation
- Battery Device

Description

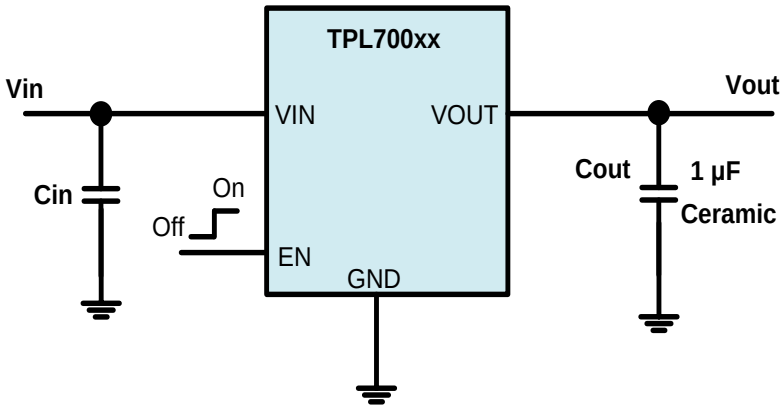
TPL700 series product is a high performance and low dropout linear regulator. Current output capability is 300mA. TPL700 series product support low quiescent current and high-PSRR, especially for high frequency. TPL700 series can be stable with output capacitance of 1μF to 10μF with ESR of up to 100mΩ.

The TPL700 series have a high PSRR at high frequency and PSRR can be about 70dB at 2M frequency point. This feature makes TPL700 series very suitable for power-sensitive applications with high noise from front stage power supply. When coupled with a no load quiescent current of 35μA (typical) and 0.1μA shutdown current, the TPL700 series is an ideal choice for portable or wireless equipment. Current-limit and thermal overload protection circuits prevent damage under these conditions. The TPL700 series also includes an internal pull-down resistor on the EN input.

The TPL700 series comes in many fixed voltage options with ±2% output voltage accuracy over temperature, line and load. Other output voltage options are available on request.

The TPL700 series is guaranteed over the temperature range of -40°C to +85°C. The TPL700 series of LDOs are available in 3-mm*3-mm SOT23-5 package and SC70-5 package.

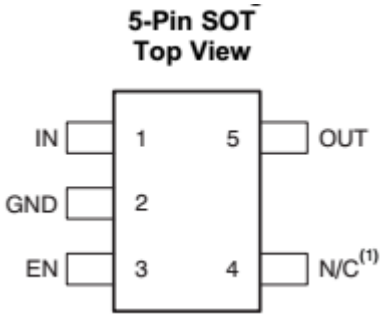
Typical Application Circuit

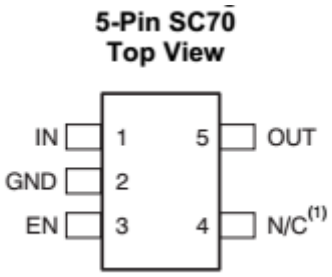


Absolute Maximum Ratings*

		Min	Max	Unit
Voltage	Vin	-0.3	7	V
	Ven	-0.3	7	V
	Vout	-0.3	7	V
Maximum output current	Iout	Internal limited		mA
Temperature	Operating junction, TJ	-55	150	℃
	Storage, Tstg	-55	150	℃

Pin Configuration (Top View)





PIN				I/O	Description
Name	SOT	DFN	SC70-5		
IN	1	4	1	I	Input voltage pin. Bypass V_{IN} to GND with a 1μF or greater capacitor.
OUT	5	1	5	O	Regulated output voltage. Bypass V_{OUT} to GND with a 1μF or greater capacitor.
EN	3	3	3	I	Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to V_{IN}.
NC	4	-	4	-	No connection. This pin can be tied to ground to improve thermal dissipation.
GND	2	2	2	-	GND is the connection to system ground. Connect to PCB Ground plane

ESD Rating

		Value	Units
V(ESD) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins	+/-8000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, V all pins(	+/-2000	V

Recommended Operating Conditions

	Min	Nom	Max	Units
Vin	2.1		5.5	V
Iout	0		300	mA

Thermal Information

THERMAL METRIC	TPL700	Unit
	SOT23-5	
RθJA Junction-to-ambient thermal resistance	280	°C/W
RθJC(top) Junction-to-case (top) thermal resistance	61.9	
RθJB Junction-to-board thermal resistance	54	
ψJT Junction-to-top characterization parameter	0.8	
ψJB Junction-to-board characterization parameter	53.4	
RθJC(bot) Junction-to-case (bottom) thermal resistance	n/a	

Order information

Model Name	Class	V_O	Order Number**	Package	Transport Media, Quantity	Marking Information
TPL700	Fixed	1.8V	TPL700F18-TR	SOT23-5	Tape and Reel, 3,000	L1F
TPL700	Fixed	2.8V	TPL700F28-TR	SOT23-5	Tape and Reel, 3,000	L1H
TPL700	Fixed	3.0V	TPL700F30-TR	SOT23-5	Tape and Reel, 3,000	L1I
TPL700	Fixed	3.3V	TPL700F33-TR	SOT23-5	Tape and Reel, 3,000	L1J
TPL700	Fixed	3.3V	TPL700F33-CR	SOC70-5	Tape and Reel, 3,000	L1J

Electrical Characteristics

At VIN = VOUT (Typ) + 0.3 V or 2.0 V (whichever is greater); IOUT = 10 mA, VEN = 0.9 V, COUT = 1.0 µF, and TJ = –40°C to +125°C, unless otherwise noted. Typical values are at TJ = +25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range		2.1		5.5	V
V_O	DC output accuracy	–40°C ≤ T_J ≤ +125°C	-2		+2	%
$\Delta V_{IN}/\Delta V_{OUT}$	Line Regulation	$V_{OUT(NOM)}$ + 0.3 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 10 mA		1.5		mV
$\Delta V_{IN}/\Delta I_{OUT}$	Load Regulation	0 mA ≤ I_{OUT} ≤ 300 mA		1	15	mV
ΔV_{DO}	Dropout Voltage (Note 2)	Vin = Vout(nom), Iout = 100 mA,		88		mV
		Vin = Vout (nom), Iout = 200 mA		170		mV
		Vin = Vout (nom), Iout = 300 mA		230		mV
I_{CL}	Output Current Limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$		500		mA
I_{SHDN}	Shutdown Current	V_{EN} ≤ 0.4 V, V_{IN} = 2.0 V		400		nA
		V_{EN} ≤ 0.4 V, 2.0 V ≤ V_{IN} ≤ 4.5 V		1		µA
I_{GND}	Quiescent Current	I_{OUT} = 0mA		35		µA
		I_{OUT} = 300 mA, V_{IN} = V_{OUT} + 0.5 V		1000		µA
PSRR	Power Supply Rejection Ratio	V_{IN} = 4.3 V, V_{OUT} = 3.3 V, I_{OUT} = 10 mA, f = 1KHz		55		dB
t_{STR}	Startup time (Note 3)	C_{OUT} = 1.0 µF, I_{OUT} = 300mA		100		µS
$V_{EN(HI)}$	Enable pin high (enabled)		0.6		V_{IN}	V
$V_{EN(LO)}$	Enable pin low (disabled)		0		0.45	V
I_{EN}	Enable pin current	V_{IN} = V_{EN} = 5.5 V		0.03		µA
UVLO	Under voltage lockout	V_{IN} rising		1.9		V
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		170		°C
T_J	Operating junction temperature	Reset, temperature decreasing		145		°C
			-40		+125	°C

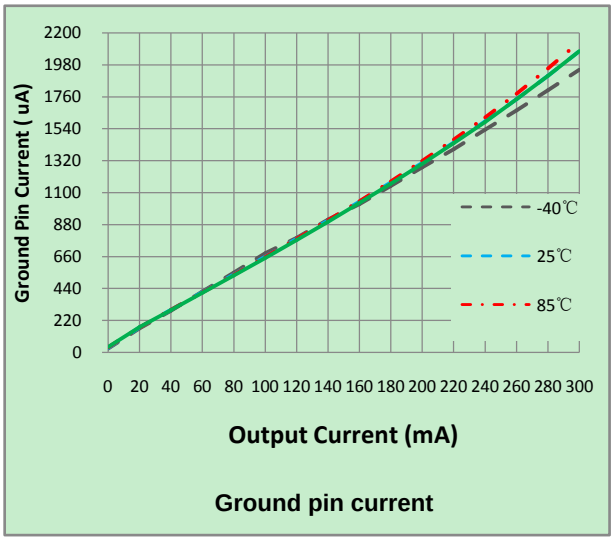
Note 1: The TPL700 series regulators are tested and specified under pulse load conditions such that TJ ≈ TA. The TPL700 series is 100% production tested at TA = 25°C. Performance at -40°C and 125°C is assured by design, characterization and correlation with statistical process controls.

Note 2: Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage will be equal to: VIN – Vdropout.

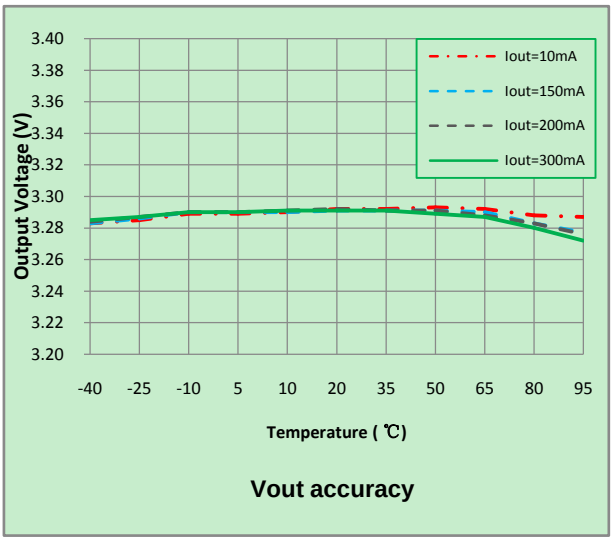
Note 3: Startup time = time from EN assertion to 0.98 × VOUT (NOM)

Typical Characteristics

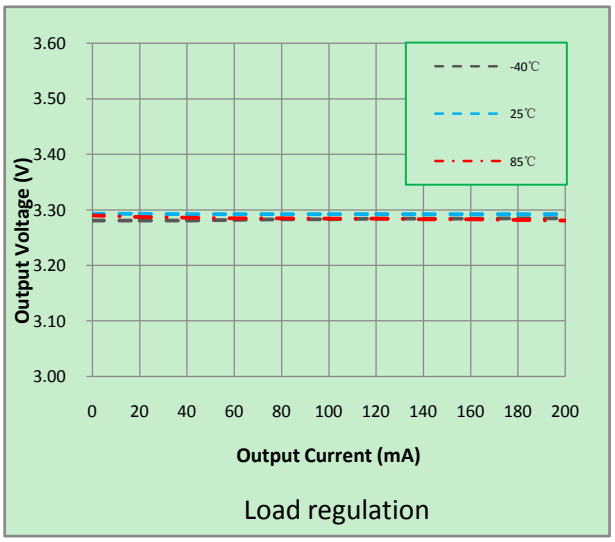
Over operating temperature range (TJ = –40°C to +125°C), VIN = VOUT (nom) + 0.5 V or 2 V, whichever is greater; IOUT = 10 mA,VEN = VIN, COUT = 1 µF, unless otherwise noted. Typical values are at TJ = 25°C



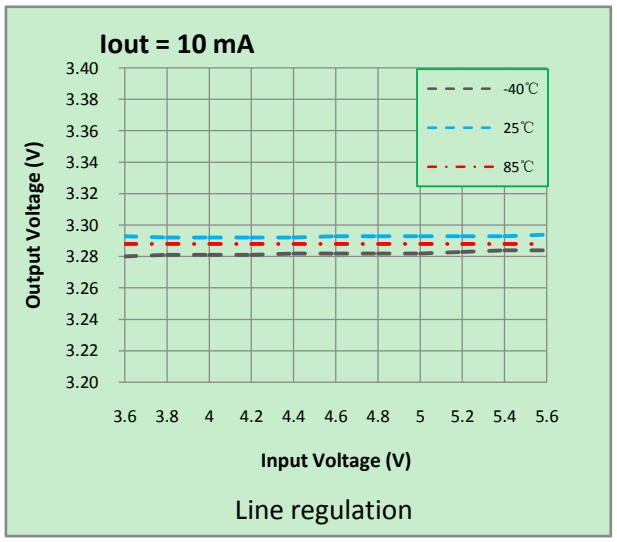
Ground pin current



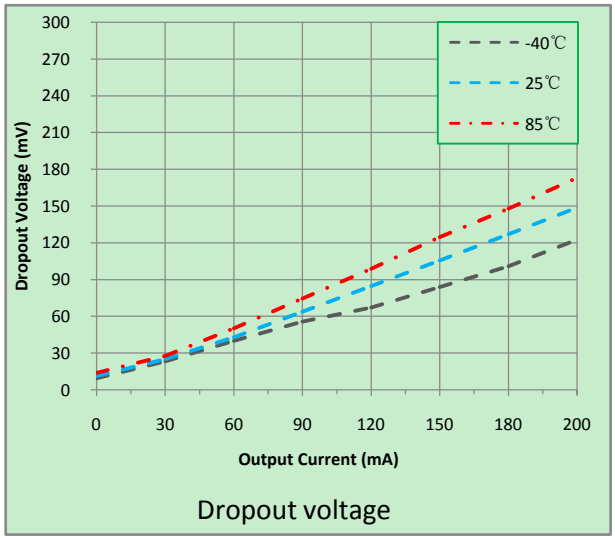
Vout accuracy



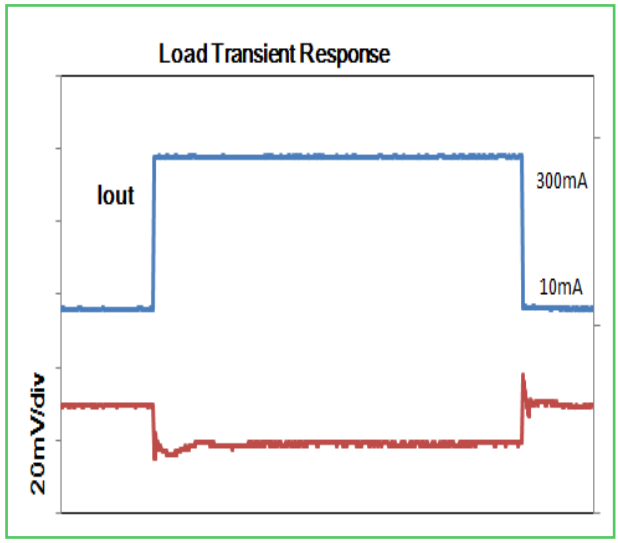
Load regulation



Line regulation



Dropout voltage



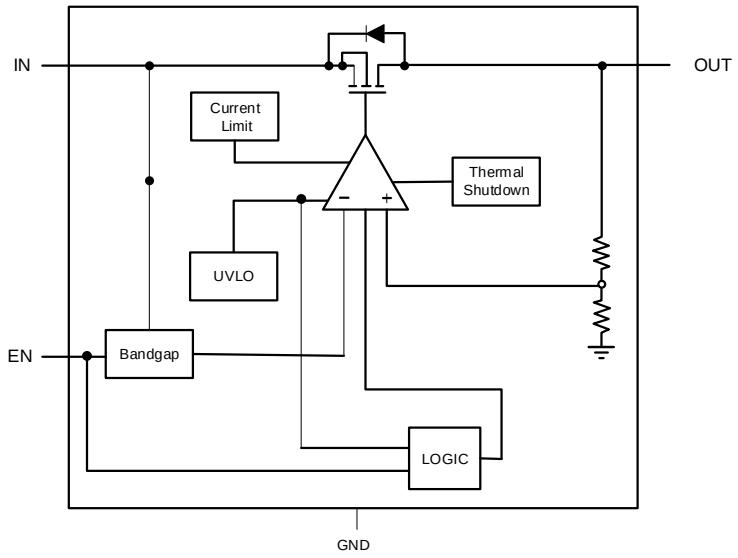
Overview

The TPL700 series is a high PSRR, low quiescent current, low dropout linear regulator that operates from 2.1 V to 5.5 V and can provide up to 300mA output current. The TPL700 series consumes a low 35μA of quiescent current (typical). Shutdown current consumption is typically 0.1μA.

Internally, the TPL700 series consists of a reference, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to pass and decreasing the output voltage.

The TPL700 series is available in all output voltage options, ranging from 0.8 V to 5.0 V

Functional block diagram



Features description

Enable Feature

The enable pin (EN) is active high. The device is enabled when the voltage at the EN pin goes above 0.6V. This relatively lower voltage value required to turn the LDO on can be exploited to power the LDO with a GPIO of recent processors whose GPIO logic 1 voltage level is lower than traditional microcontrollers. The device is turned off when the EN pin is held at less than 0.4V. When shutdown capability is not required, EN can be connected to the IN pin.

Current Limit Protection

The TPL700 series has an internal foldback current limit that helps to protect the regulator during fault conditions. The current supplied by the device is gradually throttled down as the output voltage decreases. When the output is shorted, the LDO supplies a typical current of 90 mA. Output voltage is not regulated when the device is in current limit, and is VOUT = ILIMIT × RLOAD. The advantage of foldback current limit is that the ILIMIT value is less than the fixed current limit. Therefore, the power that the PMOS pass transistor dissipates [(VIN – VOUT) × ILIMIT] is much less.

The TPL700 series PMOS pass element has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

Output Capacitance and Transient Response

The TPL700 series is designed for operation with small, space-saving ceramic capacitors, but it can function with most commonly used capacitors as long as care is taken with regard to the effective series resistance (ESR) value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 1μF capacitance with an ESR of 100 mΩ or less is recommended to ensure the stability of the TPL700 series. For output voltage stable, we high recommend that the output capacitance should be near to the voltage output pin.Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the TPL700 series to large changes in load current.

Under voltage Lockout (UVLO)

The TPL700 series uses an under voltage lockout circuit (UVLO = 1.9 V) to keep the output shut off until the internal circuitry operates properly.

Input Bypass Capacitor

Connecting a 1μF capacitor from VIN to GND reduces the circuit sensitivity to the PCB layout, especially when long input traces or high source impedance are encountered. If output capacitance greater than 1μF is required, the input capacitor should be increased to match it.

Thermal Fault Protection

In the event that the die temperature exceeds typically +170°C, the output of the LDO will shut down until the die temperature cools down to typically +145°C, the output circuitry is again enabled. The level of power dissipated, combined with the ambient temperature and the thermal impedance of the package, will determine if the junction temperature exceeds the thermal shutdown temperature. Also see the section on “Power Dissipation”.

Power Dissipation

The junction temperature must not exceed the range specified in “Recommended Operating Conditions” on page 3. The power dissipation can be calculated using below Equation:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND}$$

The maximum allowable junction temperature, TJ(MAX) and the maximum expected ambient temperature, TA(MAX) will determine the maximum allowable junction temperature rise (ΔTJ), as shown in below Equation:

$$\Delta T_J = T_{J(MAX)} - T_{A(MAX)}$$

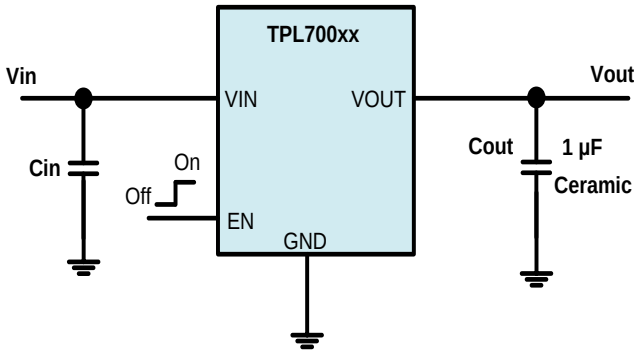
To calculate the maximum ambient operating temperature, use the junction-to-ambient thermal resistance (θJA), as shown in below Equation:

$$T_{J(MAX)} = P_{D(MAX)} \times \theta_{JA} + T_A$$

Application and Implementation

NOTE Information in the following applications sections is not part of the 3peak's component specification and 3peak does not warrant its accuracy or completeness. 3peak's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Typical Application Circuit



The input and output capcitance requirement 3peak recommends using 1µF X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature. However, the TPL700 series is designed to be stable with an effective capacitance of 1µF or larger at the output. Thus, the device is stable with capacitors of other dielectric types as well, as long as the effective capacitance under operating bias voltage and temperature is greater than 1µF. This effective capacitance refers to the capacitance that the LDO sees under operating bias voltage and temperature conditions; that is, the capacitance after taking both bias voltage and temperature derating into consideration. In addition to allowing the use of cheaper dielectrics, this capability of being stable with 1µF effective capacitance also enables the use of smaller footprint capacitors that have higher derating in size- and space-constrained applications.

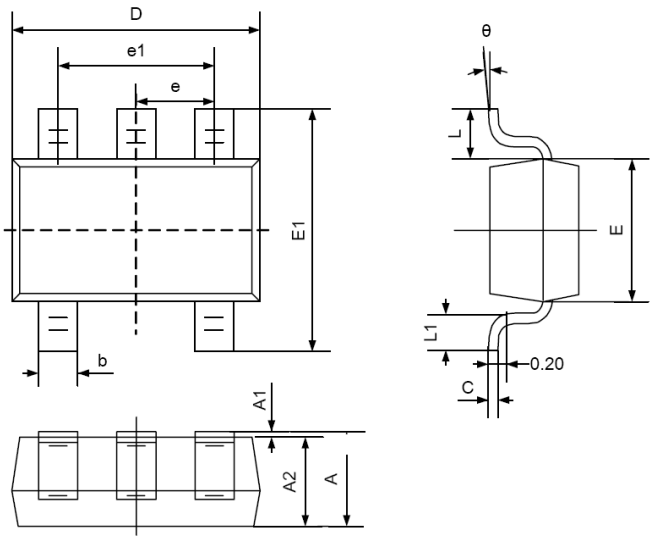
Using a 1µF rated capacitor at the output of the LDO does not ensure stability because the effective capacitance under the specified operating conditions must not be less than 1µF. Maximum ESR should be less than 100 mΩ.

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1µF to 10µF, low ESR capacitor across the IN pin and GND in of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2Ω, a 1µF input capacitor may be necessary to ensure stability.

Layout requirement

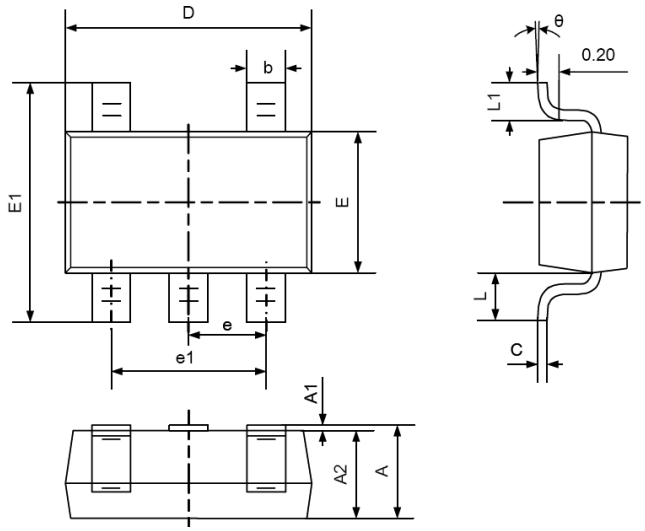
Input and output capacitors should be placed as close to the device pins as possible. To improve AC performance such as PSRR, output noise, and transient response, 3peak recommends designing the printed-circuit boards with separate ground planes for VIN and VOUT, with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should be connected directly to the GND pin of the device. High ESR capacitors may degrade PSRR performance.

Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
C	0.080	0.150	0.003	0.006
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650TYP		0.026TYP	
e1	1.200	1.400	0.047	0.055
L	0.525REF		0.021REF	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

SC70-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
C	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.460	0.012	0.024
θ	0°	8°	0°	8°

SOT23-5