HM-65162

2K x 8 Asynchronous CMOS Static RAM

March 1997

Features

- **Fast Access Time. . . . . 70/90ns Max**
- **Low Standby Current. . . . . .50µA Max**
- **Low Operating Current . . . . . 70mA Max**
- **Data Retention at 2.0V. . . . . .20µA Max**
- **TTL Compatible Inputs and Outputs**
- **JEDEC Approved Pinout (2716, 6116 Type)**
- **No Clocks or Strobes Required**
- **Equal Cycle and Access Time**
- **Single 5V Supply**
- **Gated Inputs**
- **No Pull-Up or Pull-Down Resistors Required**

Description

The HM-65162 is a CMOS 2048 x 8 Static Random Access Memory manufactured using the Intersil Advanced SAJI V process. The device utilizes asynchronous circuit design for fast cycle time and ease of use. The pinout is the JEDEC 24 pin DIP, and 32 pad 8-bit wide standard which allows easy memory board layouts flexible to accommodate a variety of industry standard PROMs, RAMs, ROMs and EPROMs. The HM-65162 is ideally suited for use in microprocessor based systems with its 8-bit word length organization. The convenient output enable also simplifies the bus interface by allowing the data outputs to be controlled independent of the chip enable. Gated inputs lower operating current and also eliminate the need for pull-up or pull-down resistors.

Ordering Information

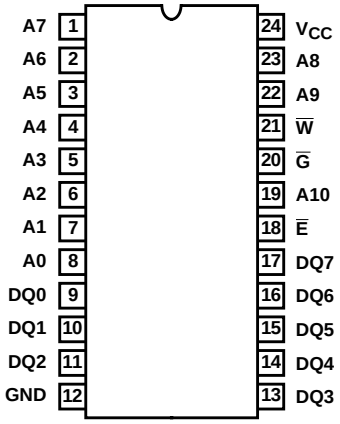
PACKAGE	TEMP. RANGE	**70ns/20µA** (NOTE 1)	**90ns/40µA** (NOTE 1)	**90ns/300µA** (NOTE 1)	PKG. NO.
CERDIP	-40°C to +85°C	HM1-65162B-9	HM1-65162-9	HM1-65162C-9	F24.6
JAN#	-55°C to +125°C	29110BJA	29104BJA	-	F24.6
SMD#	-55°C to +125°C	8403606JA	8403602JA	8403603JA	F24.6
CLCC	-40°C to +85°C	HM4-65162B-9	HM4-65162-9	HM4-65162C-9	J32.A
SMD#	-55°C to 125°C	8403606ZA	8403602ZA	8403603ZA	J32.A

NOTE:

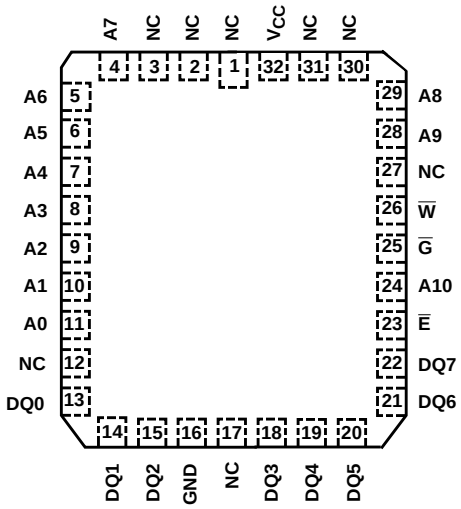
1. Access time/data retention supply current.

Pinouts

HM-65162 (CERDIP)
TOP VIEW

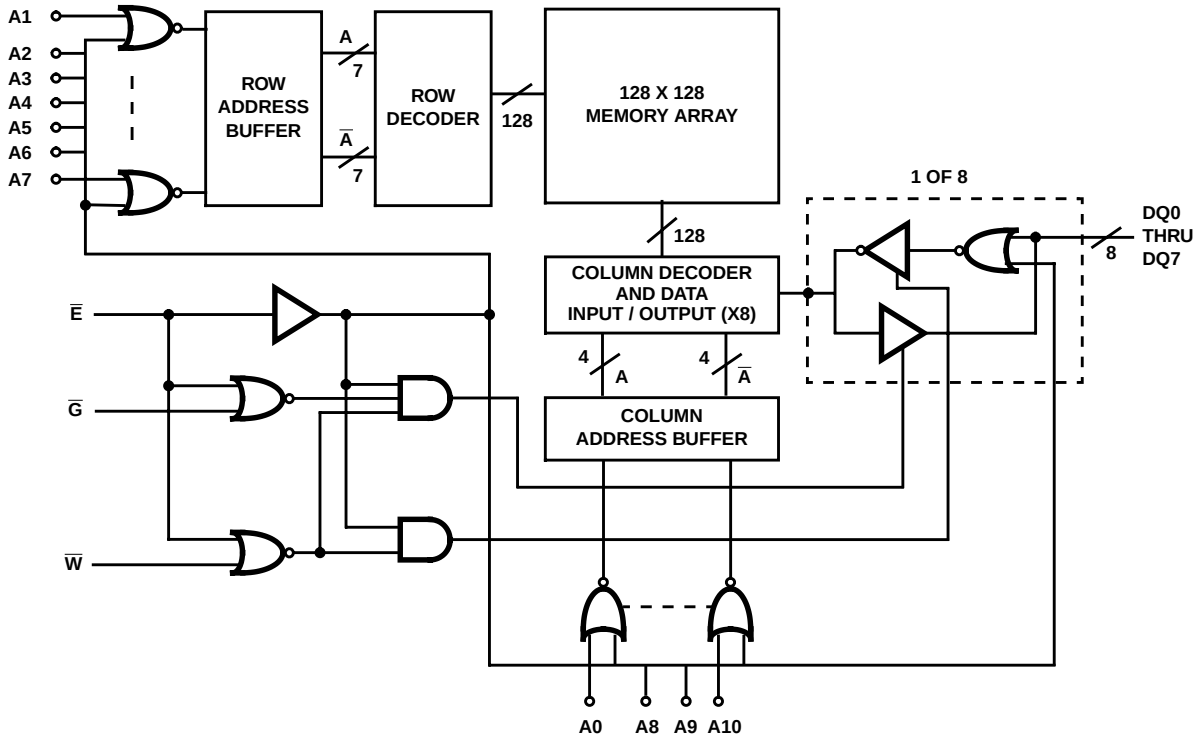


HM-65162 (CLCC)
TOP VIEW



PIN	DESCRIPTION
NC	No Connect
A0 - A10	Address Input
$\overline{E}$	Chip Enable/Power Down
V_{SS}/GND	Ground
DQ0 - DQ7	Data In/Data Out
V_{CC}	Power (+5V)
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable

Functional Diagram



Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to V_{CC} +0.3V
Typical Derating Factor . . . . . 05mA/MHz Increase in ICCOP
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
HM-65162S-9, HM-65162B-9,
HM-65162-9, HM65162C-9. . . . . -40^oC to $+85^oC$

Thermal Information

Thermal Resistance	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	48	8
CLCC Package	66	12

Maximum Storage Temperature Range . . . . . -65^oC to $+150^oC$
Maximum Junction Temperature. . . . . $+175^oC$
Maximum Lead Temperature (Soldering 10s). . . . . $+300^oC$

Die Characteristics

Gate Count . . . . . 26000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications V_{CC} = 5V ±10%; T_A = -40^oC to $+85^oC$ (HM-65162S-9, HM-65162B-9, HM-65162-9, HM-65162C-9)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
ICCSB1	Standby Supply Current	-	50	µA	HM-65162B-9, IO = 0mA, $\overline{E}$ = V_{CC} - 0.3V, V_{CC} = 5.5V
		-	100	µA	HM-65162S-9, HM65162-9, IO = 0mA, $\overline{E}$ = V_{CC} - 0.3V, V_{CC} = 5.5V
		-	900	µA	HM-65162C-9, IO = 0mA, $\overline{E}$ = V_{CC} - 0.3V, V_{CC} = 5.5V
ICCSB	Standby Supply Current	-	8	mA	$\overline{E}$ = 2.2V, IO = 0mA, V_{CC} = 5.5V
ICCEN	Enabled Supply Current	-	70	mA	$\overline{E}$ = 0.8V, IO = 0mA, V_{CC} = 5.5V
ICCOP	Operating Supply Current (Note 1)	-	70	mA	$\overline{E}$ = 0.8V, IO = 0mA, f = 1MHz, V_{CC} = 5.5V
ICCDR	Data Retention Supply Current	-	20	µA	HM-65162B-9, IO = 0mA, V_{CC} = 2.0V, $\overline{E}$ = VCC - 0.3V
		-	40	µA	HM-65162S-9, HM-65162-9, IO = 0mA, V_{CC} = 2.0V, $\overline{E}$ = V_{CC} - 0.3V
		-	300	µA	HM-65162C-9, IO = 0mA, V_{CC} = 2.0V, $\overline{E}$ = V_{CC} - 0.3V
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = V_{CC} or GND, V_{CC} = 5.5V
IIOZ	Input/Output Leakage Current	-1.0	+1.0	µA	VIO = V_{CC} or GND, V_{CC} = 5.5V
V_{IL}	Input Low Voltage	-0.3	0.8	V	V_{CC} = 4.5V
V_{IH}	Input High Voltage	2.2	V_{CC} +0.3	V	V_{CC} = 5.5V
VOL	Output Low Voltage	-	0.4	V	IO = 4.0mA, V_{CC} = 4.5V
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA, V_{CC} = 4.5V
VOH2	Output High Voltage (Note 2)	V_{CC} -0.4	-	V	IO = -100µA, V_{CC} = 4.5V

Capacitance T_A = $+25^oC$

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	10	pF	f = 1MHz, All measurements are referenced to device GND
CIO	Input/Output Capacitance (Note 2)	12	pF	

NOTES:

1. Typical derating 5mA/MHz increase in ICCOP.
2. Tested at initial design and after major design changes.

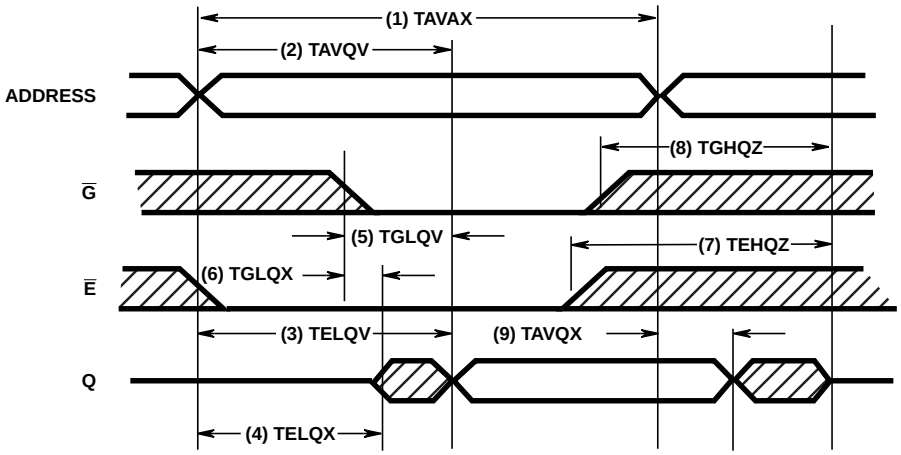
AC Electrical Specifications V_{CC} = 5V ±10%, T_A = -40°C to +85°C (HM-65162S-9, HM-65162B-9, HM65162-9, HM-65162C-9)

SYMBOL	PARAMETER	LIMITS								UNITS	CONDITIONS
		HM-65162S-9		HM-65162B-9		HM-65162-9		HM-65162C-9			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ CYCLE											
(1) TAVAX	Read Cycle Time	55	-	70	-	90	-	90	-	ns	(Notes 1, 3)
(2) TAVQV	Address Access Time	-	55	-	70	-	90	-	90	ns	(Notes 1, 3, 4)
(3) TELQV	Chip Enable Access Time	-	55	-	70	-	90	-	90	ns	(Notes 1, 3)
(4) TELQX	Chip Enable Output Enable Time	5	-	5	-	5	-	5	-	ns	(Notes 2, 3)
(5) TGLQV	Output Enable Access Time	-	35	-	50	-	65	-	65	ns	(Notes 1, 3)
(6) TGLQX	Output Enable Output Enable Time	5	-	5	-	5	-	5	-	ns	(Notes 2, 3)
(7) TEHQZ	Chip Enable Output Disable Time	-	35	-	35	-	50	-	50	ns	(Notes 2, 3)
(8) TGHQZ	Output Enable Output Disable Time	-	30	-	35	-	40	-	40	ns	(Notes 2, 3)
(9) TAVQX	Output Hold From Address Change	5	-	5	-	5	-	5	-	ns	(Notes 1, 3)
WRITE CYCLE											
(10) TAVAX	Write Cycle Time	55	-	70	-	90	-	90	-	ns	(Notes 1, 3)
(11) TELWH	Chip Selection to End of Write	45	-	45	-	55	-	55	-	ns	(Notes 1, 3)
(12) TAVWL	Address Setup Time	5	-	10	-	10	-	10	-	ns	(Notes 1, 3)
(13) TWLWH	Write Enable Pulse Width	40	-	40	-	55	-	55	-	ns	(Notes 1, 3)
(14) TWHAX	Write Enable Read Setup Time	10	-	10	-	10	-	10	-	ns	(Notes 1, 3)
(15) TGHQZ	Output Enable Output Disable Time	-	30	-	35	-	40	-	40	ns	(Notes 2, 3)
(16) TWLQZ	Write Enable Output Disable Time	-	30	-	40	-	50	-	50	ns	(Notes 2, 3)
(17) TDVWH	Data Setup Time	25	-	30	-	30	-	30	-	ns	(Notes 1, 3)
(18) TWHDX	Data Hold Time	10	-	10	-	15	-	15	-	ns	(Notes 1, 3)
(19) TWHQX	Write Enable Output Enable Time	0	-	0	-	0	-	0	-	ns	(Notes 1, 3)
(20) TWLEH	Write Enable Pulse Setup Time	45	-	40	-	55	-	55	-	ns	(Notes 1, 3)
(21) TDVEH	Chip Enable Data Setup Time	25	-	30	-	30	-	30	-	ns	(Notes 1, 3)
(22) TAVWH	Address Valid to End of Write	45	-	50	-	65	-	65	-	ns	(Notes 1, 3)

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent and C_L = 50pF (min) - for C_L greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. V_{CC} = 4.5 and 5.5V.
4. TAVQV = TELQV + TAVEL.

Timing Waveforms

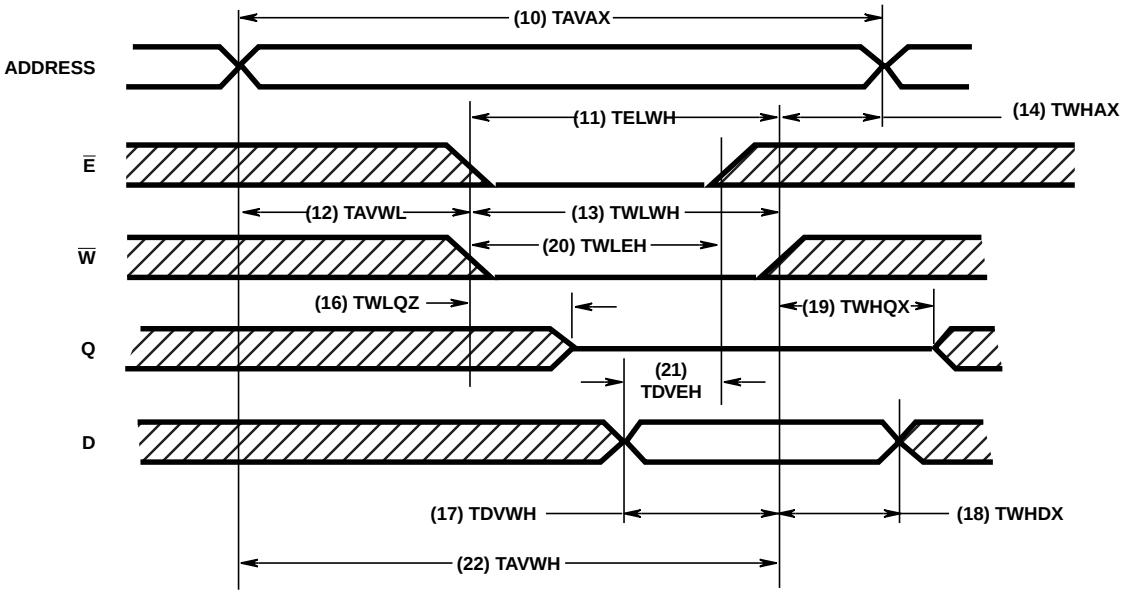


NOTE:

1. $\overline{W}$ is high for a Read Cycle.

FIGURE 1. READ CYCLE

Addresses must remain stable for the duration of the read cycle. To read, $\overline{G}$ and $\overline{E}$ must be $\leq V_{IL}$ and $\overline{W} \geq V_{IH}$. The output buffers can be controlled independently by $\overline{G}$ while $\overline{E}$ is low. To execute consecutive read cycles, $\overline{E}$ may be tied low continuously until all desired locations are accessed. When $\overline{E}$ is low, addresses must be driven by stable logic levels and must not be in the high impedance state.



NOTE:

1. $\overline{G}$ is low throughout Write Cycle.

FIGURE 2. WRITE CYCLE I

To write, addresses must be stable, $\overline{E}$ low and $\overline{W}$ falling low for a period no shorter than TWLWH. Data in is referenced with the rising edge of $\overline{W}$, (TDVWH and TWHDX). While addresses are changing, $\overline{W}$ must be high. When $\overline{W}$ falls low, the I/O pins are still in the output state for a period of TWLQZ and input data of the opposite phase to the outputs must not be applied, (Bus contention). If $\overline{E}$ transitions low simultaneously with the $\overline{W}$ line transitioning low, or after the $\overline{W}$ transition, the output will remain in a high impedance state. $\overline{G}$ is held continuously low.

Timing Waveforms (Continued)

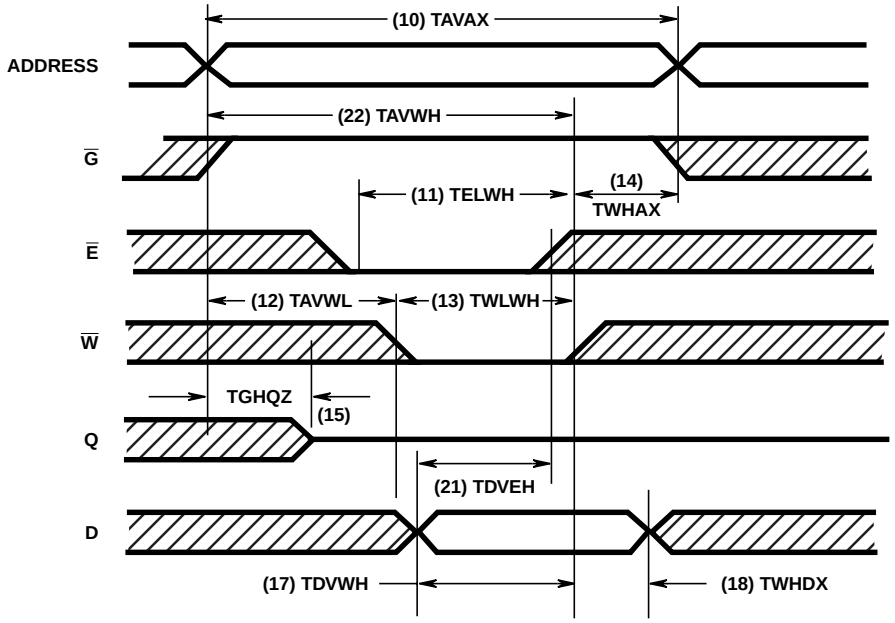


FIGURE 3. WRITE CYCLE II

In this write cycle $\overline{G}$ has control of the output after a period, TGHQZ. $\overline{G}$ switching the output to a high impedance state allows data in to be applied without bus contention after TGHQZ. When $\overline{W}$ transitions high, the data in can change after TWHDX to complete the write cycle.

Low Voltage Data Retention

Intersil CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules ensure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within V_{CC} -0.3V to V_{CC} +0.3V.
2. On RAMs which have selects or output enables (e.g., S, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. Inputs which are to be held high (e.g., $\overline{E}$) must be kept between V_{CC} +0.3V and 70% of V_{CC} during the power up and down transitions.
4. The RAM can begin operation > 55ns after V_{CC} reaches the minimum operating voltage (4.5V).

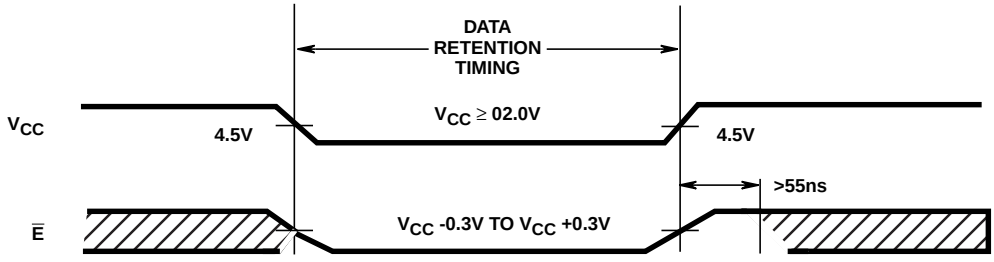


FIGURE 4. DATA RETENTION TIMING

Typical Performance Curve

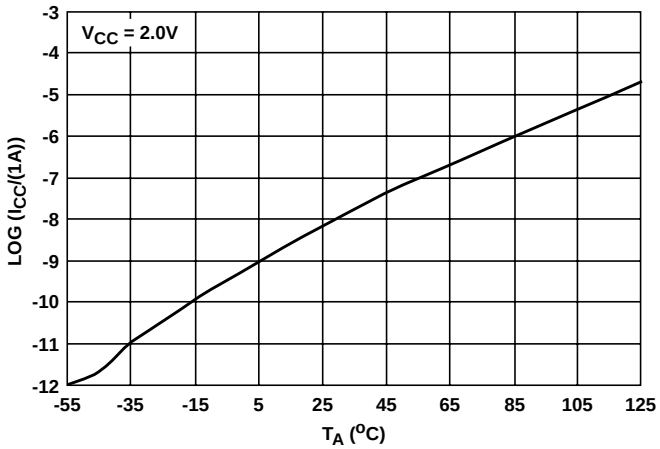


FIGURE 5. TYPICAL ICCDR vs T_A

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