



2.5V Wide Range Frequency Clock Driver (33MHz - 233MHz)

Recommended Application:

- DDR Memory Modules / Zero Delay Board Fan Out
- Provides complete DDR DIMM logic solution with ICSSTV16857, ICSSTV16859 or ICSSTV32852

Product Description/Features:

- Low skew, low jitter PLL clock driver
- 1 to 10 differential clock distribution (SSTL_2)
- Feedback pins for input to output synchronization
- PD# for power management
- Spread Spectrum tolerant inputs
- Auto PD when input signal removed
- Choice of static phase offset available, for easy board tuning;

-XXX = device pattern number for options listed below.

- ICS93V857-025 0ps
- ICS93V857-125 +125ps
- ICS93V857-130 .. +40ps

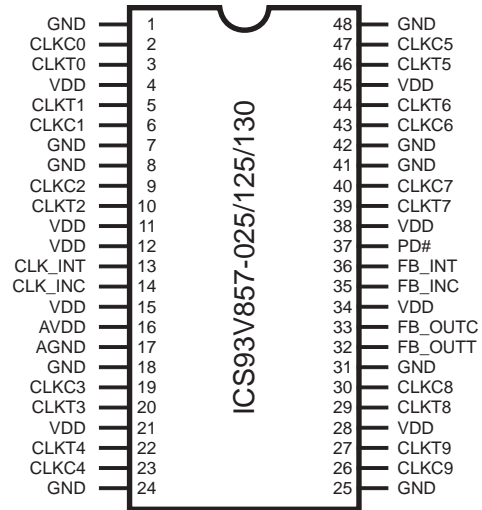
Switching Characteristics:

- Period jitter (>66MHz): <40ps
- CYCLE - CYCLE jitter (66MHz): <120ps
- CYCLE - CYCLE jitter (>100MHz): <65ps
- OUTPUT - OUTPUT skew: <60ps
- Output Rise and Fall Time: 650ps - 950ps
- DUTY CYCLE: 49.5% - 50.5%

Functionality

INPUTS				OUTPUTS				PLL State
AVDD	PD#	CLK_INT	CLK_INC	CLKT	CLKC	FB_OUTT	FB_OUTC	
GND	H	L	H	L	H	L	H	Bypassed/off
GND	H	H	L	H	L	H	L	Bypassed/off
2.5V (nom)	L	L	H	Z	Z	Z	Z	off
2.5V (nom)	L	H	L	Z	Z	Z	Z	off
2.5V (nom)	H	L	H	L	H	L	H	on
2.5V (nom)	H	H	L	H	L	H	L	on
2.5V (nom)	X	<20MHz ⁽¹⁾		Z	Z	Z	Z	off

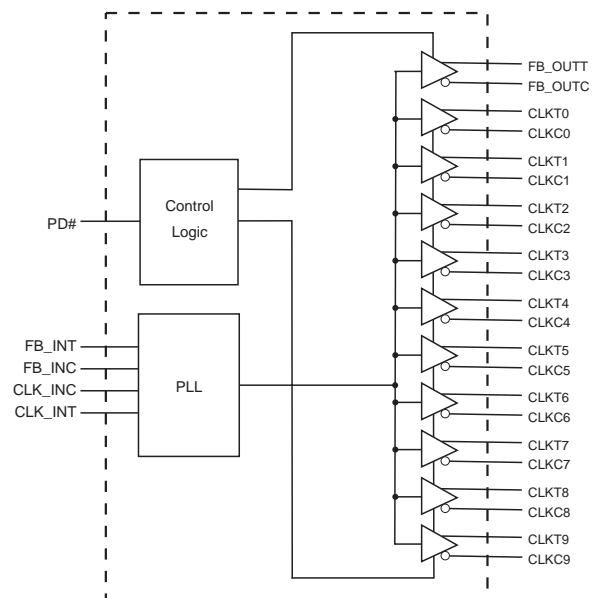
Pin Configuration



48-Pin TSSOP & TVSOP

6.10 mm. Body, 0.50 mm. pitch = TSSOP
4.40 mm. Body, 0.40 mm. pitch = TSSOP (TVSOP)

Block Diagram





Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
4, 11, 12, 15, 21, 28, 34, 38, 45,	VDD	PWR	Power supply 2.5V
1, 7, 8, 18, 24, 25, 31, 41, 42, 48	GND	PWR	Ground
16	AVDD	PWR	Analog power supply, 2.5V
17	AGND	PWR	Analog ground.
27, 29, 39, 44, 46, 22, 20, 10, 5, 3	CLKT(9:0)	OUT	"True" Clock of differential pair outputs.
26, 30, 40, 43, 47, 23, 19, 9, 6, 2	CLKC(9:0)	OUT	"Complementary" clocks of differential pair outputs.
14	CLK_INC	IN	"Complementary" reference clock input
13	CLK_INT	IN	"True" reference clock input
33	FB_OUTC	OUT	"Complementary" Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INC.
32	FB_OUTT	OUT	"True" Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INT.
36	FB_INT	IN	"True" Feedback input, provides feedback signal to the internal PLL for synchronization with CLK_INT to eliminate phase error.
35	FB_INC	IN	"Complementary" Feedback input, provides signal to the internal PLL for synchronization with CLK_INC to eliminate phase error.
37	PD#	IN	Power Down. LVCMOS input

This PLL Clock Buffer is designed for a V_{DD} of 2.5V, AV_{DD} of 2.5V and differential data input and output levels.

ICS93V857-XXX is a zero delay buffer that distributes a differential clock input pair (CLK_INC, CLK_INT) to ten differential pair of clock outputs (CLKT[0:9], CLKC[0:9]) and one differential pair feedback clock output (FB_OUT, FB_OUTC). The clock outputs are controlled by the input clocks (CLK_INC, CLK_INT), the feedback clocks (FB_INT, FB_INC), the 2.5-V LVCMOS input (PD#) and the Analog Power input (AV_{DD}). When input (PD#) is low while power is applied, the receivers are disabled, the PLL is turned off and the differential clock outputs are Tri-Stated. When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes.

When the input frequency is less than the operating frequency of the PLL, approximately 20MHz, the device will enter a low power mode. An input frequency detection circuit on the differential inputs, independent from the input buffers, will detect the low frequency condition and perform the same low power features as when the (PD#) input is low. When the input frequency increases to greater than approximately 20 MHz, the PLL will be turned back on, the inputs and outputs will be enabled and PLL will obtain phase lock between the feedback clock pair (FB_INT, FB_INC) and the input clock pair (CLK_INC, CLK_INT).

The PLL in **ICS93V857-XXX** clock driver uses the input clocks (CLK_INC, CLK_INT) and the feedback clocks (FB_INT, FB_INC) to provide high-performance, low-skew, low-jitter output differential clocks (CLKT [0:9], CLKC [0:9]). **ICS93V857-XXX** is also able to track Spread Spectrum Clock (SSC) for reduced EMI.

ICS93V857-XXX is characterized for operation from 0°C to 85°C.



Absolute Maximum Ratings

- Supply Voltage (VDD & AVDD) -0.5V to 4.6V
- Logic Inputs GND - 0.5V to V_{DD} + 0.5V
- Ambient Operating Temperature 0°C to +85°C
- Storage Temperature -65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 85°C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Current	I _{IH}	V _I = V _{DD} or GND	5			μA
Input Low Current	I _{IL}	V _I = V _{DD} or GND			5	μA
Operating Supply Current	I _{DD2.5}	C _L = 0pf @ 100MHz		250		mA
	I _{DDPD}	C _L = 0pf		65	90	mA
Input Clamp Voltage	V _{IK}	V _{DDQ} = 2.3V I _{in} = -18mA			-1.2	V
High-level output voltage	V _{OH}	I _{OH} = -1 mA	V _{DD} - 0.1	2.45		V
		I _{OH} = -12 mA	1.7	2.10		V
Low-level output voltage	V _{OL}	I _{OL} = 1 mA		0.05	0.1	V
		I _{OL} = 12 mA		0.35	0.6	V
Input Capacitance ¹	C _{IN}	V _I = GND or V _{DD}		3		pF
Output Capacitance ¹	C _{OUT}	V _{OUT} = GND or V _{DD}		3		pF

¹Guaranteed by design at 233MHz, not 100% tested in production.



Recommended Operating Condition (see note1)

$T_A = 0 - 85^\circ\text{C}$; Supply Voltage A_{VDD} , $V_{DD} = 2.5 \text{ V} \pm 0.2\text{V}$ (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DDQ}, A_{VDD}		2.3	2.5	2.7	V
Low level input voltage	V_{IL}	CLK_INT, CLK_INC, FB_INC, FB_INT		0.4	$V_{DD}/2 - 0.18$	V
		PD#	-0.3		0.7	V
High level input voltage	V_{IH}	CLK_INT, CLK_INC, FB_INC, FB_INT	$V_{DD}/2 + 0.18$	2.1		V
		PD#	1.7		$V_{DD} + 0.6$	V
DC input signal voltage (note 2)	V_{IN}		-0.3		$V_{DD} + 0.3$	V
Differential input signal voltage (note 3)	V_{ID}	DC - CLK_INT, CLK_INC, FB_INC, FB_INT	0.36		$V_{DD} + 0.6$	V
		AC - CLK_INT, CLK_INC, FB_INC, FB_INT	0.7		$V_{DD} + 0.6$	V
Output differential cross-voltage (note 4)	V_{OX}		$V_{DD}/2 - 0.15$		$V_{DD}/2 + 0.15$	V
Input differential cross-voltage (note 4)	V_{IX}		$V_{DD}/2 - 0.2$	$V_{DD}/2$	$V_{DD}/2 + 0.2$	V
High level output current	I_{OH}				-12	mA
Low level output current	I_{OL}				12	mA
High Impedance Output Current	I_{OZ}	$V_{DD}=2.7\text{V}, V_{OUT}=V_{DD}$ or GND		0.1	± 10	mA
Operating free-air temperature	T_A		0		85	$^\circ\text{C}$

Notes:

1. Unused inputs must be held high or low to prevent them from floating.
2. DC input signal voltage specifies the allowable DC execution of differential input.
3. Differential inputs signal voltages specifies the differential voltage [VTR-VCP] required for switching, where VTR is the true input level and VCP is the complementary input level.
4. Differential cross-point voltage is expected to track variations of V_{DD} and is the voltage at which the differential signal must be crossing.



Timing Requirements

T_A = 0 - 85C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Max clock frequency ³	freq _{op}	2.5V±0.2V	33	233	MHz
Application Frequency Range ³	freq _{App}	2.5V±0.2V	60	170	MHz
Input clock duty cycle	d _{tin}		40	60	%
CLK stabilization	T _{STAB}			100	µs

Switching Characteristics

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Low-to high level propagation delay time	t _{PLH} ¹	CLK_IN to any output		5.5		ns
High-to low level propagation delay time	t _{PHL} ¹	CLK_IN to any output		5.5		ns
Output enable time	t _{en}	PD# to any output		5		ns
Output disable time	t _{dis}	PD# to any output		5		ns
Period jitter	t _{jit (per)}	66/100/125/133/167MHz	-40		40	ps
Half-period jitter	t _{jit(hper)}	100 to <170MHz	-100		100	ps
		≥170MHz to 233MHz	-120		50	ps
Input clock slew rate	t _{s(l)}		1		4	v/ns
Output clock slew rate	t _{s(o)}	66/100/133/167MHz	1		2	v/ns
Cycle to Cycle Jitter ¹	t _{cyc-t_{cyc}}	66/100/125/133/167MHz			60	ps
Phase error	t _(phase error) ⁴		-50	0	50	ps
Output to Output Skew	t _{skew}			40	60	ps
Rise Time, Fall Time	t _r , t _f	Load = 120Ω/16pF	650	800	950	ps

Notes:

1. Refers to transition on noninverting output in PLL bypass mode.
2. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle=t_{wH}/t_c, where the cycle (t_c) decreases as the frequency goes up.
3. Switching characteristics guaranteed for application frequency range.
4. Static phase offset shifted by design.



Parameter Measurement Information

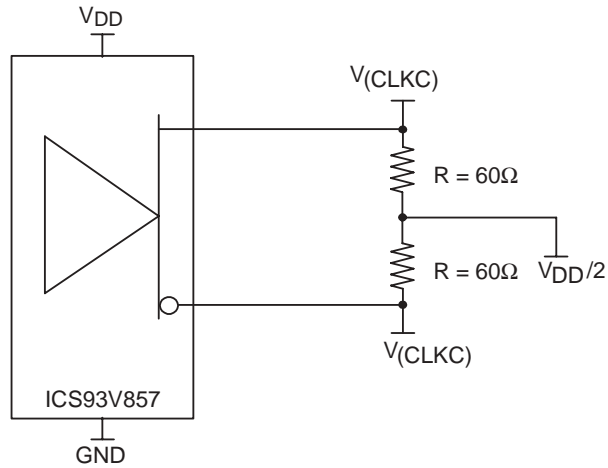
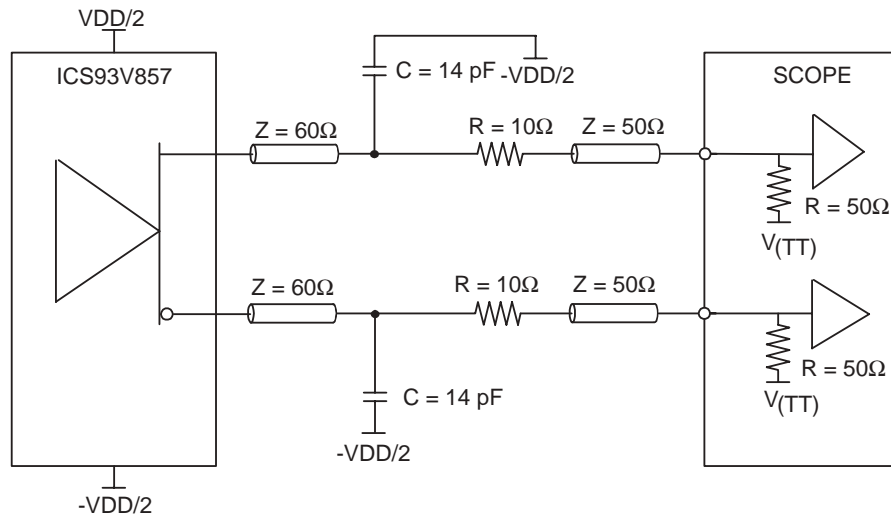


Figure 1. IBIS Model Output Load



NOTE: $V_{(TT)} = \text{GND}$

Figure 2. Output Load Test Circuit

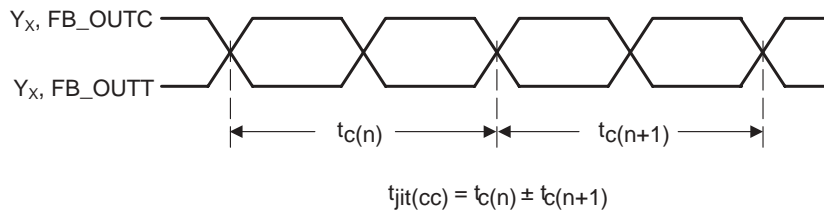


Figure 3. Cycle-to-Cycle Jitter



Parameter Measurement Information

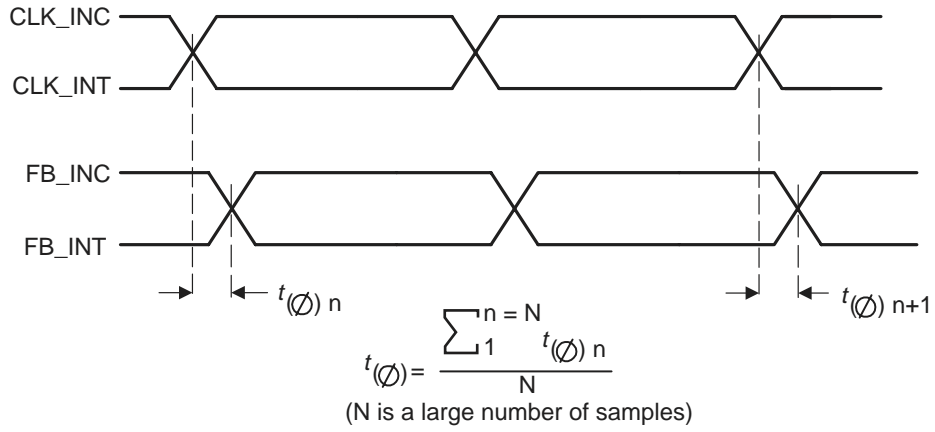


Figure 4. Static Phase Offset

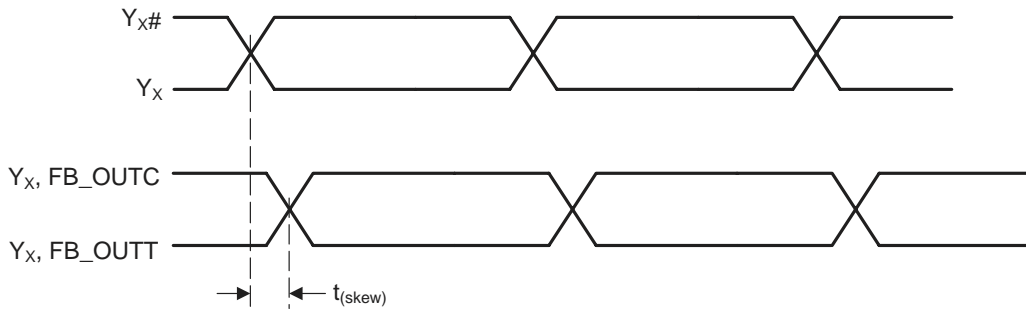


Figure 5. Output Skew

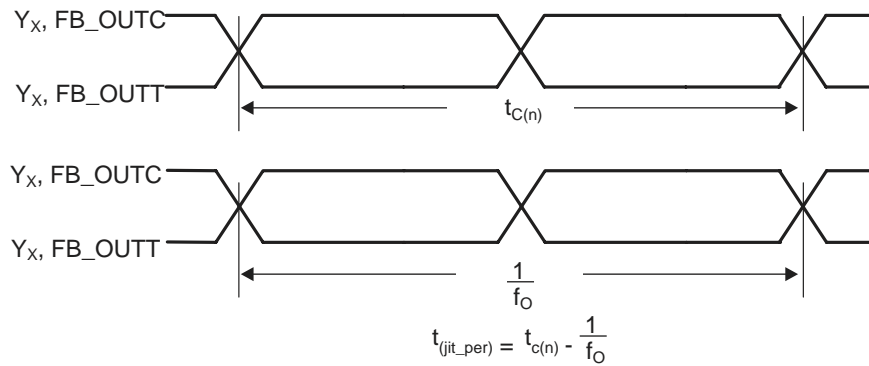


Figure 6. Period Jitter



Parameter Measurement Information

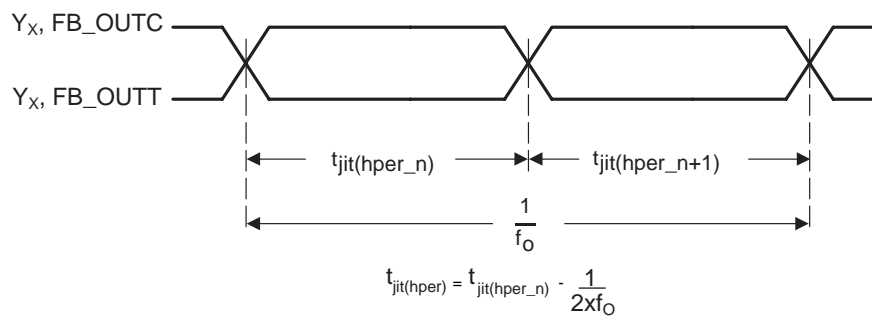


Figure 7. Half-Period Jitter

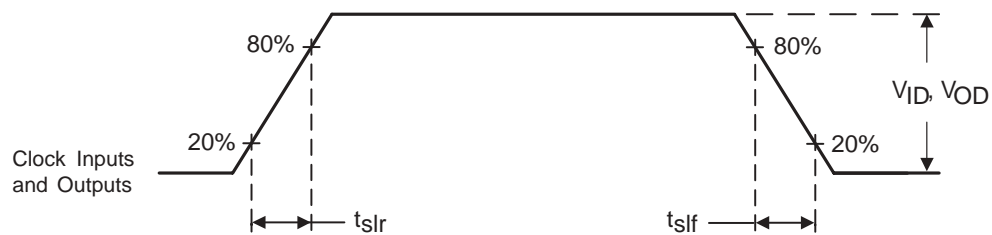
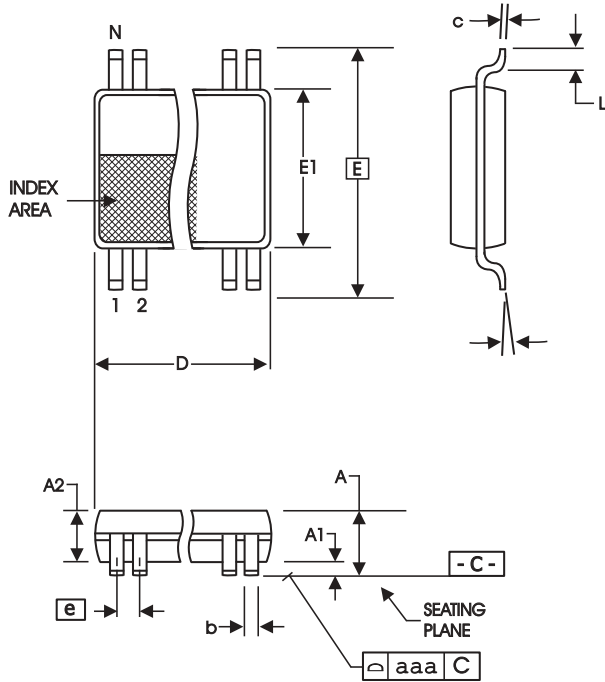


Figure 8. Input and Output Slew Rates



6.10 mm. Body, 0.50 mm. pitch TSSOP
(240 mil) (0.020 mil)

SYMBOL	In Millimeters		In Inches	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

Reference Doc.: JEDEC Publication 95, M O-153

10-0039

Choice of static phase offset available, for easy board tuning;
-XXX = device pattern number for options listed below.

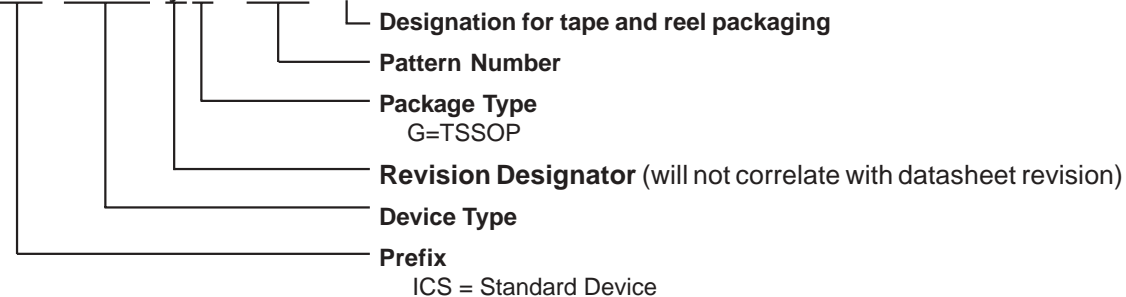
- ICS93V857-025 0ps
- ICS93V857-125 +125ps
- ICS93V857-130 .. +40ps

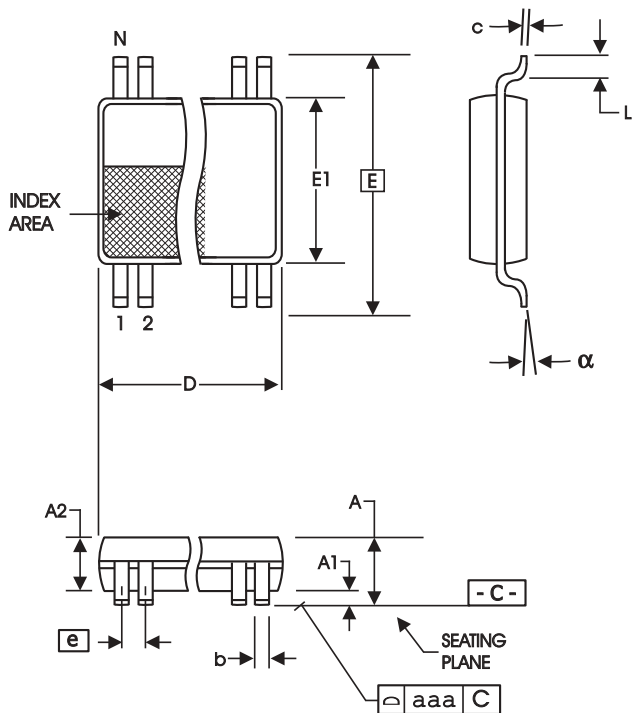
Ordering Information

ICS93V857yG-025T ICS93V857yG-125T ICS93V857yG-130T

Example:

ICS XXXX y G - PPP - T





4.40 mm. Body, 0.40 mm. pitch TSSOP
(173 mil) (16 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.13	0.23	.005	.009
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.40 BASIC		0.016 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.08	--	.003

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	9.60	9.80	.378	.386

Reference Doc.: JEDEC Publication 95, MO-153
 10-0037

Choice of static phase offset available, for easy board tuning;

-XXX = device pattern number for options listed below.

- ICS93V857-025 0ps
- ICS93V857-125 +125ps
- ICS93V857-130 .. +40ps

Ordering Information

ICS93V857yL-025T ICS93V857yL-125T ICS93V857yL-130T

Example:

ICS XXXX y L - PPP - T

