ADVANCE INFORMATION

CASCADABLE 16-BIT ARITHMETIC/LOGIC UNIT

FEATURES

- High-speed 16-bit, 8-function ALU
- Superset combination of four 74381/382-type 4-bit ALUs
- Input and output registers for pipelined operation (can be transparent)
- Easily cascadable with or without carry lookahead
- Internal feedback path for accumulation
- Low-power, high-speed CMOS
- All status and carry outputs available
- Pin-for-pin compatible with Logic Devices L4C381

APPLICATIONS

- Add partial sums-of-products from Zoran Digital Filter Processors to:
  - Create higher sample rate filters
  - Create larger word-length filters
  - Create larger 2-D kernel filters
- Digital Video
- Image processing
- Adaptive filters
- Radar
- Sonar
- High-speed communications

FUNCTIONAL DESCRIPTION

The ZR37381 is a flexible, high-speed 16-bit Arithmetic and Logic Unit slice. It combines four 74381/382-type ALUs, a lookahead carry generator, and miscellaneous interface logic in a 68-pin package. It is fully functional and performance compatible with the bipolar 74381/382 designs, but in addition it contains many new features such as input/output registers to support high-speed, pipelined architectures and single 16-bit bus architectures.

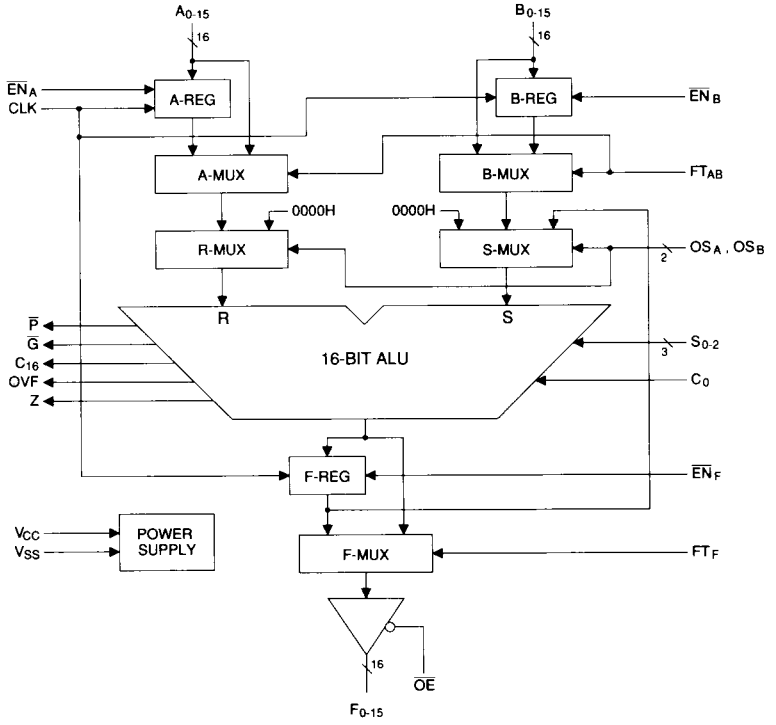


FIGURE 1. ZR37381 BLOCK DIAGRAM

INTERFACE SIGNAL DESCRIPTION

Name	Function
V_{CC}	+5V power supply input.
V_{SS}	Power supply ground input.
CLK	The CLK input strobes the input registers, A-REG and B-REG, and the output register F-REG.
$A_{0\text{-}15}$	These are the 16 inputs for operand A. They are passed directly to the inputs of the A operand multiplexer when FT_{AB} is high. When FT_{AB} is low, these inputs are strobed into the input register, A-REG, by the rising edge of CLK when $\overline{EN}_A$ is also low.
$B_{0\text{-}15}$	These are the 16 inputs for operand B. They are passed directly to the inputs of the B operand multiplexer when FT_{AB} is high. When FT_{AB} is low, these inputs are strobed into the input register B-REG, by the rising edge of CLK when $\overline{EN}_B$ is also low.
$F_{0\text{-}15}$	These 16 outputs are the result of the ALU operation. When FT_F is high, they propagate directly from the internal ALU. When FT_F is low they are the output of the internal pipeline register, F-REG, which is strobed by the rising edge of CLK when $\overline{EN}_F$ is low.
C_0	This is the carry input for cascading the ALU to process operands larger than 16 bits. It is the carry input for addition, but inverted carry for subtraction. See Table 3.
C_{16}	This is the ripple carry output for cascading the ALU to process operands larger than 16 bits. See Table 3.
$\overline{P}$	This is the active low carry propagate output for using carry lookahead. See Table 3.
$\overline{G}$	This is the active low carry generate output for using carry lookahead. See Table 3.
OVF	A high on this output indicates two's complement overflow in the ALU. See Table 3.
ZERO	A high on this output indicates all output bits, $F_{0\text{-}15}$ are zero.
$\overline{EN}_A$	A low on this input enables the input register, A-REG, to latch the operand A data on inputs $A_{0\text{-}15}$ upon the rising edge of CLK. Operation of $\overline{EN}_A$ is independent of FT_{AB}.
$\overline{EN}_B$	A low on this input enables the input register, B-REG, to latch the operand B data on inputs $B_{0\text{-}15}$ upon the rising edge of CLK. Operation of $\overline{EN}_B$ is independent of FT_{AB}.

Name	Function
FT_{AB}	A high on this input causes the input operands, $A_{0\text{-}15}$ and $B_{0\text{-}15}$ to bypass the input register, A-REG and B-REG, respectively. A low on this input causes the input operands to be latched into the A-REG and B-REG registers upon the rising edge of CLK when the corresponding enable signal, $\overline{EN}_A$ or $\overline{EN}_B$, is low.
$\overline{EN}_F$	A low on this input enables the output register, F-REG, to latch the ALU result upon the rising edge of CLK. Operation of $\overline{EN}_F$ is independent of FT_F.
FT_F	A high on this input causes the ALU result to bypass the output register, F-REG. A low on this input causes the ALU result to be latched into the F-REG register upon the rising edge of CLK when the enable signal, $\overline{EN}_F$, is low.
OS_A, OS_B	These two inputs select the source of A(OPA) and B(OPB) operands for the ALU, according to Table 1. The operands labelled "A" and "B" originate at the $A_{0\text{-}15}$ and $B_{0\text{-}15}$ device pins respectively. The operand "F" is the fedback ALU result. The operand "0" has all bits low.
$S_{0\text{-}2}$	These three inputs select the arithmetic or logical function to be performed according to Table 2.
$\overline{OE}$	A low on this input enables the ALU result to the three-state driver output pins, $F_{0\text{-}15}$. A high on this input disables the $F_{0\text{-}15}$ output pins.

TABLE 1

OS_B	OS_A	OPB	OPA
0	0	F	A
0	1	0	A
1	0	B	0
1	1	B	A

TABLE 2

S_2	S_1	S_0	Function
0	0	0	CLEAR (F=00...0)
0	0	1	NOT(A) + B
0	1	0	A + NOT(B)
0	1	1	A + B
1	0	0	A XOR B
1	0	1	A OR B
1	1	0	A AND B
1	1	1	PRESET (F=11...1)

ALU FUNCTIONAL DESCRIPTION

The ZR37381 operates on two 16-bit operands, A and B, to produce a single result, F. Three select lines, S_{0-2}, control the ALU function, providing the same 3 arithmetic, 3 logical and 2 initialization functions as the industry-standard 74381 and 74382 4-bit ALUs. Full ALU status is provided, compatible with both the 74381 and 74382. The carry propagate ($\overline{P}$) and generate ($\overline{G}$) signals of the 381 and the ripple carry (C_{16}) and overflow (OVF) signals of the 382 are all provided. In addition a ZERO flag indicates a zero ALU result. These signals allow the ALU to be cascaded to form longer word lengths.

Several features have been added to enhance the industry-standard functionality. Registers are provided on both the ALU inputs and the output to support high-speed pipelined architectures and 16-bit bus architectures. These may be bypassed under user control to replicate the industry-standard functionality.

An internal feedback path allows the registered ALU output result to be routed to the B ALU input for accommodating chain operations and accumulation. Either the A or B input to the ALU can be forced to zero, allowing unary functions to be performed on either operand.

ALU Function Selection

The three select signals, S_{0-2}, determine the ALU function to be performed, as shown in Table 2.

ALU Status

The ALU provides a ZERO status bit which is set when all sixteen output bits are zero. The two's complement overflow (OVF) and ripple carry (C_{16}) status, compatible with the industry-standard 74382, are provided. The carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) bits for look-ahead carry cascading, compatible with the industry-standard 74381, are also provided. The OVF, C_{16}, $\overline{P}$ and $\overline{G}$ outputs are defined for the three arithmetic functions only. Their status for the A+B operation is defined in Table 3. Status for NOT(A)+B and A+NOT(B) is determined by complementing A_i and B_i respectively in Table 3.

Operand Registers

The ZR37381 has two 16-bit input registers, A-REG and B-REG, to latch operands A and B. The operands are loaded into these registers on the rising edge of CLK when the respective enable signal, $\overline{EN}_A$ or $\overline{EN}_B$, is on. This feature allows the ZR37381 to be used in pipelined mode or to accept operands from a single 16-bit bus. Both registers may be bypassed to emulate the 381/382 exactly by asserting the FT_{AB} control signal high. Even though the registers are bypassed with FT_{AB} asserted, the registers continue to be loaded under control of the enable signals, $\overline{EN}_A$ and $\overline{EN}_B$.

Output Register

The ALU combinatorial logic output is latched into the output register, F-REG, on the rising edge of CLK when the enable signal, $\overline{EN}_F$, is asserted low. To emulate the 381/382 exactly, the output register is bypassed by asserting the FT_F control signal high. Even though the register is bypassed with FT_F asserted, the register will continue to be loaded under control of the enable signal, $\overline{EN}_A$. The output of the register or the ALU in bypass mode passes through three-state drivers to reach the device output pins. The three-state drivers are controlled by the $\overline{OE}$ signal; a low on $\overline{OE}$ enables the outputs, and a high disables them. These three-state outputs allow the ZR37381 output to be attached to a bus, for example, in a single, bidirectional bus system.

Operand Selection

Feature enhancements added to the industry-standard 381/382 ALUs are the ability to force one of the operands (either A or B) to zero and the ability to feedback the ALU output to the B input. The two operand select signals, OS_A and OS_B, control multiplexers immediately preceding the ALU inputs. Operand selection is shown in Table 1.

When both operand select lines are low, the ZR37381 is configured as a chain calculation ALU. The registered ALU output is fed back to the B input of the ALU. This allows accumulation to be performed by providing new operands at the A input port. The accumulator can be preloaded from the A input by setting OS_A high and OS_B low. The accumulator may be cleared by setting the function select lines to CLEAR ($S_0S_1S_0 = 000$). This feedback is not affected by the state of the FT_F control signal.

TABLE 3. ALU Status Flags

Bit Carry Generate = $g_i = A_iB_i$	for i = 0,1,...,15
Bit Carry Propagate = $p_i = A_i + B_i$	for i = 0,1,...,15
$P_0 = p_0$	
$P_i = p_i(P_{i-1})$	for i = 1,2,...,15
and	
$G_0 = g_0$	
$G_i = g_i + p_i(G_{i-1})$	for i = 1,2,...,15
$C_i = (G_{i-1}) + (P_{i-1})(C_{i-1})$	for i = 1,2,...,15
then	
$\overline{G}$ = NOT(G_{15})	
$\overline{P}$ = NOT(P_{15})	
$C_{16} = G_{15} + P_{15}C_{15}$	
OVF = C_{15} XOR C_{16}	

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias..... -55°C to +125°C
Storage Temperature..... -65°C to +150°C
Supply Voltage to Ground Potential
Continuous..... -0.5V to +7.0V

DC Voltage Applied to
Outputs for High Output State..... -0.5V to +7.0V
DC Input Voltage..... -0.5V to +5.5V

DC Output Current, into Outputs
(not to exceed 200 mA total)..... 20mA/output
Latch-up Trigger Current..... >200mA

NOTE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGE

Commercial Devices

Temperature..... $0°C \le T_A \le +70°C$
Supply Voltage..... $4.75V \le V_{CC} \le 5.25V$

Military Devices

Temperature..... $-55°C \le T_A \le +125°C$
Supply Voltage..... $4.5V \le V_{CC} \le 5.5V$

DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 8mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -2mA
I_{CC}	Power Supply Current		100	mA	T_A = 0°C, V_{CC} = 5V
I_{LI}	Input Leakage Current		±10	µA	$0 < V_{IN} < V_{CC}$
I_{LO}	Output Leakage Current		±10	µA	$0.45 < V_{OUT} < V_{CC}$
V_{CL}	Clock in Low Voltage	-0.5	0.6	V	
V_{CH}	Clock in High Voltage	4.0	V_{CC} + 0.5	V	
C_{IN}	Input Capacitance		10	pF	f_C = 1MHz
C_{IO}	I/O, Clock, and Output Capacitance		10	pF	f_C = 1MHz

SWITCHING CHARACTERISTICS (OVER COMMERCIAL OPERATING RANGE)

Guaranteed Maximum Combinational Delays (ns)

TO OUTPUT / FROM INPUT	ZR37381-55				ZR37381-40				ZR37381-26			
	F_{0-15}	$\overline{P}, \overline{G}$	OVF, Z	C_{16}	F_{0-15}	$\overline{P}, \overline{G}$	OVF, Z	C_{16}	F_{0-15}	$\overline{P}, \overline{G}$	OVF, Z	C_{16}
FT_{AB} = 0, FT_F = 0												
Clock	32	38	53	36	26	30	44	32	22	22	26	22
C_0	-	-	34	22	-	-	28	20	-	-	28	18
S_{0-2}, OS_A, OS_B	-	42	42	42	-	32	34	35	-	22	22	22
FT_{AB} = 0, FT_F = 1												
Clock	56	38	53	36	46	30	44	32	28	22	26	22
C_0	37	-	34	22	30	-	28	20	22	-	18	18
S_{0-2}, OS_A, OS_B	55	42	42	42	40	32	34	35	26	22	22	22
FT_{AB} = 1, FT_F = 0												
A_{0-15}, B_{0-15}	-	36	46	37	-	30	40	32	-	22	22	22
Clock	32	-	-	-	26	-	-	-	20	-	-	-
C_0	-	-	34	22	-	-	28	20	-	-	18	18
S_{0-2}, OS_A, OS_B	-	42	42	42	-	32	34	35	-	22	22	22
FT_{AB} = 1, FT_F = 1												
A_{0-15}, B_{0-15}	55	36	46	37	40	30	40	32	26	22	22	22
C_0	37	-	34	22	30	-	28	20	22	-	18	18
S_{0-2}, OS_A, OS_B	55	42	42	42	40	32	34	35	26	22	22	22

Guaranteed Minimum Setup and Hold Times with Respect to Clock Rising Edge (ns)

INPUT	ZR37381-55				ZR37381-40				ZR37381-26			
	FT_{AB} = 0		FT_{AB} = 1		FT_{AB} = 0		FT_{AB} = 1		FT_{AB} = 0		FT_{AB} = 1	
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold
A_{0-15}, B_{0-15}	8	0	35	0	6	0	28	0	6	0	16	0
C_0	21	0	21	0	16	0	16	0	8	0	8	0
S_{0-2}, OS_A, OS_B	44	0	44	0	32	0	32	0	18	0	18	0
$\overline{EN}_A$, $\overline{EN}_B$, $\overline{EN}_F$	8	0	8	0	6	0	6	0	6	0	6	0

Clock Cycle Time and Pulse Width (ns)

	ZR37381-55	ZR37381-40	ZR37381-26
Minimum Cycle Time	43	34	20
High-going Pulse	15	10	10
Low-going Pulse	15	10	10

Three State Enable/Disable Times (ns)

	ZR37381-55	ZR37381-40	ZR37381-26
t_{EN}	20	18	16
t_{DIS}	20	18	16

SWITCHING CHARACTERISTICS (OVER MILITARY OPERATING RANGE)

Guaranteed Maximum Combinational Delays (ns)

TO OUTPUT / FROM INPUT	ZR37381-65				ZR37381-45				ZR37381-30			
	F_{0-15}	$\overline{P}, \overline{G}$	OVF, Z	C_{16}	F_{0-15}	$\overline{P}, \overline{G}$	OVF, Z	C_{16}	F_{0-15}	$\overline{P}, \overline{G}$	OVF, Z	C_{16}
FT_{AB} = 0, FT_F = 0												
Clock	37	44	63	45	28	34	50	34	26	28	34	28
C_0	-	-	42	25	-	-	32	23	-	-	22	22
S_{0-2}, OS_A, OS_B	-	48	48	48	-	38	38	38	-	28	28	28
FT_{AB} = 0, FT_F = 1												
Clock	68	44	63	45	56	34	50	34	34	28	34	28
C_0	42	-	42	25	32	-	32	23	26	-	22	22
S_{0-2}, OS_A, OS_B	66	48	48	48	46	38	38	38	30	28	28	28
FT_{AB} = 1, FT_F = 0												
A_{0-15}, B_{0-15}	-	44	56	44	-	32	46	36	-	28	28	28
Clock	37	-	-	-	28	-	-	-	26	-	-	-
C_0	-	-	42	25	-	-	32	23	-	-	22	22
S_{0-2}, OS_A, OS_B	-	48	48	48	-	38	38	38	-	28	28	28
FT_{AB} = 1, FT_F = 1												
A_{0-15}, B_{0-15}	65	44	56	44	45	32	46	36	30	28	28	28
C_0	42	-	42	25	32	-	32	23	26	-	22	22
S_{0-2}, OS_A, OS_B	66	48	48	48	46	38	38	38	30	28	28	28

Guaranteed Minimum Setup and Hold Times with Respect to Clock Rising Edge (ns)

INPUT	ZR37381-65				ZR37381-45				ZR37381-30			
	FT_{AB} = 0		FT_{AB} = 1		FT_{AB} = 0		FT_{AB} = 1		FT_{AB} = 0		FT_{AB} = 1	
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold
A_{0-15}, B_{0-15}	10	0	43	0	8	0	33	0	8	0	20	0
C_0	25	0	25	0	20	0	20	0	12	0	12	0
S_{0-2}, OS_A, OS_B	50	0	50	0	36	0	36	0	20	0	20	0
$\overline{EN}_A$, $\overline{EN}_B$, $\overline{EN}_F$	10	0	10	0	8	0	8	0	8	0	8	0

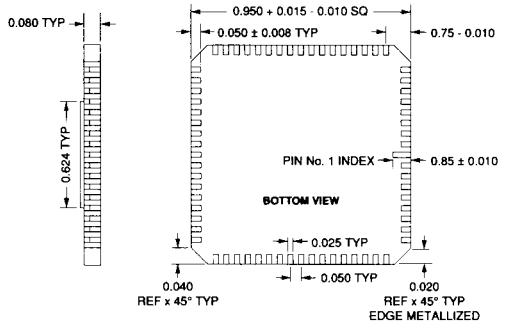
Clock Cycle Time and Pulse Width (ns)

	ZR37381-65	ZR37381-45	ZR37381-30
Minimum Cycle Time	52	38	26
High-going Pulse	20	15	12
Low-going Pulse	20	15	12

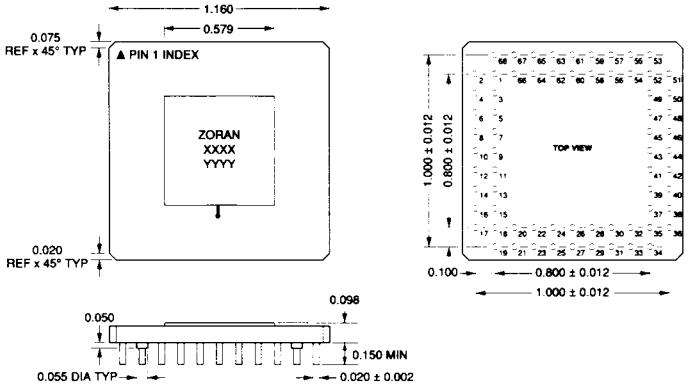
Three State Enable/Disable Times (ns)

	ZR37381-65	ZR37381-45	ZR37381-30
t_{EN}	22	20	18
t_{DIS}	22	20	18

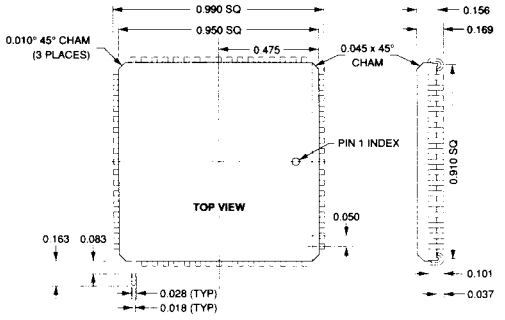
PACKAGE INFORMATION



68-TERMINAL CERAMIC LEADLESS CHIP CARRIER (L) [1,2]



68-TERMINAL PIN GRID ARRAY (G) [2]



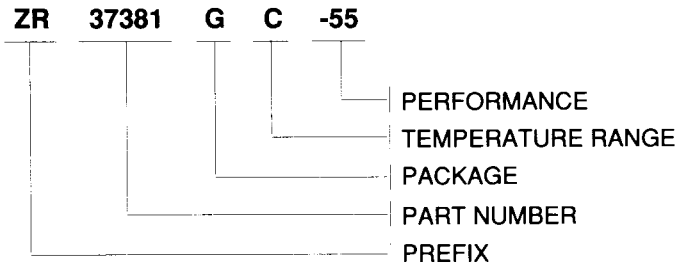
68-TERMINAL PLASTIC LEADED CHIP CARRIER (PJ) [1]

NOTES:
1. (L, PJ packages) Pin numbers sequenced counterclockwise from pin 1 in top view.
2. (L, G packages) Gold plating 60µ inches min. over 100µ inches ref. thickness of nickel.
3. ALL DIMENSIONS ARE IN INCHES.

PIN NUMBER LIST

FUNCTION	PIN # (PJ, L)	PIN # (G)	FUNCTION	PIN # (PJ, L)	PIN # (G)	FUNCTION	PIN # (PJ, L)	PIN # (G)	FUNCTION	PIN # (PJ, L)	PIN # (G)
A_0	1	60	V_{CC}	18	9	F_8	35	26	$\overline{EN}_A$	52	43
A_1	2	61	GND	19	10	F_7	36	27	B_0	53	44
A_2	3	62	C_{16}	20	11	F_6	37	28	B_1	54	45
A_3	4	63	$\overline{P}$	21	12	F_5	38	29	B_2	55	46
A_4	5	64	$\overline{G}$	22	13	F_4	39	30	B_3	56	47
A_5	6	65	ZERO	23	14	F_3	40	31	B_4	57	48
A_6	7	66	OVF	24	15	F_2	41	32	B_5	58	49
A_7	8	67	$\overline{EN}_F$	25	16	F_1	42	33	B_6	59	50
A_8	9	68	FT_F	26	17	F_0	43	34	B_7	60	51
A_9	10	1	$\overline{OE}$	27	18	C_0	44	35	B_8	61	52
A_{10}	11	2	F_{15}	28	19	S_0	45	36	B_9	62	53
A_{11}	12	3	F_{14}	29	20	S_1	46	37	B_{10}	63	54
A_{12}	13	4	F_{13}	30	21	S_2	47	38	B_{11}	64	55
A_{13}	14	5	F_{12}	31	22	OS_A	48	39	B_{12}	65	56
A_{14}	15	6	F_{11}	32	23	OS_B	49	40	B_{13}	66	57
A_{15}	16	7	F_{10}	33	24	FT_{AB}	50	41	B_{14}	67	58
CLK	17	8	F_9	34	25	$\overline{EN}_B$	51	42	B_{15}	68	59

ORDERING INFORMATION



PACKAGE

L - Leadless Chip Carrier
G - Pin Grid Array
PJ - Plastic Leaded Chip Carrier

TEMPERATURE RANGE

C - 0°C to +70°C (V_{CC} = 4.75V to 5.25V)
M - -55°C to +125°C (V_{CC} = 4.5V to 5.5V)

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NOTES

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