54F/74F273

Octal D Flip-Flop

Description

The 'F273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

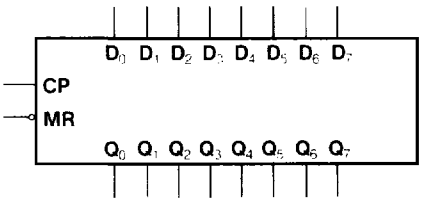
The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

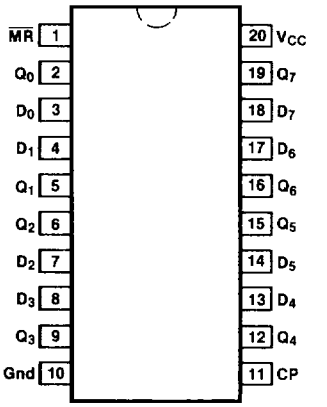
- **Ideal Buffer for MOS Microprocessor or Memory**
- **Eight Edge-Triggered D Flip-Flops**
- **Buffered Common Clock**
- **Buffered, Asynchronous Master Reset**
- **See 'F377 for Clock Enable Version**
- **See 'F377 for Transparent Latch Version**
- **See 'F374 for 3-State Version**

Ordering Code: See Section 5

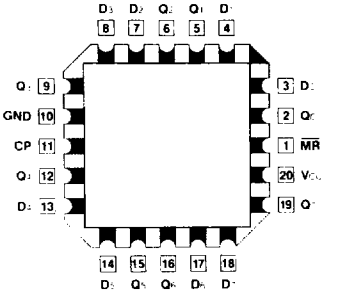
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

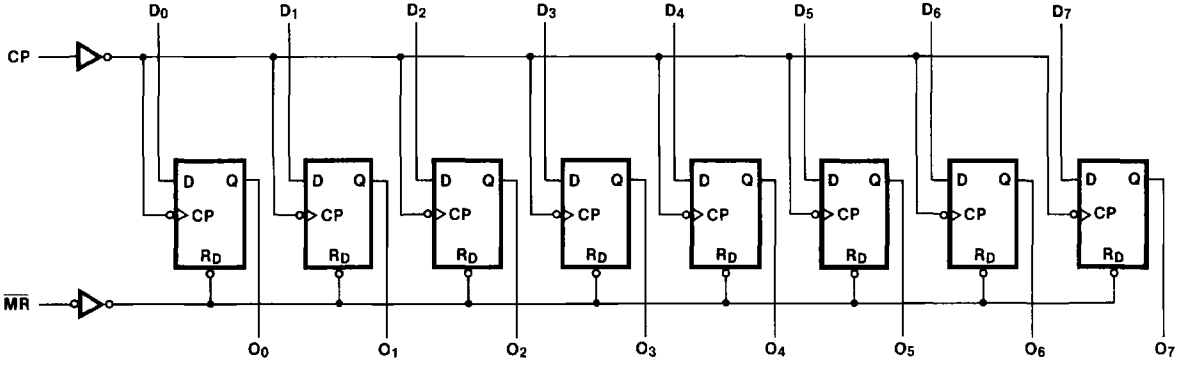
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_7	Data Inputs	0.5/0.375
$\overline{MR}$	Master Reset (Active LOW)	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
Q_0-Q_7	Data Outputs	25/12.5

Mode Select-Function Table

Operating Mode	Inputs			Output
	$\overline{MR}$	CP	D_n	Q_n
Reset (Clear)	L	X	X	L
Load '1'	H	↑	h	H
Load '0'	H	↑	l	L

H = HIGH Voltage Level steady state
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition
L = LOW Voltage Level steady state
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition
X = Immaterial
↑ = LOW-to-HIGH clock transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		50	60	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$	T_A, V_{CC} = Mil $C_L = 50\ pF$	T_A, V_{CC} = Com $C_L = 50\ pF$		
		Min Typ Max	Min Max	Min Max		
f_{max}	Maximum Clock Frequency	100			MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	10.0 11.0			ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay $\overline{MR}$ to Output	11.0 11.0			ns	3-1 3-11

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW Data to CP	3.0 3.0			ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW Data to CP	1.0 1.0			ns	3-5
$t_w(L)$	Clock Pulse Width, LOW	4.0			ns	3-7
$t_w(H)$ $t_w(L)$	$\overline{MR}$ Pulse Width HIGH or LOW	4.0 4.0			ns	3-11
t_{rec}	Recovery Time, $\overline{MR}$ to CP	3.0			ns	3-11