Document Title

256K x8 bit Super Low Power and Low Voltage Full CMOS Static RAM

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft	July 9, 1998	Advance

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256K x 8 bit Super Low Power and Low Voltage Full CMOS Static RAM

FEATURES

- Process Technology: Full CMOS
- Organization: 256K x8 bit
- Power Supply Voltage: 2.7 ~ 3.3V
- Low Data Retention Voltage: 1.0V(Min)
- Three state output status and TTL Compatible
- Package Type: 48-CSP with 0.75mm ball pitch

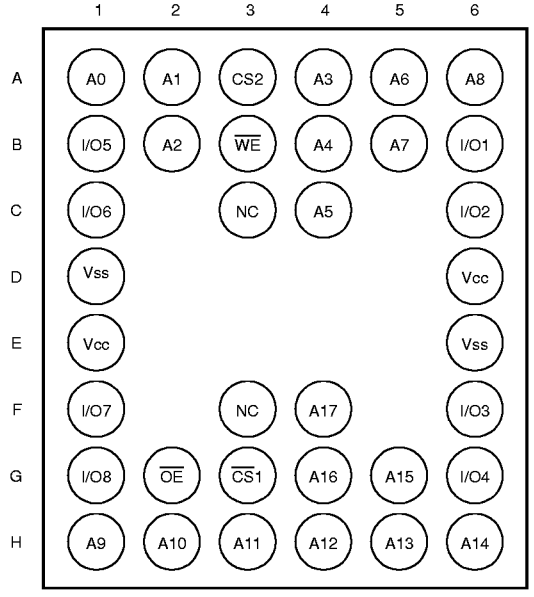
GENERAL DESCRIPTION

The KM68FU2000A families are fabricated by SAMSUNG's advanced full CMOS process technology. The families support industrial temperature range and 48 ball Chip Scale Package for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed(ns)	Power Dissipation		PKG Type
				Standby (I_{SB1}, Typ.)	Operating (I_{CC1}, Max)	
KM68FU2000A	Industrial(-40~85°C)	2.7~3.3V	70/100	0.5μA	3mA	48-CSP

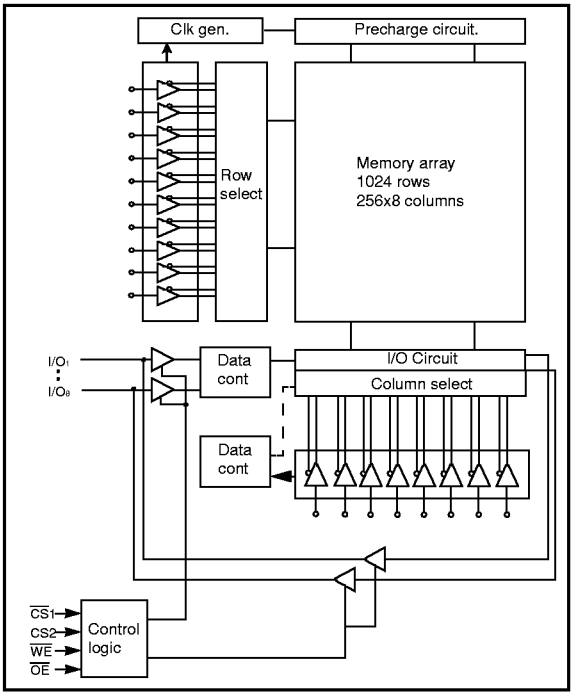
PIN DESCRIPTION



48-ball CSP - Top View (Ball Down)

Name	Function	Name	Function
$\overline{CS}_1$	Chip Select Input 1	Vcc	Power
CS_2	Chip Select Input 2	Vss	Ground
$\overline{OE}$	Output Enable Input	A_0~A_{17}	Address Inputs
$\overline{WE}$	Write Enable Input	I/O_1~I/O_8	Data Inputs/Outputs
N.C.	No Connection		

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Industrial Temperature Products(-40~85°C)	
Part Name	**Function**
KM68FU2000AZI-7	48-CSP with 48 ball, 70ns, 3.0V
KM68FU2000AZI-10	48-CSP with 48 ball, 100ns, 3.0V

FUNCTIONAL DESCRIPTION

$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	I/O	Mode	Power
H	X[1]	X[1]	X[1]	High-Z	Deselected	Standby
X[1]	L	X[1]	X[1]	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disable	Active
L	H	L	H	Dout	Read	Active
L	H	X[1]	L	Din	Write	Active

1. X means don't care. (Must be low or high state)

ABSOLUTE MAXIMUM RATINGS[1]

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.2 to 3.6V	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 4.0V	V
Power Dissipation	P_D	1.0	W
Storage temperature	T_{STG}	-55 to 150	°C
Operating Temperature	T_A	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	2.7	3.0	3.3	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	2.2	-	Vcc+0.3[2)]	V
Input low voltage	V_{IL}	-0.2[3)]	-	0.6	V

Note:
1. T_A=-40 to 85°C, otherwise specified
2. Overshoot: Vcc + 2.0 V in case of pulse width ≤ 20ns
3. Undershoot: -2.0 V in case of pulse width ≤ 20ns
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)] (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

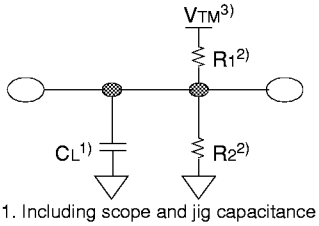
Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=Vss to Vcc	-1	-	1	μA
Output leakage current	I_{LO}	$\overline{CS_1}$=V_{IH} or CS_2=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to Vcc	-1	-	1	μA
Operating power supply current	I_{CC}	I_{IO}=0mA, $\overline{CS_1}$=V_{IL} or CS_2=V_{IH}, V_{IN}=V_{IL} or V_{IH}	-	-	3	mA
Average operating current	I_{CC1}	Cycle time=1ms, 100% duty, I_{IO}=0mA, $\overline{CS_1}$≤0.2V, CS_2≥V_{CC}-0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V	-	-	3	mA
	I_{CC2}	Cycle time=Min, 100% duty, I_{IO}=0mA, $\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, V_{IN}=V_{IL} or V_{IH}	-	-	35	mA
Output low voltage	V_{OL}	I_{OL}=2.1mA	-	-	0.4	V
Output high voltage	V_{OH}	I_{OL}=-1.0mA	2.2	-	-	V
Standby Current(TTL)	I_{SB}	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL}, Other inputs=V_{IL} or V_{IH}	-	-	0.3	mA
Standby Current (CMOS)	I_{SB1}	$\overline{CS_1}$≥Vcc-0.2V, CS_2≥Vcc-0.2V or $\overline{CS}$≤0.2V, Other inputs=0~Vcc	-	0.5	10[1)]	μA

1. Super low power product=2μA with special handling

AC OPERATING CONDITIONS

TEST CONDITIONS(Test Load and Test Input/Output Reference)

Input pulse level: 0.4 to 2.2V
Input rising and falling time: 5ns
Input and output reference voltage: 1.5V
Output load (See right):C_L= 100pF+1TTL



1. Including scope and jig capacitance
2. R_1=3070W, R_2=3150W
3. V_{TM}=2.8V

AC CHARACTERISTICS (T_A=-40 to 85°C, Vcc=2.7~3.3V)

Parameter List		Symbol	Speed Bins				Units
			70ns		100ns		
			Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	100	-	ns
	Address access time	tAA	-	70	-	100	ns
	Chip select to output	tCO	-	70	-	100	ns
	Output enable to valid output	tOE	-	35	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	25	0	30	ns
	Output disable to high-Z output	tOHZ	0	25	0	30	ns
	Output hold from address change	tOH	10	-	15	-	ns
Write	Write cycle time	tWC	70	-	100	-	ns
	Chip select to end of write	tCW	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	80	-	ns
	Write pulse width	tWP	55	-	70	-	ns
	Write recovery time	tWR	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	30	ns
	Data to write time overlap	tDW	30	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	ns

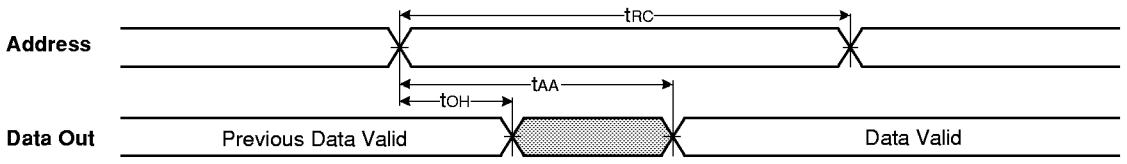
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
Vcc for data retention	VDR	$\overline{CS_1}$≥Vcc-0.2V1)	1.0	-	3.3	V
Data retention current	IDR	Vcc= 1.2V, $\overline{CS_1}$≥Vcc-0.2V1)	-	0.5	32)	µA
Data retention set-up time	tSDR	See data retention waveform	0	-	-	ns
Recovery time	tRDR		tRC	-	-	

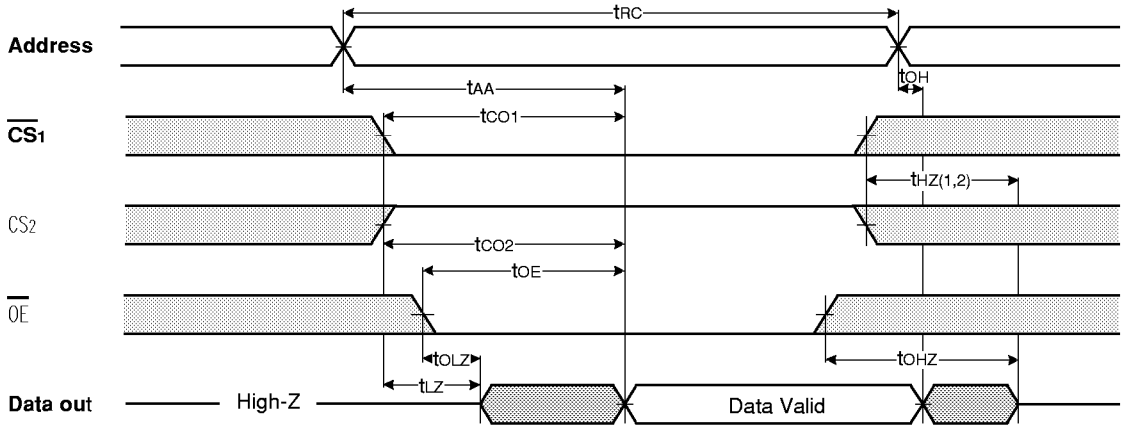
1. $\overline{CS_1}$≥Vcc-0.2V, CS_2≥Vcc-0.2V($\overline{CS_1}$ controlled) or CS_2≤0.2V(CS_2 controlled)
2. Super low power product=1µA with special handling.

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS1}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



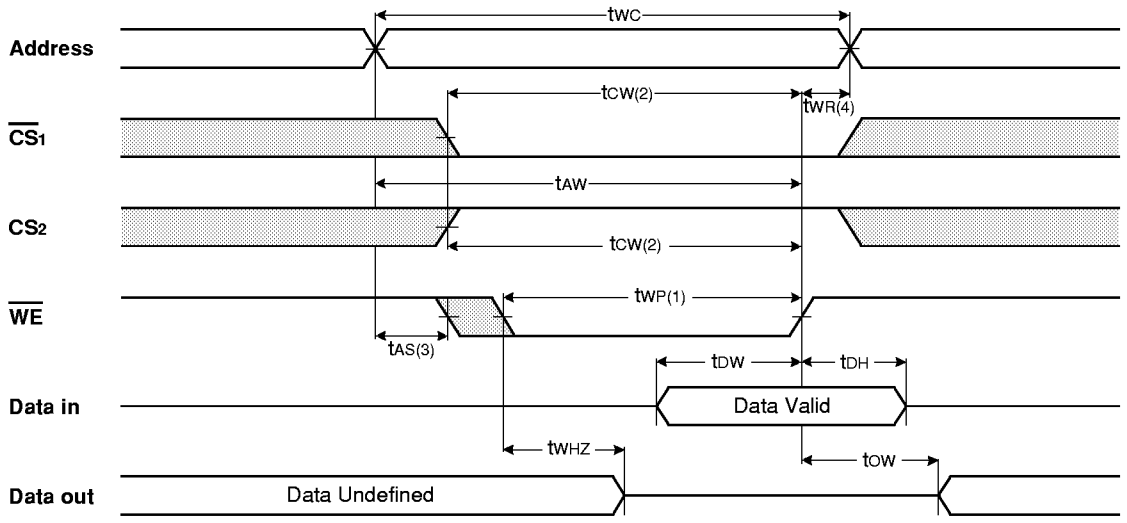
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



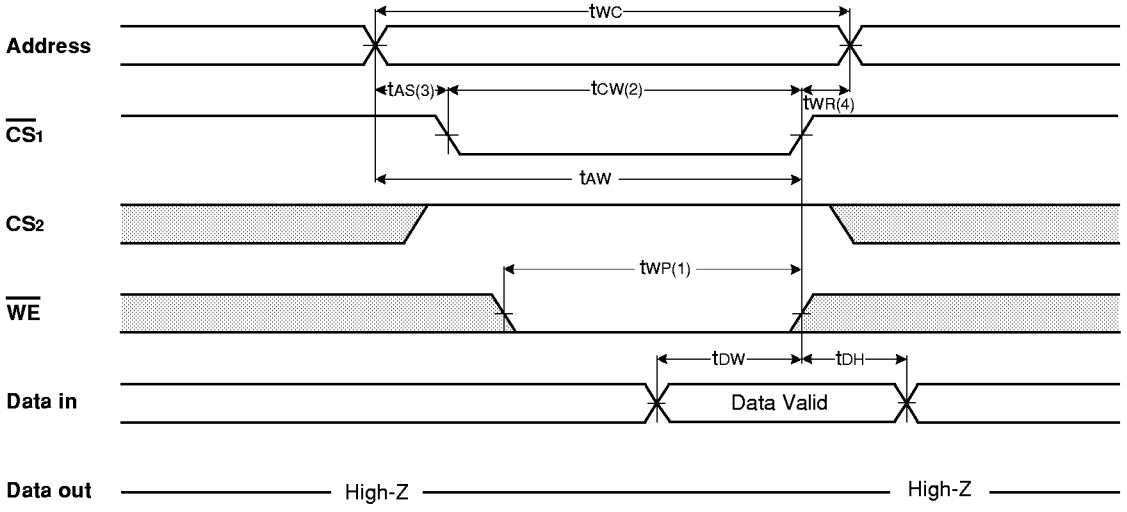
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

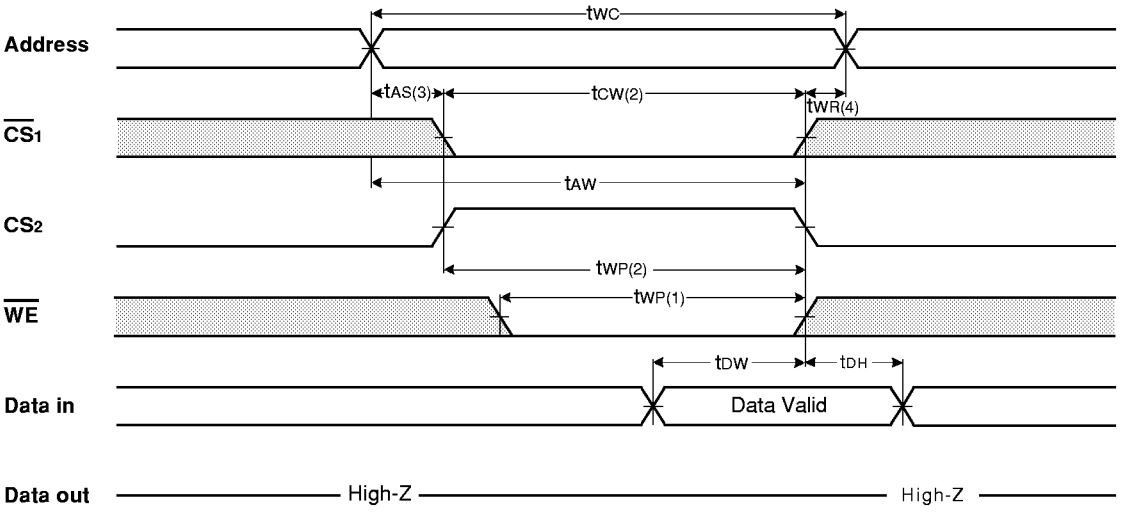
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS_1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{CS_1}$ Controlled)

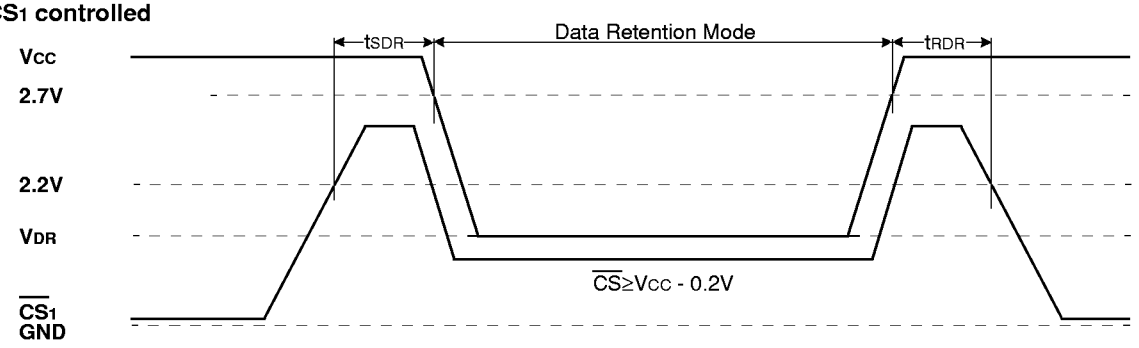


NOTES (WRITE CYCLE)

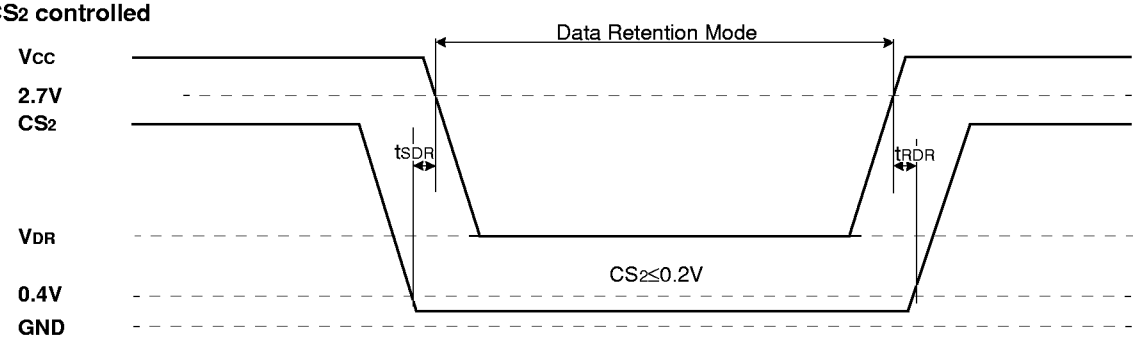
1. A write occurs during the overlap of a low $\overline{CS_1}$, a high CS_2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS_1}$ goes low, CS_2 going high and $\overline{WE}$ going low: A write end at the earliest transition among $\overline{CS_1}$ going high, CS_2 going low and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS_1}$ going low or CS_2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. $t_{WR(1)}$ applied in case a write ends as $\overline{CS_1}$ or $\overline{WE}$ going high $t_{WR(2)}$ applied in case a write ends as CS_2 going to low.

DATA RETENTION WAVE FORM

$\overline{CS_1}$ controlled

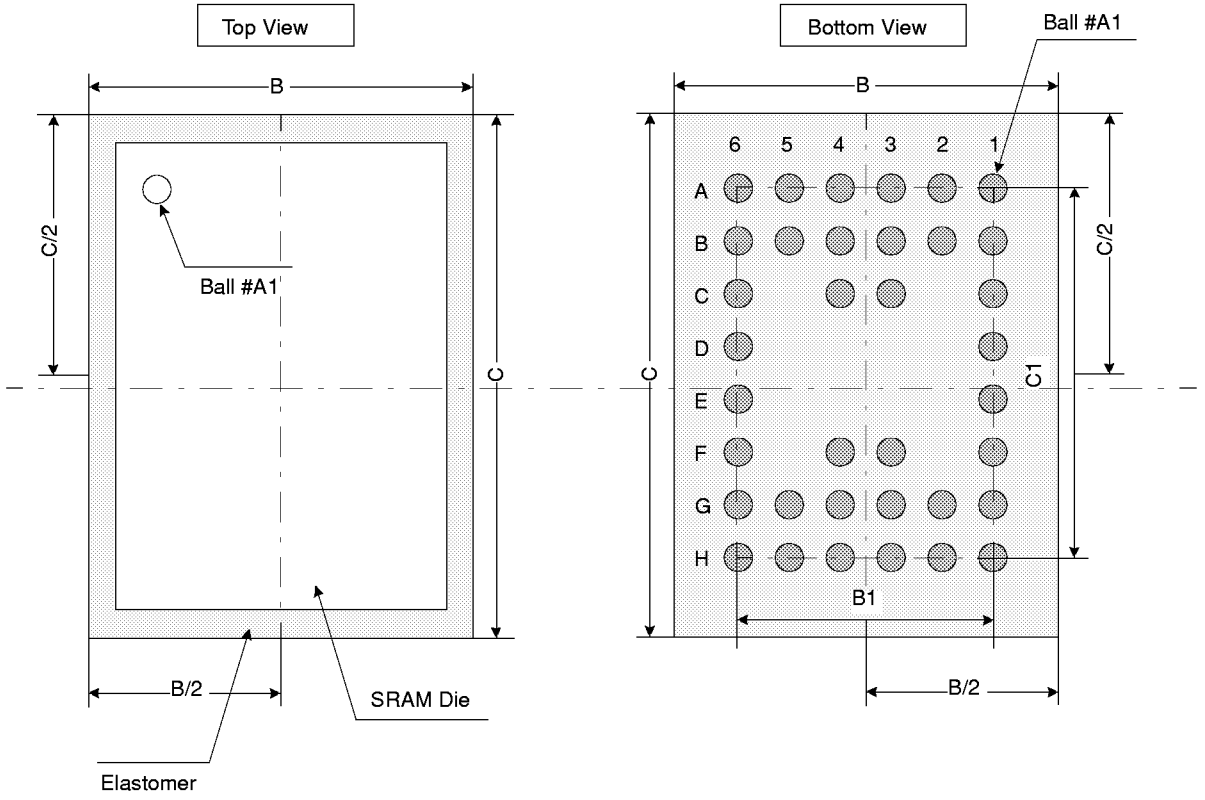


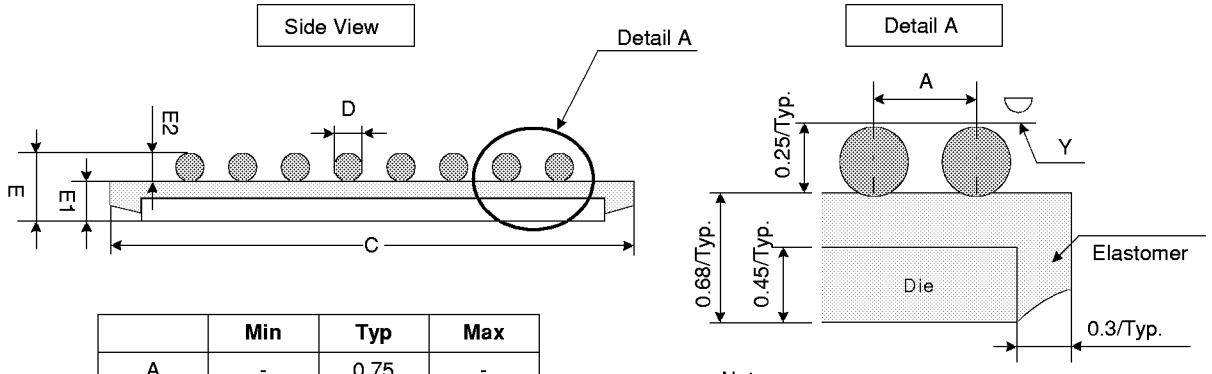
CS_2 controlled



PACKAGE DIMENSIONS

Units : millimeter





	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	0.93	0.94
E1	-	0.68	-
E2	-	0.25	-
Y	-	-	0.08

Notes.

1. Bump counts : 48(8row x 6row)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerence are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity: 0.08(Max)