National Semiconductor

54F/74F673A
16-Bit Serial-In, Serial/Parallel-Out Shift Register

General Description

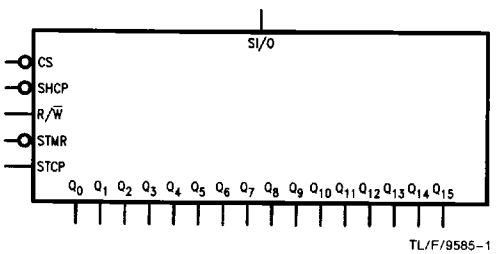
The 'F673A contains a 16-bit serial-in, serial-out shift register and a 16-bit parallel-out storage register. A single pin serves either as an input for serial entry or as a TRI-STATE® serial output. In the Serial-out mode, the data recirculates in the shift register. By means of a separate clock, the contents of the shift register are transferred to the storage register for parallel outputting. The contents of the storage register can also be parallel loaded back into the shift register. A HIGH signal on the Chip Select input prevents both shifting and parallel transfer. The storage register may be cleared via $\overline{STMR}$.

Features

- Serial-to-parallel converter
- 16-bit serial I/O shift register
- 16-bit parallel-out storage register
- Recirculating serial shifting
- Recirculating parallel transfer
- Common serial data I/O pin
- Slim 24 lead package

Ordering Code: See Section 5

Logic Symbols



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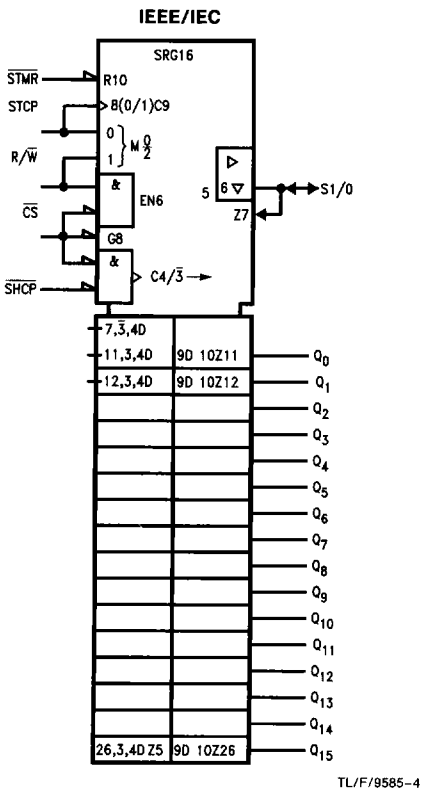
IEEE/IEC



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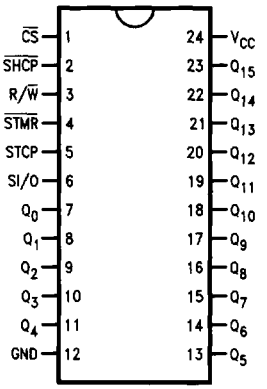
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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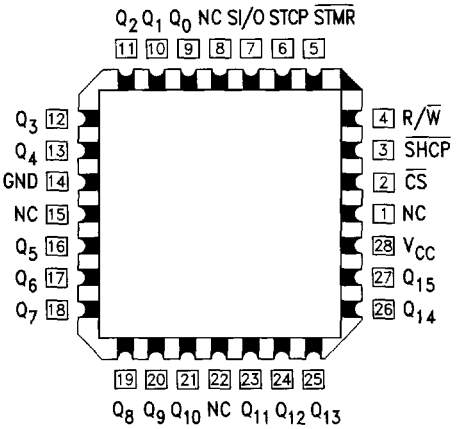
Pin Assignment for LCC



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Unit Loading/Fan Out: See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\overline{CS}$	Chip Select Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
$\overline{SHCP}$	Shift Clock Pulse Input (Active Falling Edge)	1.0/1.0	20 μA/−0.6 mA
$\overline{STMR}$	Store Master Reset Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
STCP	Store Clock Pulse Input	1.0/1.0	20 μA/−0.6 mA
R/$\overline{W}$	Read/Write Input	1.0/1.0	20 μA/−0.6 mA
SI/O	Serial Data Input or	3.5/1.0	70 μA/−0.6 mA
	TRI-STATE Serial Output	150/40 (33.3)	−3 mA/24 mA (20 mA)
Q_0–Q_{15}	Parallel Data Outputs	50/33.3	−1 mA/20 mA

Functional Description

The 16-bit shift register operates in one of four modes, as indicated in the Shift Register Operations Table. A HIGH signal on the Chip Select ($\overline{CS}$) input prevents clocking and forces the Serial Input/Output (SI/O) TRI-STATE buffer into the high impedance state. During serial shift-out operations, the SI/O buffer is active (i.e., enabled) and the output data is also recirculated back into the shift register. When parallel loading the shift register from the storage register, serial shifting is inhibited.

The storage register has an asynchronous master reset ($\overline{STMR}$) input that overrides all other inputs and forces the Q_0–Q_{15} outputs LOW. The storage register is in the Hold mode when either $\overline{CS}$ or the Read/Write (R/$\overline{W}$) input is HIGH. With $\overline{CS}$ and R/$\overline{W}$ both LOW, the storage register is parallel loaded from the shift register.

Shift Register Operations Table

Control Inputs				SI/O Status	Operating Mode
$\overline{CS}$	R/$\overline{W}$	$\overline{SHCP}$	STCP		
H	X	X	X	High Z	Hold
L	L		X	Data In	Serial Load
L	H	↘	L	Data Out	Serial Output with Recirculation
L	H	↘	H	Active	Parallel Load; No Shifting

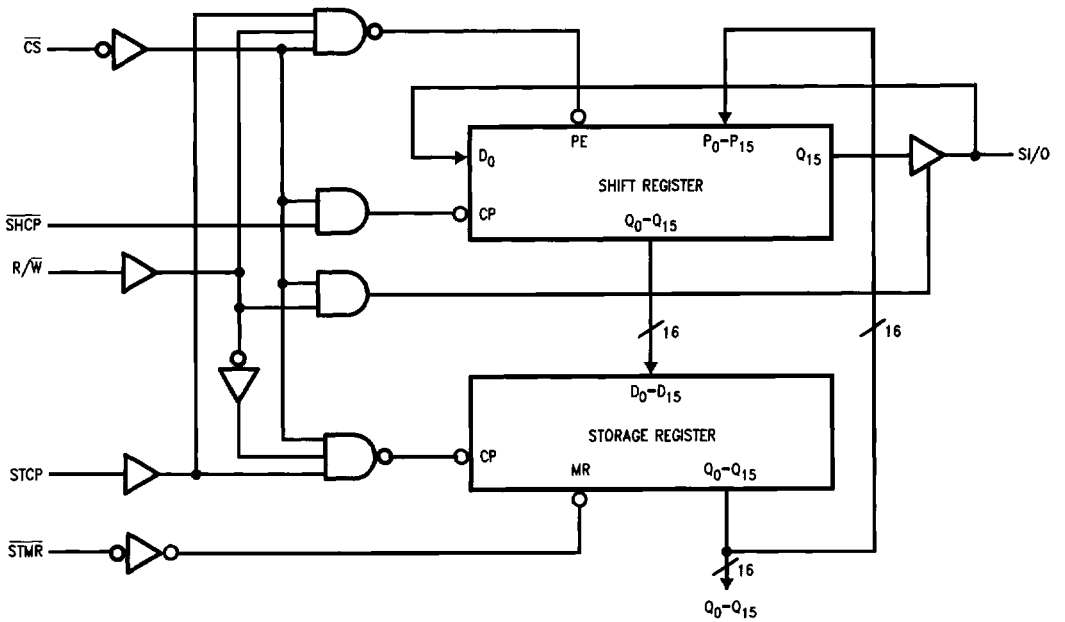
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↘ = HIGH-to-LOW Transition

Storage Register Operations Table

Control Inputs				Operating Mode
$\overline{STMR}$	$\overline{CS}$	R/$\overline{W}$	STCP	
L	X	X	X	Reset; Outputs LOW
H	H	X	X	Hold
H	X	H	X	Hold
H	L	L	↗	Parallel Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW-to-HIGH Transition

Block Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA (Non I/O pins)
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA (Q_n, SI/O)
		54F 10% V_{CC}	2.4					I_{OH} = −3 mA (SI/O)
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA (Q_n, SI/O)
		74F 10% V_{CC}	2.4					I_{OH} = −3 mA (SI/O)
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA (Q_n, SI/O)
		74F 5% V_{CC}	2.7					I_{OH} = −3 mA (SI/O)
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA (All outputs)
		74F 10% V_{CC}			0.5			I_{OL} = 20 mA (Q_n)
		74F 10% V_{CC}			0.5			I_{OL} = 24 mA (SI/O)
I_{IH}	Input HIGH Current				20	μA	Max	V_{IN} = 2.7V (Non I/O pins)
I_{BVI}	Input HIGH Current Breakdown Test				100	μA	Max	V_{IN} = 7.0V (Non I/O pins)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)				1.0	mA	Max	V_{IN} = 5.5V (SI/O)
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{IH} + I_{OZH}	Output Leakage Current				70	μA	Max	V_{OUT} = 2.7V (SI/O)
I_{IL} + I_{OZL}	Output Leakage Current				−650	μA	Max	V_{OUT} = 0.5V (SI/O)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CEX}	Output HIGH Leakage Current				250	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				500	μA	0.0V	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current			114	172	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			114	172	mA	Max	V_O = LOW

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$			54F $T_A, V_{CC} = Mil$ $C_L = 50\ pF$		74F $T_A, V_{CC} = Com$ $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	130				85		MHz	2-1
t_{PLH} t_{PHL}	Propagation Delay STCP to Q_n	3.0 3.0	8.0 10.5	10.5 13.5			2.5 2.5	12.0 15.0	ns	2-3
t_{PHL}	Propagation Delay $\overline{STMR}$ to Q_n	6.0	16.5	20.5			5.5	22.5	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{SHCP}$ to SI/O	4.0 4.5	6.5 8.0	8.5 10.5			3.5 4.0	9.5 12.0	ns	2-3
t_{PZH} t_{PZL}	Output Enable Time $\overline{CS}$ to SI/O	5.0 5.5	8.5 9.0	11.0 11.5			4.0 4.5	12.5 13.0	ns	2-5
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{CS}$ to SI/O	3.5 3.0	5.5 4.5	7.5 6.5			3.0 2.5	8.5 7.5		
t_{PZH} t_{PZL}	Output Enable Time R/$\overline{W}$ to SI/O	4.5 4.5	7.5 8.0	9.5 10.0			4.0 4.0	10.5 11.5	ns	2-5
t_{PHZ} t_{PLZ}	Output Disable Time R/$\overline{W}$ to SI/O	3.0 2.5	5.5 4.0	7.0 5.5			2.5 2.0	8.0 6.5		

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	54F/74F $T_A = +25°C$ $V_{CC} = +5.0V$		54F $T_A, V_{CC} = Mil$		74F $T_A, V_{CC} = Com$		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CS}$ or R/$\overline{W}$ to STCP	3.5 6.0				4.0 7.0		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CS}$ or R/$\overline{W}$ to STCP	0 0				0 0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW SI/O to $\overline{SHCP}$	3.0 3.0				3.5 3.5		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW SI/O to $\overline{SHCP}$	3.0 3.0				3.5 3.5			