HARRIS

# RFP4N05L
# RFP4N06L

## N-Channel Logic Level Power Field-Effect Transistors ($L^2FET$)

August 1991

### Features

- 4A, 50V and 60V
- $r_{DS(ON)} = 0.8\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanoscecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

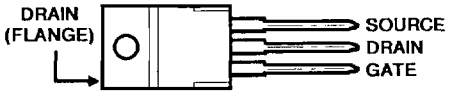
### Description

The RFP4N05L and RFP4N06L are N-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFP series types are supplied in the JEDEC TO-220AB plastic package.

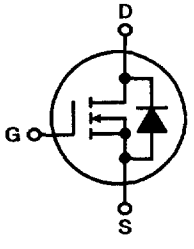
### Package

TO-220AB
TOP VIEW




### Terminal Diagram

N-CHANNEL ENHANCEMENT MODE




**Absolute Maximum Ratings** ($T_C$ = +25°C) Unless Otherwise Specified

| | | RFP4N05L | RFP4N06L | UNITS |
|---|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 50 | 60 | V |
| Drain-Gate Voltage ($R_{GS}$ = 1MΩ) | $V_{DGR}$ | 50 | 60 | V |
| Continuous Drain Current | | | | |
| RMS Continuous | $I_D$ | 4 | 4 | A |
| Pulsed Drain Current | $I_{DM}$ | 10 | 10 | A |
| Gate-Source Voltage | $V_{GS}$ | ±10 | ±10 | V |
| Maximum Power Dissipation | | | | |
| $T_C$ = +25°C | $P_D$ | 25 | 25 | W |
| Above $T_C$ = +25°C, Derate Linearly | | 0.2 | 0.2 | W/°C |
| Operating and Storage Junction Temperature Range | $T_J, T_{STG}$ | -55 to +150 | -55 to +150 | °C |

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.



File Number **2876**

**Electrical Characteristics** ($T_C$ = +25°C), Unless Otherwise Specified

| CHARACTERISTIC | SYMBOLS | TEST CONDITIONS | LIMITS RFP4N05L MIN | LIMITS RFP4N05L MAX | LIMITS RFP4N06L MIN | LIMITS RFP4N06L MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $I_D$ = 1mA, $V_{GS}$ = 0 | 50 | – | 60 | – | V |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 2mA | 1 | 2 | 1 | 2 | V |
| Zero-Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 40V | – | 1 | – | – | μA |
| | | $V_{DS}$ = 50V | – | – | – | 1 | μA |
| | | $T_C$ = +125°C, $V_{DS}$ = 40V | – | 50 | – | – | μA |
| | | $V_{DS}$ = 50V | – | – | – | 50 | mA |
| Gate-Source Leakage Current | $I_{GSS}$ | $V_{GS}$ = ±10V, $V_{DS}$ = 0 | – | 100 | – | 100 | nA |
| Drain-Source On-Voltage | $V_{DS(on)}$* | $I_D$ = 1A, $V_{GS}$ = 5V | – | 0.8 | – | 0.8 | V |
| | | $I_D$ = 2A, $V_{GS}$ = 5V | – | 2.0 | – | 2.0 | V |
| | | $I_D$ = 4A, $V_{GS}$ = 7.5V | – | 4.8 | – | 4.8 | V |
| Static Drain-Source On Resistance | $r_{DS(on)}$* | $I_D$ = 1A, $V_{GS}$ = 5V | – | 0.8 | – | 0.8 | Ω |
| Forward Transconductance | $g_{fs}$* | $I_D$ = 1A, $V_{DS}$ = 10V | 800 | – | 800 | – | S(℧) |
| Input Capacitance | $C_{ISS}$ | $V_{GS}$ = 0V, $V_{DS}$ = 25V, f = 1MHz | – | 225 | – | 225 | pF |
| Output Capacitance | $C_{OSS}$ | | – | 100 | – | 100 | pF |
| Reverse Transfer Capacitance | $C_{RSS}$ | | – | 40 | – | 40 | pF |
| Turn-On Delay Time | $t_{d(on)}$ | $I_D$ = 1A, $V_{DD}$ = 30V, $R_{GEN}$ = ∞, $R_{GS}$ = 6.25V, $V_{GS}$ = 5V | 10 (typ) | 20 | 10 (typ) | 20 | ns |
| Rise Time | $t_r$ | | 65 (typ) | 130 | 65 (typ) | 130 | ns |
| Turn-Off Delay Time | $t_{d(off)}$ | | 20 (typ) | 40 | 20 (typ) | 40 | ns |
| Fall Time | $t_f$ | | 30 (typ) | 60 | 30 (typ) | 60 | ns |
| Thermal Resistance Junction-to-Case | $R_{\theta JC}$ | | – | 5 | – | 5 | °C/W |

**Source-Drain Diode Ratings and Characteristics**

| CHARACTERISTIC | SYMBOLS | TEST CONDITIONS | LIMITS RFP4N05L MIN | LIMITS RFP4N05L MAX | LIMITS RFP4N06L MIN | LIMITS RFP4N06L MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Diode Forward Voltage | $V_{SD}$* | $I_{SD}$ = 1A | – | 1.4 | – | 1.4 | V |
| Diode Reverse Recovery Time | $t_{rr}$ | $I_F$ = 2A, $d_{IF}/dt$ = 100A/μs | 150 (typ) | 150 (typ) | 150 (typ) | 150 (typ) | ns |

* Pulse Test: Width ≤ 300μs, Duty Cycle ≤ 2%.

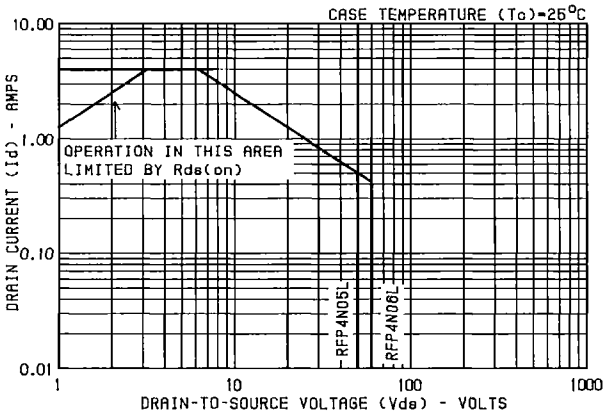



*Fig. 1 - Maximum operating areas for all types.*

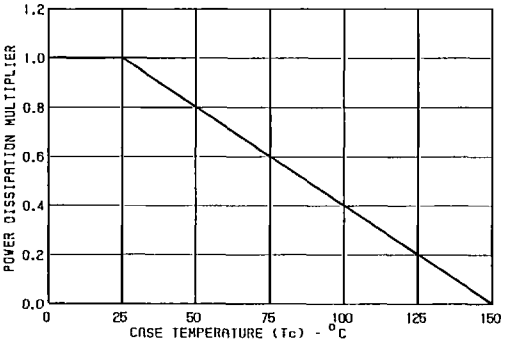



*Fig. 2 - Power dissipation vs. case temperature derating curve for all types.*

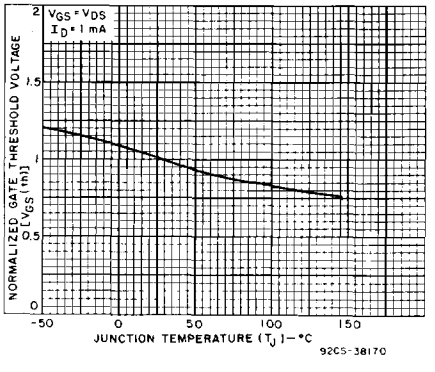



*Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.*

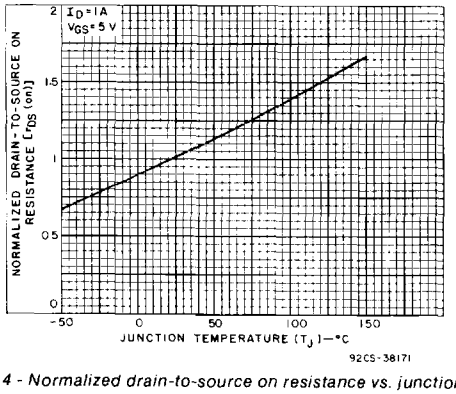



*Fig. 4 - Normalized drain-to-source on resistance vs. junction temperature for all types.*

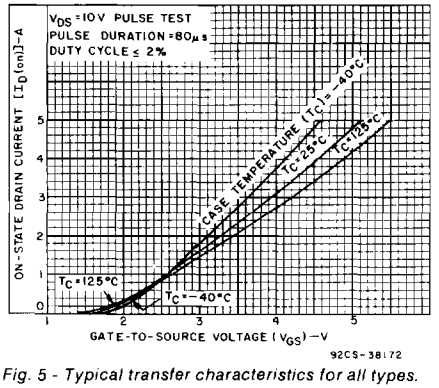



*Fig. 5 - Typical transfer characteristics for all types.*

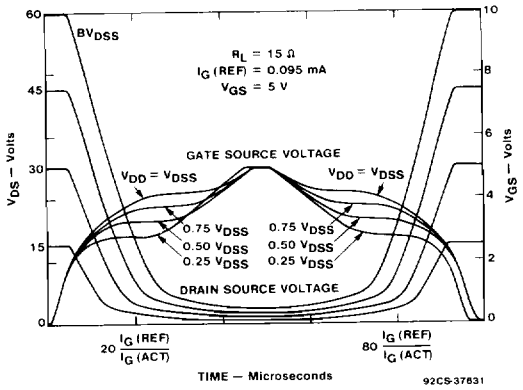



*Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.*

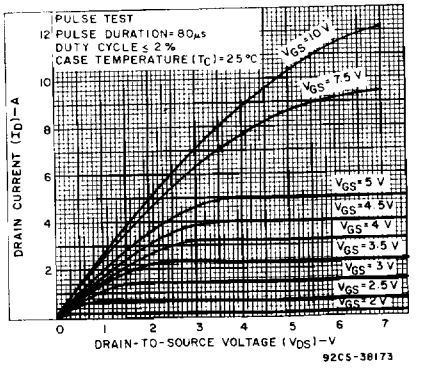



*Fig. 7 - Typical saturation characteristics for all types.*

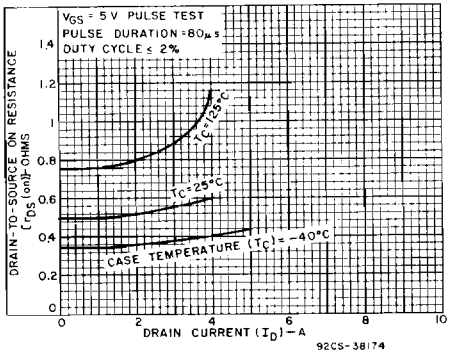



*Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.*

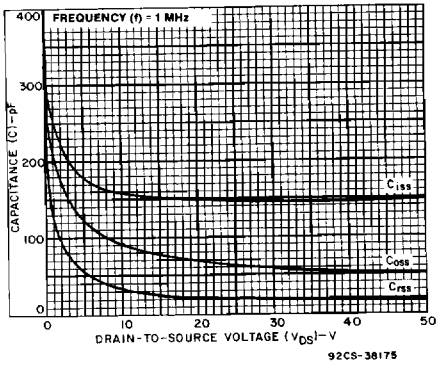



*Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.*

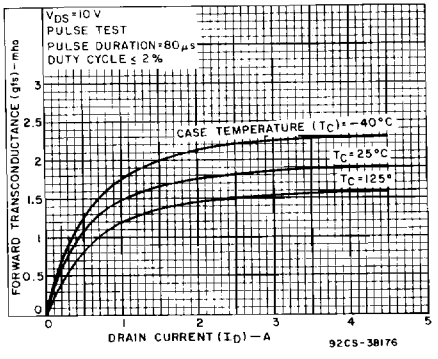



*Fig. 10 - Typical forward transconductance as a function of drain current for all types.*

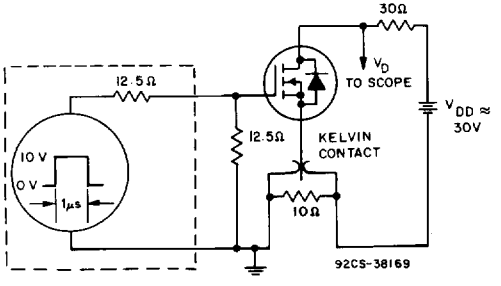



*Fig. 11 - Switching Time Test Circuit.*