

# MM54C74/MM74C74 Dual D Flip-Flop

## General Description

The MM54C74/MM74C74 dual D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. Each flip-flop has independent data, preset, clear and clock inputs and Q and  $\bar{Q}$  outputs. The logic level present at the data input is transferred to the output during the positive going transition of the clock pulse. Preset or clear is independent of the clock and accomplished by a low level at the preset or clear input.

## Features

- Supply voltage range 3V to 15V
- Tenth power TTL compatible Drive 2 LPT<sup>2</sup>L loads
- High noise immunity 0.45 V<sub>CC</sub> (typ.)

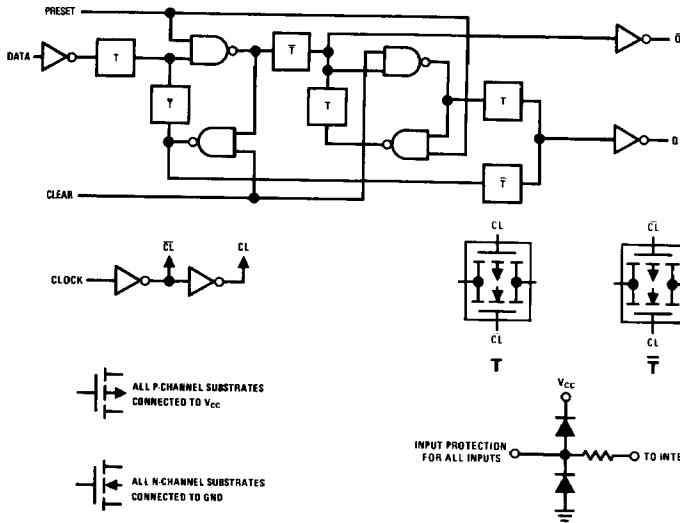
- Low power
- Medium speed operation

50 nW (typ.)  
10 MHz (typ.)  
with 10V supply

## Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial electronics
- Remote metering
- Computers

## Logic Diagram



## Truth Table

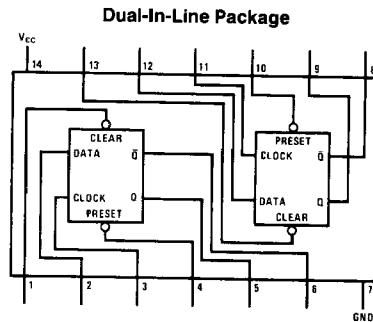
Preset	Clear	Q <sub>n</sub>	$\bar{Q}_n$
0	0	0	0
0	1	1	0
1	0	0	1
1	1	*Q <sub>n</sub>	* $\bar{Q}_n$

\*No change in output from previous state.

## Order Number MM54C74\* or MM74C74\*

\*Please look into Section 8, Appendix D for availability of various package types.

## Connection Diagram



## Top View

Note: A logic "0" on clear sets Q to logic "0".  
A logic "0" on preset sets Q to logic "1".

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin (Note 1)	-0.3V to $V_{CC} + 0.3V$
Operating Temperature Range	-55°C to +125°C
MM54C74	-40°C to +85°C
MM74C74	

Storage Temperature Range	-65°C to +150°C
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (Soldering, 10 seconds)	260°C
Operating $V_{CC}$ Range	3V to 15V
$V_{CC}(\text{Max})$	18V

**DC Electrical Characteristics** Min/Max limits apply across temperature range unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>CMOS TO CMOS</b>						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$	3.5			V
		$V_{CC} = 10V$	80			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$			1.5	V
		$V_{CC} = 10V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V$	4.5			V
		$V_{CC} = 10V$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V$			0.5	V
		$V_{CC} = 10V$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$			1.0	$\mu A$
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$	-1.0			$\mu A$
$I_{CC}$	Supply Current	$V_{CC} = 15V$		0.05	60	$\mu A$
<b>CMOS/LPTTL INTERFACE</b>						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5$			
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC} = 4.75V$ 74C, $V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC} = 4.5V, I_D = -360 \mu A$ 74C, $V_{CC} = 4.75V, I_D = -360 \mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC} = 4.5V, I_D = 360 \mu A$ 74C, $V_{CC} = 4.75V, I_D = 360 \mu A$			0.4	V
<b>OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)</b>						
$I_{SOURCE}$	Output Source Current	$V_{CC} = 5V, V_{IN(0)} = 0V$ $T_A = 25^\circ C, V_{OUT} = 0V$	-1.75			mA
$I_{SOURCE}$	Output Source Current	$V_{CC} = 10V, V_{IN(0)} = 0V$ $T_A = 25^\circ C, V_{OUT} = 0V$	-8.0			mA
$I_{SINK}$	Output Sink Current	$V_{CC} = 5V, V_{IN(1)} = 5V$ $T_A = 25^\circ C, V_{OUT} = V_{CC}$	1.75			mA
$I_{SINK}$	Output Sink Current	$V_{CC} = 10V, V_{IN(1)} = 10V$ $T_A = 25^\circ C, V_{OUT} = V_{CC}$	8.0			mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

# AC Electrical Characteristics\* $T_A = 25^\circ\text{C}$ , $C_L = 50\text{ pF}$ , unless otherwise noted

MMS4C74/MM74C74

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$C_{IN}$	Input Capacitance	Any Input (Note 2)		5.0		pF
$t_{pd}$	Propagation Delay Time to a Logical "0" $t_{pd0}$ or Logical "1" $t_{pd1}$ from Clock to Q or $\bar{Q}$	$V_{CC} = 5V$		180	300	ns
		$V_{CC} = 10V$		70	110	ns
$t_{pd}$	Propagation Delay Time to a Logical "0" from Preset or Clear	$V_{CC} = 5V$		180	300	ns
		$V_{CC} = 10V$		70	110	ns
$t_{pd}$	Propagation Delay Time to a Logical "1" from Preset or Clear	$V_{CC} = 5V$		250	400	ns
		$V_{CC} = 10V$		100	150	ns
$t_{SO}, t_{S1}$	Time Prior to Clock Pulse that Data Must be Present $t_{SETUP}$	$V_{CC} = 5V$	100	50		ns
		$V_{CC} = 10V$	40	20		ns
$t_{H0}, t_{H1}$	Time after Clock Pulse that Data Must be Held	$V_{CC} = 5V$		-20	0	ns
		$V_{CC} = 10V$		-8.0	0	ns
$t_{PW1}$	Minimum Clock Pulse Width ( $t_{WL} = t_{WH}$ )	$V_{CC} = 5V$		100	250	ns
		$V_{CC} = 10V$		40	100	ns
$t_{PW2}$	Minimum Preset and Clear Pulse Width	$V_{CC} = 5V$		100	180	ns
		$V_{CC} = 10V$		40	70	ns
$t_r, t_f$	Maximum Clock Rise and Fall Time	$V_{CC} = 5V$	15.0			$\mu\text{s}$
		$V_{CC} = 10V$	5.0			$\mu\text{s}$
$f_{MAX}$	Maximum Clock Frequency	$V_{CC} = 5V$	2.0	3.5		MHz
		$V_{CC} = 10V$	5.0	8.0		MHz
$C_{PD}$	Power Dissipation Capacitance	(Note 3)		40		pF

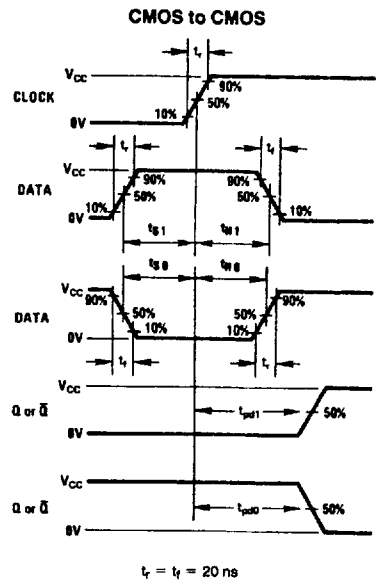
\*AC Parameters are guaranteed by DC correlated testing.

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:** Capacitance is guaranteed by periodic testing.

**Note 3:**  $C_{PD}$  determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note—AN-90.

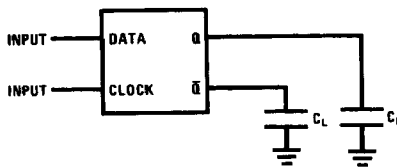
## Switching Time Waveform



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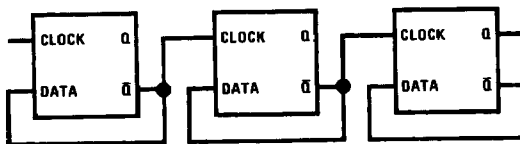
### AC Test Circuit



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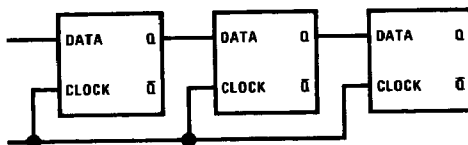
### Typical Applications

Ripple Counter (Divide by 2<sup>n</sup>)



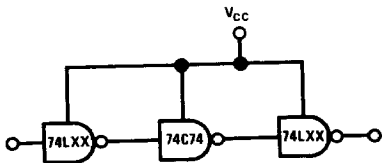
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Shift Register



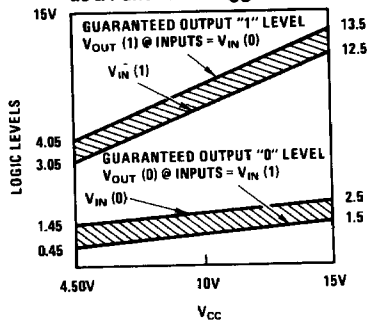
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74C Compatibility



TL/F/5885-7

Guaranteed Noise Margin as a Function of V<sub>CC</sub>



TL/F/5885-8