HEWLETT PACKARD

FDDI 1300 nm Transceiver

Technical Data

HFBR-5125

Features

- **Full Compliance with FDDI PMD Standard**
- **Receiver Sensitivity Exceeds FDDI PMD Standard**
- **Integral Package with Transmitter, Receiver, and MIC/Receptacle**
- **Multisourced Package Style with:**
  - **2 X 11 Pins**
  - **User Installable Key**
- **Single +5 V Power Supply**
- **Shifted ECL Logic Interface Directly Compatible with FDDI PHY Circuits**
- **Directly Compatible with TAXIchip™ * Encode/ Decode Circuits**
- **High Reliability**
- **High Immunity to EMI/RFI**
- **Wavesolder and Aqueous Wash Compatible**

Applications

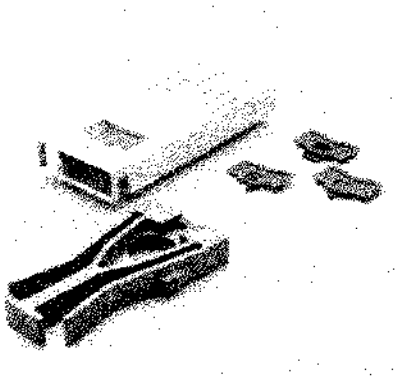
- **FDDI Single or Dual Attachment Stations**
- **FDDI Bridges, Routers, and Concentrators**
- **FDDI Backbone Servers**
- **FDDI Workstations**
- **Non-FDDI Proprietary Data Links**

*TAXIchip™ is a trademark of Advanced Micro Devices, Inc.

Description

The FDDI transceiver described in this data sheet is a member of a growing family of 1300 nm technology fiber optic products available from Hewlett-Packard. FDDI is an acronym for the Fiber Distributed Data Interface local area network standard. This FDDI transceiver product supplies the performance necessary for the system designer who seeks to develop equipment with fully compliant FDDI interfaces per the FDDI Physical Layer Medium Dependent (PMD) standard. This standard has been approved as an International Standard, ISO/IEC 9314-3, and an American National Standard, ANSI X3.166-1990. The performance of this Hewlett-Packard transceiver is guaranteed over the operating temperature and power supply voltage ranges found in most commercial equipment. Sufficient margin exists over the FDDI PMD requirements to allow for substantial equipment mission-life and configuration flexibility.

Hewlett-Packard is a vertically integrated supplier. The 1300 nm LED and PIN devices



along with the three custom bipolar integrated circuits (ICs) used in these products have been developed and manufactured by Hewlett-Packard. The assembly and testing of the transceiver product is performed in facilities wholly-owned and operated by Hewlett-Packard.

Transmitter Section

The transmitter section of the FDDI transceiver uses a 1300 nm InGaAsP LED and a single custom silicon bipolar LED driver integrated circuit. The LED is an advanced planar device with an integral etched lens that provides efficient coupling to multimode fibers when combined with the Hewlett-Packard custom optical subassembly. The driver circuit

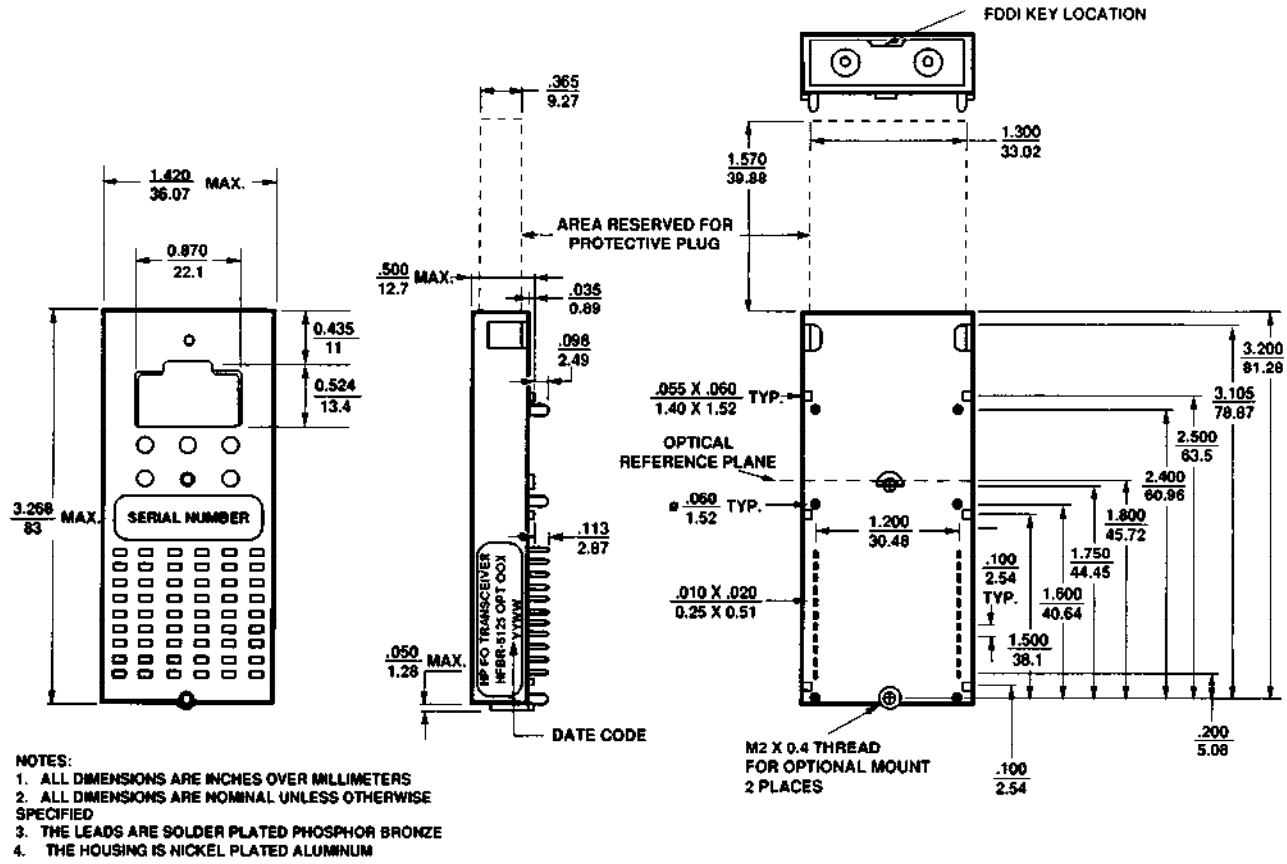


Figure 1. Outline Drawing.

provides temperature compensation for a predictable output optical power over the recommended operating temperature range. It also maintains a steady power supply current due to internal loads which conduct the LED drive current when logic "0"s are being transmitted to minimize creation of high frequency noise on power supply lines. The data input to the transmitter section is differential, 100K ECL compatible, referenced (shifted) to operate from a +5 volt supply.

Receiver Section

The receiver section of the FDDI transceiver uses a 1300 nm InGaAs PIN photodiode and two custom silicon bipolar integrated circuits. The PIN is a planar top-illuminated device which provides ease of assembly into the Hewlett-Packard custom optical subassembly. The preamplifier IC is mounted in the optical subassembly with the PIN detector to maximize the receiver sensitivity. This sensitivity is guaranteed over a wide time-window in the data output eye-pattern. The second IC, a quantizer, provides the final pulse shaping for the logic output and the Signal Detect function. Both the Data and Signal Detect logic outputs are differential, 100K ECL compatible, referenced (shifted) to a +5 volt power supply.

A strong attribute of the receiver section of this transceiver is the ability to provide excellent sensitivity over a wide output data eye-opening. A wide

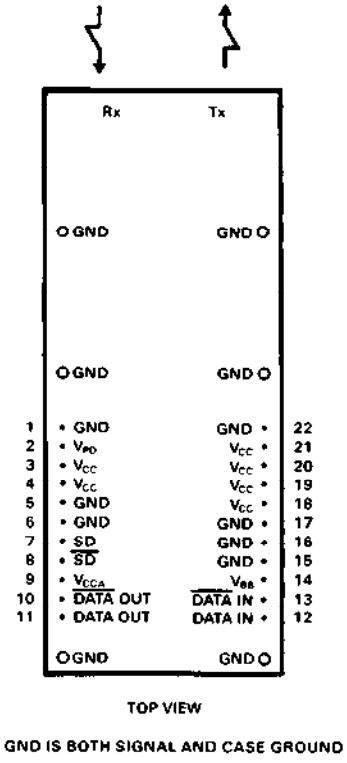


Figure 2. Pin Assignments.

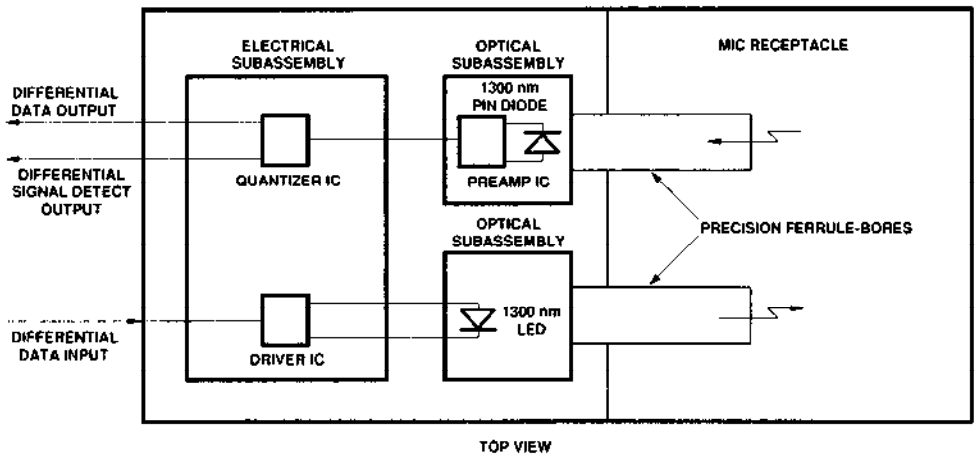


Figure 3. Block Diagram.

window time-width (eye-opening) that results in only a small sensitivity change from the center symbol time-position relaxes strict timing requirements on the FDDI PHY clock recovery circuitry. The receiver sensitivity is guaranteed over a wide 4.6 ns window time-width under minimum input jitter conditions. This wide window time-width ensures that under maximum FDDI PMD worst case Active Input Interface peak-to-peak jitter conditions of DCD (1.0 ns), DDJ (1.2 ns), and RJ (0.76 ns), the receiver will maintain a minimum 2.13 ns window time-width for a clock recovery circuit per the example in the FDDI PMD Annex E. Receiver tests using wider window time-width opening along with corresponding smaller input jitter conditions are equivalent to testing with the larger, worst case FDDI PMD input jitter conditions and the minimum window time-width of 2.13 ns. Please read Note 18 for a detailed explanation.

When only small sensitivity changes occur over a wide window time-width, the clock recovery circuit can exhibit larger static alignment error (a time offset from true center symbol position) plus more data dependent and random clock jitter and still maintain the FDDI PMD error rate requirements. Figure 9 illustrates the typical tradeoff of available window time-width versus sensitivity penalty. Designers can tradeoff for less clock recovery performance with little loss of sensitivity in this Hewlett-Packard receiver.

Package

The overall package concept for the Hewlett-Packard FDDI transceiver consists of three basic elements; the optical subassemblies, the electrical subassembly, and the overall housing with integral FDDI Media Interface Connector Receptacle, MIC/R. The objective of the design is to provide consistent optoelectronic performance in commercial equipment environments over extended equipment mission-lifetimes. The benefits of this integral package are: 1) only one part needs to be inserted into the circuit board; 2) precision alignment between the transmitter and receiver optics and the MIC/R is built-in by Hewlett-Packard.

The package is mechanically attached to the circuit board by wave-soldered posts that eliminate the need for secondary operations which screw or rivet the device to the board. Two tapped holes are provided in the bottom of the package for those circuit board applications where additional, or alternate, mechanical attachment is desired.

The optical subassemblies contain the 1300 nm LED and the 1300 nm PIN with preamplifier IC in hermetic enclosures. These optical subassemblies are actively aligned to the GRIN rod optical elements in the precision ferrule-bores. This active alignment provides optimal optical coupling for both the transmitter and receiver functions. The precision bore assures that the FDDI MIC Plug ferrule tips containing the fibers will

smoothly mate with the optical subassemblies and be precisely positioned relative to the reference plane of the optics.

The electrical subassembly is a thick-film ceramic substrate containing the driver and quantizer integrated circuits along with various surface-mounted passive components. This thick-film substrate provides optimum electrical performance with good noise immunity.

The housing, including the MIC/R, is cast aluminum with nickel plating. Aluminum is used for its excellent thermal conductivity which maintains the junction temperatures of the active semiconductors at the lowest levels possible for high reliability and long mission-life. The optical subassemblies with their precision connector ferrule-bores are attached to the electrical subassembly and precision aligned to the MIC/R. Electrical and optical subassembly signal grounds are connected to the aluminum housing for maximum shielding.

The optical ports in the MIC/R are covered with an easily removable, high temperature, protective plug to prevent contamination during wavesolder assembly of circuit boards and for shipment to end-user sites. This package uses a unique open construction which is compatible with wavesolder and aqueous wash assembly procedures used in the industry today.

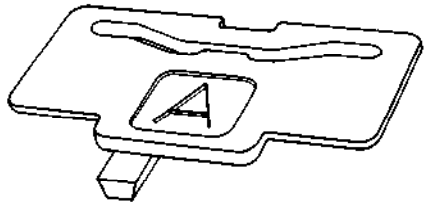
The transceiver is delivered in a specially designed shipping container to protect the part from mechanical or ESD damage during shipment or storage.

Product Reliability Data

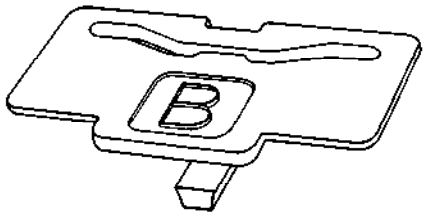
Various environmental and life tests have been performed on these products and these tests are ongoing. Contact your local Hewlett-Packard sales representative to obtain copies of the summaries of these test results as they become available.

Ordering Information

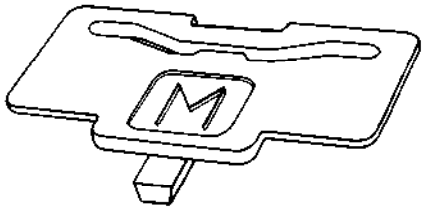
The Hewlett-Packard FDDI Transceiver is available packaged either with or without key inserts per Table 1 below. These parts replace the original fixed key version of the HFBR-5125 transceiver which were sold under the part numbers HFBR-5125 Options 00A, 00B, 00M, 00S, or 00N. Figure 4 shows the key inserts which are black plastic parts with an identifying key letter code molded into the top surface of each key.



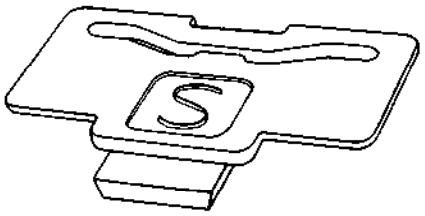
A KEY INSERT



B KEY INSERT



M KEY INSERT



S KEY INSERT

NOTES:
1. ALL KEY INSERTS MATE WITH KEYHOLE IN TOP OF TRANSCEIVER SHOWN IN FIGURE 1.
2. ALL KEY INSERTS ARE BLACK PLASTIC.

Figure 4. Key Inserts.

Table 1. Ordering Information

Product Number	Description
HFBR-5125 Option ALL	Transceiver with a set of 4 key inserts (A, B, M, and S)
HFBR-5125 Option 0FN	Transceiver with no key inserts included
HFBR-ABMS	Bag of 50 bags of 4 key inserts (A, B, M, and S)
HFBR-000A	Bag of 100 A key inserts
HFBR-000B	Bag of 100 B key inserts
HFBR-000M	Bag of 100 M key inserts
HFBR-000S	Bag of 100 S key inserts

FDDI Transceiver

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Storage Temperature	T_S	-40		100	°C	
Operating Temperature-Ambient	T_A	-10		80	°C	Note 1
Lead Soldering Temperature	T_{SOLD}			270	°C	
Lead Soldering Time	t_{SOLD}			4	sec.	
Supply Voltage	V_{CC}	-0.5		7.0	V	Note 2
Data Input Voltage	V_I	-0.5		V_{CC}	V	
Differential Input Voltage	V_D			1.4	V	Note 3
Output Current	I_O			50	mA	Note 4

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by electrostatic discharge (ESD).

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Operating Temperature-Ambient	T_A	0		70	°C	Note 1
Supply Voltage	V_{CC}	4.75		5.25	V	Note 2
Supply Voltage – ECL Driver	V_{CCA}	4.75		5.25	V	Note 2
Supply Voltage – PIN	V_{PD}	4.75		5.25	V	Note 2
Data Input Voltage – Low	$V_{IL} - V_{CC}$	-1.810		-1.475	V	
Data Input Voltage – High	$V_{IH} - V_{CC}$	-1.165		-0.880	V	
Data and Signal Detect Output Load	R_L		50		Ω	Note 5
Signaling Rate	fs	10		125	MBd	Note 6 Figures 5, 6

Transmitter Section

Transmitter Electrical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CC}		220	240	mA	Note 7
Power Dissipation	P_{DISS}		1.1	1.2	W	Note 7
Threshold Voltage	V_{BB} - V_{CC}	-1.420		-1.240	V	Note 8
Data Input Current – Low	I_{IL}	-350			µA	
Data Input Current – High	I_{IH}			350	µA	

Transmitter Optical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Output Optical Power 62.5/125 µm, NA = 0.275 Fiber	P_O	-18.5	-16.5	-14	dBm avg	Note 9
50/125 µm, NA = 0.20 Fiber	P_O	-23.5	-20.8	-17	dBm avg	Note 9, 10
Output Optical Power Temperature Coefficient	$\frac{\Delta P_O}{\Delta T}$		-0.015	-0.02	dB/°C	
Optical Extinction Ratio			0.01 -40	1 -20	% dB	Note 11
Center Wavelength	λ_C	1270	1300	1380	nm	Note 12 Figure 7
Spectral Width – FWHM	$\Delta\lambda$		130	170	nm	Note 13 Figure 7
Optical Rise Time	t_r	0.6	0.85	3.0	ns	Note 14 Figures 7, 8
Optical Fall Time	t_f	0.6	2.0	3.0	ns	Note 14 Figures 7, 8
Duty Cycle Distortion	DCD		0.03	0.4	ns pk-to-pk	Note 15
Data Dependent Jitter	DDJ		0.20	0.6	ns pk-to-pk	Note 16
Random Jitter	RJ		0.01	0.69	ns pk-to-pk	Note 17

Receiver Section

Receiver Optical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Input Optical Power						
Minimum at Window Edge	$P_{IN\ Min}$ (W)		-35	-33	dBm avg	Note 18 Figure 9
Minimum at Center	$P_{IN\ Min}$ (C)		-37	-34.5	dBm avg	Note 19 Figure 9
Maximum	$P_{IN\ Max}$	-14	-13		dBm avg	
Operating Wavelength	λ	1270		1380	nm	
Signal Detect						
Asserted	P_A	P_D + 1.5 dB	-36.2	-33.5	dBm avg	Note 20, 30 Figure 10
Deasserted	P_D	-45	-38.5		dBm avg	Note 21, 31 Figure 10
Hysteresis	P_A - P_D	1.5	2.3		dB	Figure 10

Receiver Electrical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CC}		70	115	mA	Note 22
Supply Current	I_{CCA}		30	50	mA	Note 22
Supply Current – PIN Diode	I_{PD}		35	500	µA	Note 23
Power Dissipation	P_{DISS}		0.3	0.5	W	Note 24
Data Output Voltage – Low	V_{OL} - V_{CC}	-1.840		-1.620	V	Note 25
Data Output Voltage – High	V_{OH} - V_{CC}	-1.045		-0.880	V	Note 25
Data Output Rise Time	t_r	0.35	0.7	2.2	ns	Note 26
Data Output Fall Time	t_f	0.35	0.7	2.2	ns	Note 26
Duty Cycle Distortion	DCD		0.18	0.4	ns pk-to-pk	Note 27
Data Dependent Jitter	DDJ		0.5	1.0	ns pk-to-pk	Note 28
Random Jitter	RJ			2.14	ns pk-to-pk	Note 29
Signal Detect						
Output Voltage – Low	V_{OL} - V_{CC}	-1.840		-1.620	V	Note 25
Output Voltage – High	V_{OH} - V_{CC}	-1.045		-0.880	V	Note 25
Output Rise Time	t_r	0.6	1.0	2.2	ns	Note 26
Output Fall Time	t_f	0.6	1.0	2.2	ns	Note 26
Assert Time (off to on)	AS_Max	0	50	100	µs	Note 20, 30 Figure 10
Deassert Time (on to off)	ANS_Max	0	190	350	µs	Note 21, 31 Figure 10

Notes:

1. This maximum rating applies to still air environments around the transceiver.
2. When component testing these products all supply voltages should be applied simultaneously to avoid damage to the part.
3. This is the maximum voltage that can be applied across the Differential Transmitter Data Inputs to prevent damage to the input ESD protection circuit.
4. When component testing these products do not short the receiver data or signal detect outputs directly to ground to avoid damage to the part.
5. The outputs are terminated with 50 Ω connected to V_{CC} - 2 V.
6. The specified signaling rate of 10 MBd to 125 MBd guarantees operation of the transmitter and receiver link to the full conditions listed in the FDDI Physical Layer Medium Dependent standard. Specifically, the link bit error ratio will be equal to or better than 2.5×10^{-10} for any valid FDDI pattern. The transmitter section of the link is capable of dc to 125 MBd. The receiver is internally ac-coupled which limits the lower signaling rate to 10 MBd. For purposes of definition, the symbol rate (Baud), also called signaling rate, fs, is the reciprocal of the shortest symbol time. Data rate (bits/sec) is the symbol rate divided by the encoding factor used to encode the data (symbols/bit).
7. The power supply current needed to operate the transmitter is provided to differential ECL circuitry. This circuitry maintains a nearly constant current flow from the power supply. Constant current operation helps to prevent unwanted electrical noise from being generated, whether the noise is conducted or emitted, to neighboring receiver or logic circuitry.
8. This value is measured with an output load R_L = 10 kΩ.
9. These optical power values are measured with the following conditions:
   - At the Beginning Of Life (BOL).
   - Over the specified operating voltage and temperature ranges.
   - With HALT Line State, (12.5 MHz square-wave), input signal.
   - At the end of one meter of noted optical fiber with cladding modes removed.

   The average power value can be converted to a peak power value by adding 3 dB.
   Higher output optical power transmitters are available on special request.
10. If 50/125 um fiber cable with a 0.22 NA is used the Output Optical Power values stated for 50/125 um 0.20 NA fiber cables will all improve by 1 dB.
11. The Extinction Ratio is a measure of the modulation depth of the optical signal. The data "0" output optical power is compared to the data "1" peak output optical power and expressed as a percentage. With the transmitter driven by a HALT Line State (12.5 MHz square-wave) signal the optical signal is detected with a receiver that linearly converts optical power to voltage. The extinction ratio is the ratio of the voltage of the "0" level compared to the voltage at the "1" level expressed as a percentage.
12. This parameter complies with the FDDI PMD requirements for the tradeoffs between center wavelength, spectral width, and rise/fall times shown in Figure 7. The temperature coefficient of the center wavelength is typically +0.37 nm/°C.
13. This parameter complies with the FDDI PMD requirements for the tradeoffs between center wavelength, spectral width, and rise/fall times shown in Figure 7. The temperature coefficient of the spectral width is typically +0.25 nm/°C.
14. This parameter complies with the FDDI PMD requirements for the tradeoffs between center wavelength, spectral width, and rise/fall times shown in Figure 7. This parameter also complies with the optical pulse envelope shown in Figure 8. The optical rise and fall times are measured from 10% to 90% when the transmitter is driven by the FDDI HALT Line State (12.5 MHz square-wave) input signal.
15. Duty Cycle Distortion is measured at a 50% threshold using an IDLE Line State, 125 MBd (62.5 MHz square-wave), input signal. The maximum value for this parameter is 0.2 ns better than required by the FDDI PMD standard.
16. Data Dependent Jitter is specified with the FDDI test pattern described in FDDI PMD Annex A.5.
17. Random Jitter is specified with an IDLE Line State, 125 MBd (62.5 MHz square-wave), input signal.
18. This specification is intended to indicate the performance of the receiver section of the transceiver when Input Optical Power signal characteristics are present per the following definitions. These performance values will be the same for either 62.5/125 µm or 50/125 µm fiber cables. The Input Optical Power dynamic range from the minimum level (with a window time-width) to the maximum level is the range over which the receiver is guaranteed to provide output data with a Bit Error Ratio (BER) better than or equal to 2.5×10^{-10}. The BER will be better than or equal to 1×10^{-12} at input optical power levels greater than $P_{IN\ Min}$ plus approximately 0.8 dB with this Hewlett-Packard receiver. This is 1.2 dB better than required by the FDDI PMD. The measurement conditions are stated below.

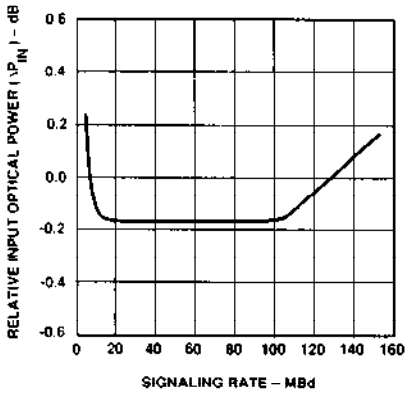
    - At the Beginning of Life (BOL)
    - Over the specified operating temperature and voltage ranges
    - Input symbol pattern is the FDDI test pattern defined in FDDI PMD Annex A.5 with 4B/5B NRZI encoded data that contains a duty cycle base-line wander effect of 50 kHz. This sequence causes a near worst case condition for inter-symbol interference.
    - Input optical rise and fall times are approximately 1 ns and 2 ns respectively.
    - Receiver data window time-width is 2.13 ns or greater and centered at mid-symbol. This worst case window time-width is the minimum allowed eye-opening presented to the FDDI PHY PM_Data.indication input (PHY input) per the example in FDDI PMD Annex E. This minimum window time-width of 2.13 ns is based upon the worst case FDDI PMD Active Input Interface optical conditions for peak-to-peak DCD (1.0 ns), DDJ

(1.2 ns) and RJ (0.76 ns) presented to the receiver.

To test a receiver with the worst case FDDI PMD Active Input jitter conditions require exacting control over DCD, DDJ and RJ jitter components that is difficult to implement with production test equipment. The receiver can be equivalently tested to the worst case FDDI PMD input jitter conditions and meet the minimum output data window time-width of 2.13 ns. This is accomplished by using a nearly ideal input optical signal (no DCD, insignificant DDJ and RJ) and measuring for a wider window time-width of 4.6 ns. This is possible due to the accumulative effect of jitter components through their superposition (DCD and DDJ are directly additive and RJ components are rms additive). Specifically, when a nearly ideal input optical test signal is used and the maximum receiver peak-to-peak jitter contributions of DCD (0.4 ns), DDJ (1.0 ns) and RJ (2.14 ns) exist, the minimum window time-width becomes 8.0 ns - 0.4 ns - 1.0 ns - 2.14 ns = 4.46 ns, or conservatively 4.6 ns. This wider window time-width of 4.6 ns guarantees the FDDI PMD Annex E minimum window time- width of 2.13 ns under worst case input jitter conditions to the Hewlett-Packard receiver.

- Transmitter operating with an IDLE Line State pattern, 125 MBd (62.5 MHz square-wave), input signal to simulate any cross-talk present between the transmitter and receiver sections of the transceiver.

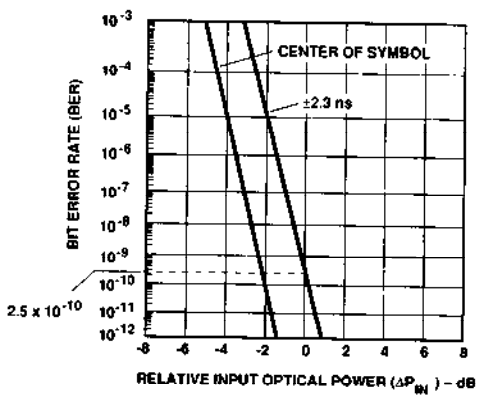
19. All conditions of Note 18 apply except that the measurement is made at the center of the symbol with no window time-width.
20. This value is measured during the transition from low to high levels of input optical power.
21. This value is measured during the transition from high to low levels of input optical power. The minimum value will be either -45 dBm average or when the input optical power yields a BER of 10^{-2} or better, whichever power is higher.
22. These values are measured with the outputs terminated into 50 Ω connected to V_{CC} - 2 V.
23. Measured at P_{IN} = -14 dBm average.
24. The power dissipation value is the power dissipated in the receiver itself. Power dissipation is calculated as the sum of the products of supply voltage and supply currents, minus the sum of the products of the output voltages and currents.
25. These values are measured with respect to V_{CC} with the output terminated into 50 Ω connected to V_{CC} - 2 V. The minimum values are corrected for +5.25 V operation for 100 K ECL values that are usually specified at -4.8 V operation.
26. The output rise and fall times are measured between 20% and 80% levels with the output connected to V_{CC} - 2 V through 50 Ω.
27. Duty Cycle Distortion is measured at 50% threshold using an IDLE Line State, 125 MBd (62.5 MHz square-wave), input signal. The input optical power level is -20 dBm average.
28. Data Dependent Jitter is specified with the FDDI test pattern described in PMD Annex A.5. The input optical power level is -20 dBm average.
29. Random Jitter is specified with an IDLE Line State, 125 MBd (62.5 MHz square-wave), input signal. The input optical power level is at maximum "$P_{IN\ Min}$ (W)".
30. The Signal Detect output shall be asserted within 100 µs after a step increase of the Input Optical Power. The step will be from a low Input Optical Power, ≤ -45 dBm, into the range between greater than P_A, and -14 dBm. The BER of the receiver output will be 10^{-2} or better during the time, LS_Max (15 µs) after Signal Detect has been asserted. See Figure 10 for more information.
31. Signal detect output shall be deasserted within 350 µs after a step decrease in the Input Optical Power from a level which is the lower of; -31 dBm or P_D + 4 dB (P_D is the power level at which signal detect was deasserted), to a power level of -45 dBm or less. This step decrease will have occurred in less than 8 ns. The receiver output will have a BER of 10^{-2} or better for a period of 12 µs or until signal detect is deasserted. The input data stream is the Quiet Line State. Also, signal detect will be deasserted within a maximum of 350 µs after the BER of the receiver output degrades above 10^{-2} for an input optical data stream that decays with a negative ramp function instead of a step function. See Figure 10 for more information.



CONDITIONS:

1. P_{IN} NORMALIZED (ΔP_{IN} = 0 dB) TO $P_{IN\ Min}$ (C) AT 125 MBd AT CENTER OF SYMBOL.
2. $\Delta P_{IN} = P_{IN}$ @ MBd - P_{IN} @ 125 MBd
3. FDDI PMD APPENDIX A.5 125 MBd TEST PATTERN WITH 50 kHz BASELINE WANDER
4. BER = 2.5 X 10^{-10}
5. T_A = 25°C
6. V_{CC} = 5 Vdc
7. INPUT OPTICAL RISE/FALL TIMES = 1.0 ns/2.1 ns

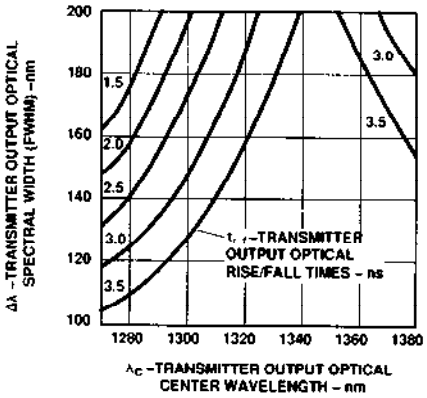
Figure 5. Relative Input Optical Power vs. Signaling Rate.



CONDITIONS:

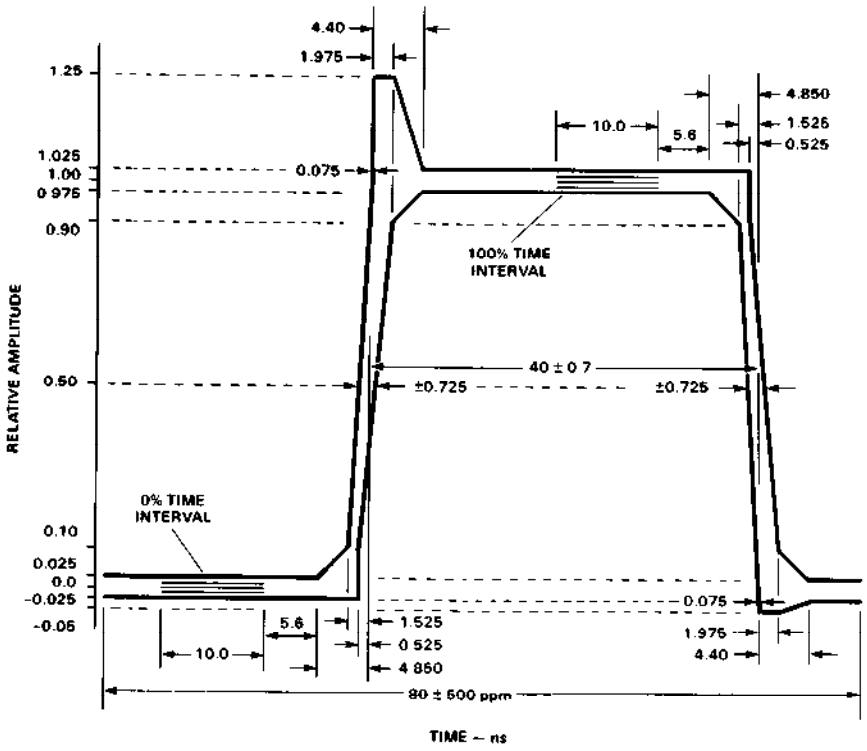
1. P_{IN} IS NORMALIZED (ΔP_{IN} = 0 dB) AT $P_{IN\ Min}$ (W) WITH BER = 2.5 x 10^{-10} AND WINDOW TIME-WIDTH OF ±2.3 ns EITHER SIDE OF SYMBOL CENTER.
2. $\Delta P_{IN} = P_{IN}$ @ BER - P_{IN} @ 2.5 x 10^{-10} BER
3. FDDI PMD APPENDIX A.5 125 MBd TEST PATTERN WITH 50 kHz BASELINE WANDER.
4. T_A = 25°C
5. V_{CC} = 5.0 Vdc
6. INPUT OPTICAL RISE/FALL TIMES = 1.0 ns/2.1 ns

Figure 6. Typical Bit Error Rate vs. Relative Input Optical Power.



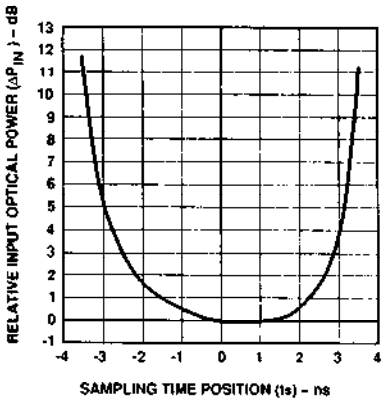
HEWLETT PACKARD FDDI TRANSMITTER TEST RESULTS OF λ_C, $\Delta\lambda$ AND t_r, t_f ARE CORRELATED AND COMPLY WITH THE ALLOWED SPECTRAL WIDTH AS A FUNCTION OF CENTER WAVELENGTH FOR VARIOUS RISE AND FALL TIMES.

Figure 7. Transmitter Output Optical Spectral Width (FWHM) vs. Transmitter Output Optical Center Wavelength and Rise/Fall Times.



THE OUTPUT OPTICAL PULSE SHAPE SHALL FIT WITHIN THE BOUNDARIES OF THE PULSE ENVELOPE. FOR RISE AND FALL TIME MEASUREMENTS, THE MAXIMUM POSITIVE AND MINIMUM NEGATIVE WAVEFORM EXCURSIONS IN THE ZERO AND 100% TIME INTERVALS SHALL BE CENTERED AROUND THE 0.0 AND 1.00 LEVELS, RESPECTIVELY. A MINIMUM BANDWIDTH RANGE OF 100 kHz TO 750 MHz IS REQUIRED FOR THE MEASUREMENT EQUIPMENT USED TO EVALUATE THE PULSE ENVELOPE.

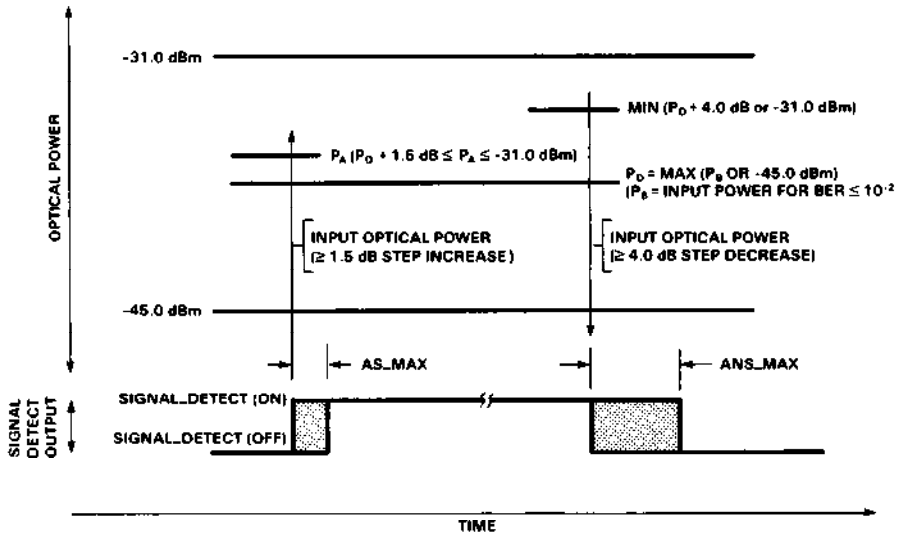
Figure 8. Output Optical Pulse Envelope.



CONDITIONS:

1. P_{IN} IS NORMALIZED TO $P_{IN\ Min}$ (C) AT CENTER OF SYMBOL.
2. $\Delta P_{IN} = P_{IN}$ @ t_s - P_{IN} @ t_{center}
3. FDDI PMD APPENDIX A.5 125 MBd TEST PATTERN WITH 50 kHz BASELINE WANDER.
4. BER = 2.5 x 10^{-10}
5. T_A = 25°C
6. V_{CC} = 5 Vdc
7. INPUT OPTICAL RISE/FALL TIMES = 1.0 ns/2.1 ns

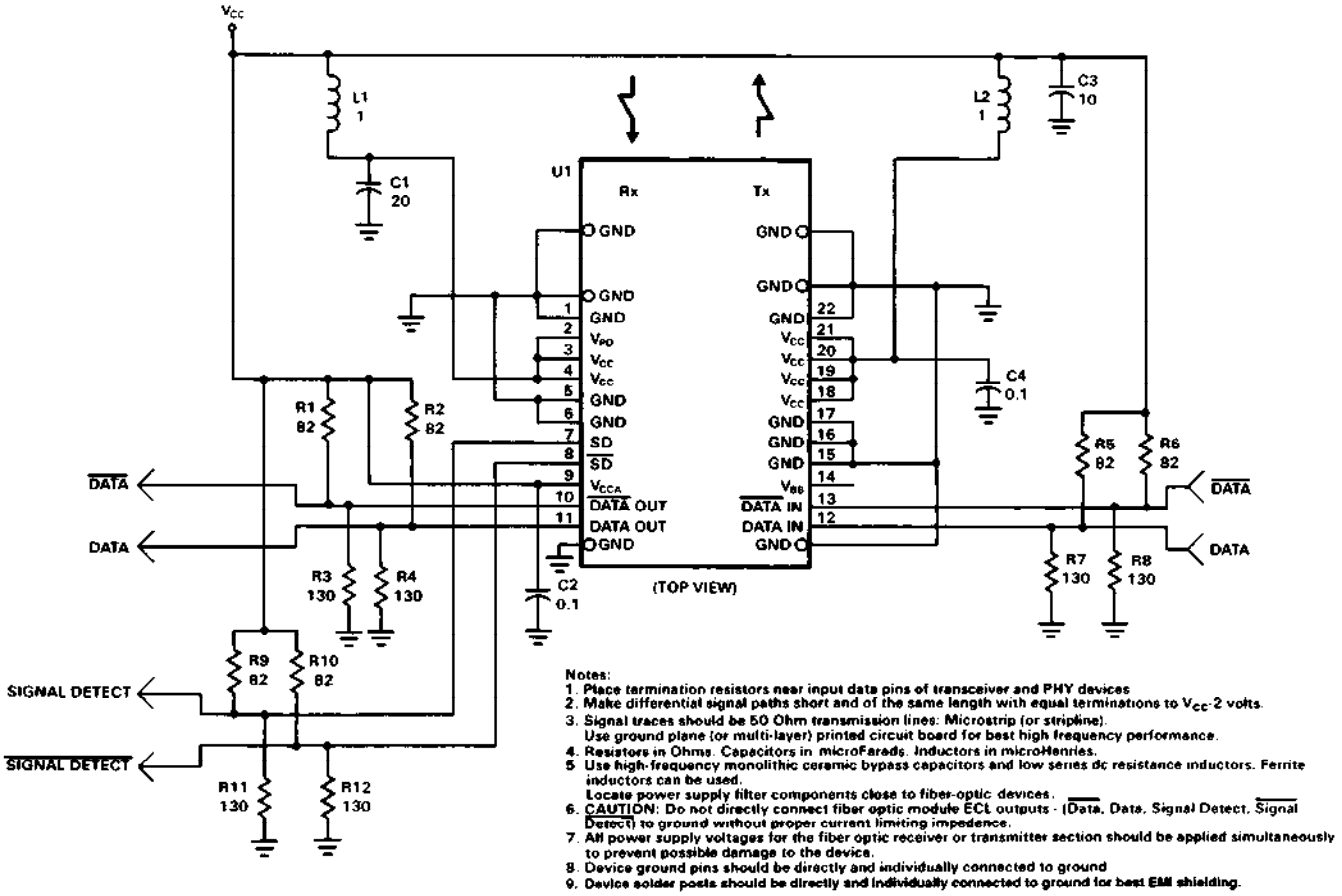
Figure 9. Relative Input Optical Power vs. Sampling Time Position.



AS_MAX—MAXIMUM ACQUISITION TIME (SIGNAL).
AS_MAX IS THE MAXIMUM SIGNAL_DETECT ASSERTION TIME FOR THE STATION.
AS_MAX SHALL NOT EXCEED 100.0 μs. THE DEFAULT VALUE OF AS_MAX IS 100.0 μs.

ANS_MAX—MAXIMUM ACQUISITION TIME (NO SIGNAL).
ANS_MAX IS THE MAXIMUM SIGNAL_DETECT DEASSERTION TIME FOR A STATION.
ANS_MAX SHALL NOT EXCEED 350 μs. THE DEFAULT VALUE OF ANS_MAX IS 350 μs.

Figure 10. Signal Detect Thresholds and Timing.



Notes:
1. Place termination resistors near input data pins of transceiver and PHY devices
2. Make differential signal paths short and of the same length with equal terminations to V_{CC}-2 volts.
3. Signal traces should be 50 Ohm transmission lines: Microstrip (or stripline).
   Use ground plane (or multi-layer) printed circuit board for best high frequency performance.
4. Resistors in Ohms. Capacitors in microFarads. Inductors in microHenries.
5. Use high-frequency monolithic ceramic bypass capacitors and low series dc resistance inductors. Ferrite inductors can be used.
   Locate power supply filter components close to fiber-optic devices.
6. CAUTION: Do not directly connect fiber optic module ECL outputs - ($\overline{Data}$, Data, Signal Detect, $\overline{Signal\ Detect}$) to ground without proper current limiting impedence.
7. All power supply voltages for the fiber optic receiver or transmitter section should be applied simultaneously to prevent possible damage to the device.
8. Device ground pins should be directly and individually connected to ground
9. Device solder posts should be directly and individually connected to ground for best EMI shielding.

Figure 11. Recommended Decoupling Circuit Diagram.

Application Assistance

The Applications Engineering group in the Hewlett-Packard Optical Communication Division is available to assist with the technical understanding and design trade-offs associated with this FDDI transceiver. You can contact them through your local Hewlett-Packard sales representative.

The following information is provided to answer some of the most common application questions that have been asked relative to the use of the HFBR-5125 transceiver.

Board Layout - Decoupling Circuit and Ground Planes

It is important to take care in the layout of your circuit board to achieve optimum performance from the HFBR-5125 transceiver. Figure 11 provides a good example of a schematic for a decoupling circuit that works well with this product. It is further recommended that a contiguous ground plane be provided in the circuit board directly under the transceiver to provide a low inductance ground for signal return current. This recommendation is in keeping with good high frequency board layout practices. Layouts that overlay the multisourced 2X11 footprint with the alternative 1X13 transceiver footprint need to pay special attention to this recommendation for a contiguous ground plane under the transceiver to achieve good performance.

Board Layout - Hole Pattern

Figure 12 shows the recommended board hole pattern to be used for the HFBR-5125 transceiver. This recommendation complies with the original Multisource FDDI Transceiver definition announced by AT&T, Hewlett-Packard, and Siemens in 1989. This hole size and location recommendation allows for easy insertion of the transceiver into the circuit board during assemble operations.

To interpret Figure 12 it is important to remember to allow for some positional tolerance beyond the perfect position noted and trade this off for tighter hole size tolerance. For example, if you desire a 0.006 inch tolerance on hole location then the consequent hole size should be held to 0.076 inch minimum instead of 0.070 minimum allowed for the case where the holes would be drilled in the perfect location.

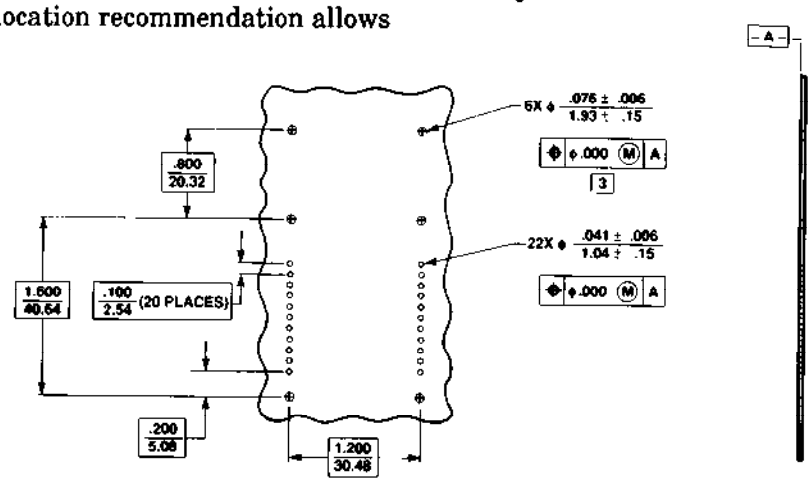


Figure 12. Board Layout – Hole Pattern.

Table 2. FDDI Application Environments

Environment	Data Centre	Office/Building	Campus
Number of Stations	small number	large number	large number
Number of Optically Bypassed Stations	4 maximum at 0 to 2.5 dB attenuation each	unspecified, implied use of concentrators with electrical bypassing	none allowed in 2 km maximum link length, implied use of concentrators with electrical bypassing
Maximum Active Station Separation	400 m maximum	unspecified, 2 km maximum implied	2 km maximum
In-line Connectors/ Slices	unspecified few implied	unspecified several implied	unspecified few implied

Table 3. FDDI PMD Optical Power Budget Specifications - End Of Life (EOL)

Fiber Cable	Active Output Interface (EOL)	Active Input Interface (EOL)	Optical Power Budget (EOL)	FDDI PMD Reference
62.5/125 µm 0.275 NA	-20 dBm	-31 dBm	11 dB	Section 8 Tables 1 and 2
50/125 µm 0.20 NA	-25 dBm	-31 to -32 dBm	6 -7 dB	Annex C Table C.3

Optical Power Budget Allocation

The FDDI PMD standard was created to serve three major application environments. Each of these applications allocates the optical power budget provided by the FDDI PMD optical interface in different ways. Table 2 summarizes the configuration assumptions that are described in the FDDI PMD Section 5.2 Environments. Each FDDI installation will be unique so these Application Environment examples are to be viewed as typical only. It is the network specifier's responsibility to stay within the optical power budget limits set by the PMD standard to maintain network integrity for multiple or single vendor networks.

Empirical measurements and mathematical link models were used by the ANSI X3T9.5 FDDI Standard Committee to derive the actual optical power budgets required to meet these performance objectives for both 62.5/125 um and 50/125 um fiber cables. These specifications are summarized in Table 3. These values must be met over the useful life of the equipment under all specified environmental conditions for the equipment in order to ensure the interoperability objective of the FDDI standard.

Figure 13, Optical Power Budget vs Link Length, illustrates the allocation of optical power budget between the fiber cable, attenuation and dispersion loss per metre, and the remaining power available for passive cable plant losses such as in-line connectors, splices, and optical bypass switches. These graphs were generated using a link model similar to the model used by the ANSI X3T9.5 FDDI committee to derive the Active Output/Input Interface requirements in the FDDI PMD. The fiber cable parameters used in the model are the same as those specified in the FDDI PMD Section 10 Cable Plant Interface Specification along with a conservative 1.5 dB/km attenuation specification.

Curves HP 62.5/125 and HP 50/125 in Figure 13 display the optical power budget provided in networks using equipment exclusively designed with the Hewlett-Packard HFBR-5125 transceiver. End of Life (EOL) values for the Hewlett-Packard transceiver will vary depending on the installation environment and mission life of the equipment that it is used in. Assuming normal commercial operation for 10 years, the HFBR-5125 will experience approximately 0.5 dB decrease in optical power budget. See Table 4 for the derivation of these curves.

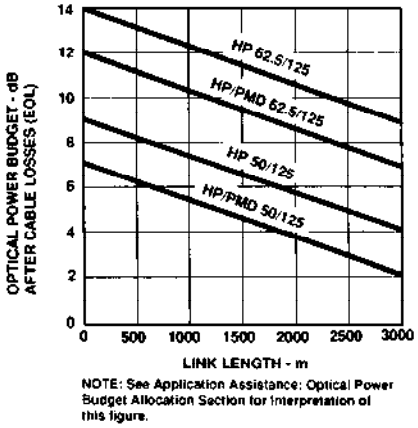


Figure 13. Optical Power Budget After Cable Losses (EOL).

Table 4. Derivation of HP Curves in Figure 13

Fiber Cable	HP Transmitter Coupled Power BOL/EOL	HP Receiver Sensitivity BOL/EOL	Optical Power Budget BOL/EOL
62.5/125 µm 0.275 NA	-18.5 dBm/-19 dBm	-33 dBm/-33 dBm	14.5 dB/14 dB
50/125 µm 0.20 NA	-23.5 dBm/-24 dBm	-33 dBm/-33 dBm	9.5 dB/9 dB

Table 5. Derivation of HP/PMD Curves in Figure 13

Fiber Cable	HP Transmitter Coupled Power BOL/EOL	PMD Receiver Sensitivity EOL	Optical Power Budget EOL
62.5/125 µm 0.275 NA	-18.5 dBm/-19 dBm	-31 dBm	12 dB
50/125 µm 0.20 NA	-23.5 dBm/-24 dBm	-31 to -32 dBm	7 to 8 dB
	PMD Transmitter Coupled Power EOL	**HP Receiver Sensitivity BOL/EOL**	**Optical Power Budget EOL**
62.5/125 µm 0.275 NA	-20 dBm	-33 dBm/-33 dBm	13 dB
50/125 µm 0.20 NA	-25 dBm	-33 dBm/-33 dBm	8 dB

Curves HP/PMD 62.5/125 and HP/PMD 50/125 in Figure 13 display the optical power budget provided in networks where equipment using the Hewlett-Packard transceivers is mixed with equipment using transceivers that comply with just the minimum performance required by the FDDI PMD standard. The resulting optical power budgets are somewhat lower than in the Hewlett-Packard exclusive case. See Table 5 for the derivation of these curves.

The interpretation of Figure 13 is that the power budget at zero cable length is totally available to use for non-cable related passive losses such as connectors, splices, and optical bypass switches. Aging and other End of Life changes have already been incorporated into the baseline values per the assumptions in Tables 4 and 5. As the distance between stations increases, optical power budget is used to overcome fiber cable attenuation and dispersion losses which leaves the budget under the curve for use to overcome other passive cable plant losses.

It should be noted that the Hewlett-Packard transceiver provides approximately 10.5 dB optical power budget for passive losses at the maximum FDDI PMD distance of 2000 m of 62.5/125 µm fiber cable and approximately 5.5 dB for passive losses at the maximum FDDI PMD distance of 2000 m of 50/125 µm 0.20 NA cable. The comparable results, when equipment with HP transceivers interface to equipment with only FDDI PMD standard performance transceivers, is that approximately 8.5 dB and 3.5 dB are available for passive losses in 62.5/125 µm and 50/125 µm 0.20 NA fiber cables. In either case, sufficient optical power budget is available at the End of Life to overcome passive losses associated with the various application Environments described in the FDDI PMD.

Further details concerning the link model and detailed assumptions that were used to create the Optical Power Budget curves in Figure 13 are available by contacting the Applications Engineering group in the Hewlett-Packard Optical Communication Division via your local sales representative.

Electromagnetic Interference (EMI)

Most equipment designs that incorporate the FDDI interface are subject to governmental EMI emissions regulations. Successful designs must take into account the high frequency nature of the FDDI interface. Potential sources of EMI are the serial 125 MBd interconnection between the FDDI PMD and PHY functional blocks and the high speed clock circuit. Care must be taken in circuit board layout to minimize sources of emissions. It is also important to shield the transceiver MIC/R (Media Interface Connector/ Receptacle) aperture through the equipment chassis in order to minimize potential EMI leakage.

The Hewlett-Packard FDDI Transceiver is housed in an aluminum package to provide optimum optoelectronic performance. This aluminum package is internally connected to the transceiver signal ground.

When implementing designs with the HFBR-5125 there are two possible design cases to consider. Either the equipment

chassis design allows, or does not allow, contact between signal/logic ground and the chassis at locations other than at the power supply.

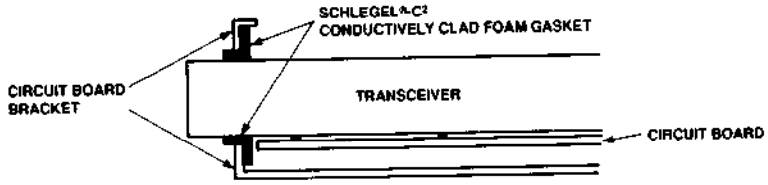
In the case where contact between signal/logic ground and the chassis is allowed, Hewlett-Packard strongly recommends the use of conductive shield or gasket material to seal the gap between the aluminum transceiver package and the equipment chassis. Figure 14 illustrates an example of one inexpensive gasketing technique using the Schlegel Corporation conductively clad foam gasket material.

Some possible sources of EMI shielding products are:

Chomerics Inc.
16 Flagstone Drive
Hudson, NH 03051
Phone: 800-633-8800
or
Chomerics Europe, Inc.
First Avenue
Marlow, Bucks.
SL7 1YA England
Phone: (06284) 6030
Product: EMI shielding laminates

Instrument Specialties
Delaware Water Gap, PA 18327
Phone: 717-424-8510
or
Instrument Specialties
Liege, Belgium
Phone: 32-41-63-3021
Product: Beryllium Copper Alloy shields

Schlegel Corporation
P.O. Box 23197
Rochester, NY 14692
Phone: 800-828-6237



NOTES:
1. THE SCHLEGEL®-C² FOAM GASKET MAY BE ATTACHED TO THE CIRCUIT BOARD BRACKET EITHER WITH ADHESIVE OR MECHANICAL MEANS.
2. SEE APPLICATION ASSISTANCE: ELECTROMAGNETIC INTERFERENCE SECTION FOR MORE INFORMATION.

Figure 14. EMI Gasket Example.

or
N.V. Schlegel S. A.
Rochesterlaan 4
B-8240 Gistel (W.VI.)
Belgium
Phone: (59) 27-72-21
Product: clad foam gaskets

In design environments that do not allow contact between signal/logic ground and the chassis, it is strongly recommended that an external RF cover be used to shield the chassis aperture for the MIC/R. This is especially important in multiple FDDI port applications such as Concentrators.

Electrostatic Discharge (ESD)

There are two design cases in which immunity to ESD damage is important.

The first case is during handling of the transceiver prior to mounting it on the circuit board. It is important to use normal ESD handling precautions for ESD sensitive devices. These precautions include using grounded wrist straps, work benches, and floor mats in ESD controlled work areas.

The Hewlett-Packard HFBR-5125 has been characterized per MIL-STD-883C Method 3015.4 to tolerate up to 1500 Volts between pins on the package without damage. This is within the ESD Class 1 specification range of 0 Volts to 2000 Volts.

The second case to consider is static discharges to the exterior of the equipment chassis after the FDDI interface card is installed. In many equipment designs the MIC/R of the FDDI transceiver is exposed outside the exterior of the chassis. With this exposure it is subject to the same ESD test criteria that applies to the entire product in which it is installed. Another specific exposure occurs whenever a Media Interface Connector/Plug is inserted into the transceiver MIC/R.

The Hewlett-Packard HFBR-5125 transceiver has been characterized to withstand up to a 14 kV air discharge in a power on mode from a Human Body

Model source without catastrophic damage. A test procedure similar to IEC 801-2 was used for this characterization test.

The designer should consider the ESD discharge path to ground. The preferred conduction path in most designs would be through the transceiver case to chassis ground.

In designs that allow contact between chassis and signal/logic ground this can be accomplished either with a conductive shield or gasket between the aluminum Hewlett-Packard transceiver housing and the chassis, or by connecting the transceiver solder posts and/or ground pins to chassis ground on the circuit board.

In the design case where the transceiver is not allowed to contact the chassis, the ESD energy will conduct through the aluminum transceiver package to the equipment signal ground plane via the transceiver solder posts and ground pins.

For more information call:

United States: 1-800-752-0900*

Or write:
Hewlett-Packard Components
Customer Information Center
Building 49 AV
19310 Pruneridge Avenue
Cupertino, California 95014

Canada: (416) 678-9430*

Europe: (49) 7031/14-0*

Asia Pacific/Australia: (65) 291-9088*

Japan: (81 3) 3331-6111*

*Or call your local HP sales office listed in your telephone directory. Ask for a Components representative.

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Obsoletes 5091-0329E/5091-2566E
Printed in U.S.A. 5091-3230E (11/91)